DUAL J-K EDGE-TRIGGERED FLIP-FLOP

S54H103
N74H103

S54H103–A,F,W • N74H103–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These dual monolithic J-K flip-flops are negative-edge-triggered. They feature individual J, K, clock, and asynchronous clear inputs to each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable-will perform according to the truth table as long as minimum setup times are observed. Input data are transferred to the outputs on the negative edge of the clock pulse.

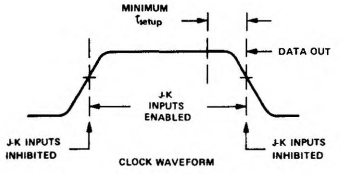
TRUTH TABLE

t_n J	t_n K	t_{n+1} Q
0	0	Q_n
0	1	0
1	0	1
1	1	Q_n

NOTES:

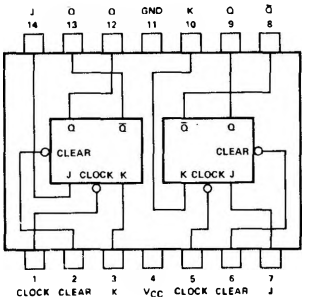
1. t_n = Bit time before clock pulse
2. t_{n+1} = Bit time after clock pulse

CLOCK WAVEFORM

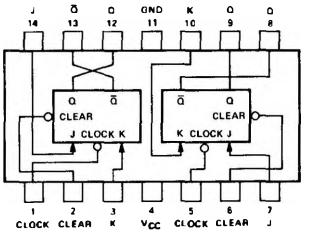


PIN CONFIGURATIONS

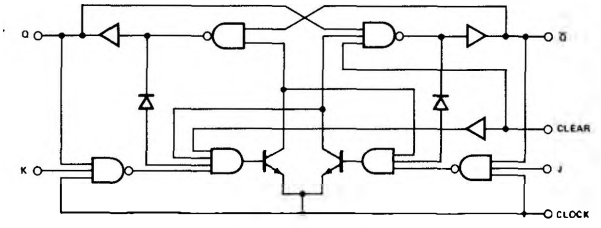
W PACKAGE



A,F PACKAGE



LOGIC DIAGRAM (each flip-flop)



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H103 Circuits		4.5	5	5.5	V
N74H103 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H103 Circuits	-55	25	125	°C
	N74H103 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		10			ns
Width of Clear Pulse, $t_{p(clear)}$		16			ns
Input Setup Time, t_{setup}: Logical 1		10			ns
Logical 0		13			ns
Input Hold Time, t_{hold}		0			ns
Clock Pulse Transition Time, t_0				150	ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -500μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 20mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or clear	V_{CC} = MAX,	V_{in} = 0.4V		-1	-2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,	V_{in} = 0.4V		-3	-4.8	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX,	V_{in} = 2.4V	0		-1	mA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	V_{CC} = MAX,	V_{in} = 2.4V			100	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current **	V_{CC} = MAX,	V_{in} = 0	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX			40	76	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	C_L = 25pF,	R_L = 280Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	C_L = 25pF,	R_L = 280Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output (clock low)	C_L = 25pF,	R_L = 280Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output. (clock high)	C_L = 25pF,	R_L = 280Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25pF,	R_L = 280Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25pF,	R_L = 280Ω	8	16	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed one second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.