

OPEN COLLECTOR POSITIVE-NAND GATE

S54S00

S54S03

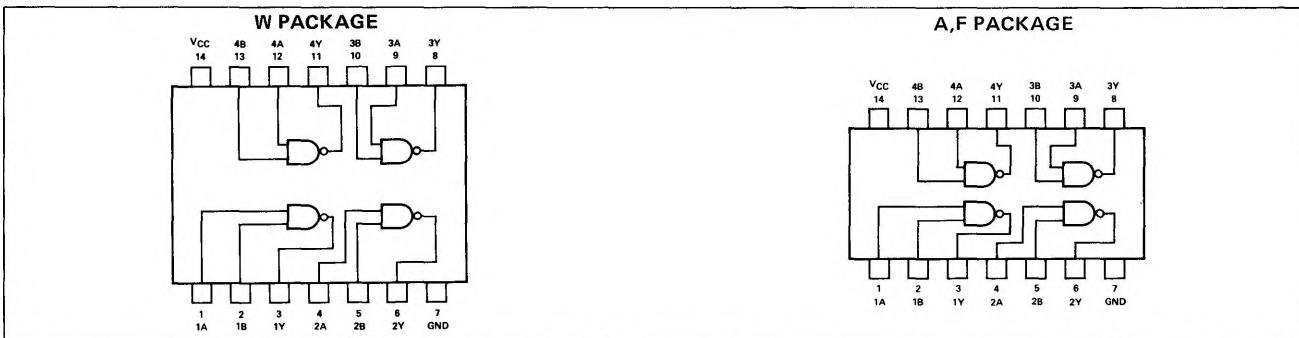
N74S00

N74S03

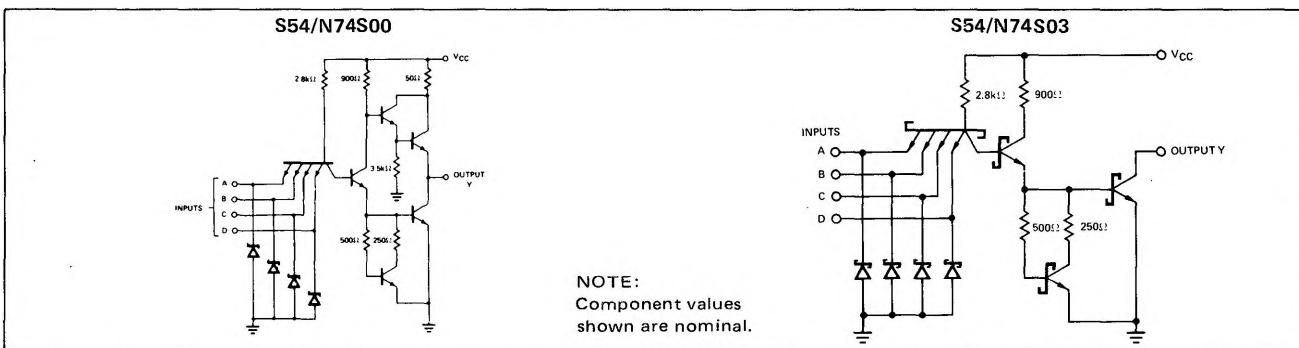
S54S00/503-A,F • N74S00/503-A,F

DIGITAL 54/74 TTL SERIES

PIN CONFIGURATIONS



SCHEMATIC (each gate)



RECOMMENDED OPERATING CONDITIONS

	S54S00			N74S00			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N:			20			20	
High logic level			10			10	
Low logic level			-55		125	0	°C
Operating Free-Air Temperature, T_A						70	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS *	TEST CONDITIONS *			UNIT	
		MIN	TYP **	MAX		
V_{IH}	High-level input voltage			2	V	
V_{IL}	Low-level input voltage			0.8	V	
V_I	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18\text{mA}$		-1.2	V	
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $I_{OH} = -1\text{mA}$	$V_{IL} = 0.8\text{V}$, Series 54S Series 74S	2.5	3.4	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 20\text{mA}$	$V_{IH} = 2\text{V}$,		0.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5\text{V}$		1	mA	
I_{IH}	High-level input current (each input)	$V_{CC} = \text{MAX}$, $V_I = 2.7\text{V}$		50	μA	
I_{IL}	Low-level input current (each input)	$V_{CC} = \text{MAX}$, $V_I = 0.5\text{V}$		-2	mA	
I_{OS}	Short-circuit output current [†]	$V_{CC} = \text{MAX}$		-40	-100	mA
I_{CCH}	Supply current, high-level output (average per gate)	$V_{CC} = \text{MAX}$, All inputs at 0V		2.5	4	mA
I_{CCL}	Supply current, low-level output (average per gate)	$V_{CC} = \text{MAX}$, All inputs at 5V		5	9	mA

SIGNETICS DIGITAL 54/74 TTL SERIES — S54S00 • N74S00 • S54S03 • N74S03

SWITCHING CHARACTERISTICS, $V_{CC} = 5V$, $T_A = 25^\circ C$, $N = 10$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15\text{pF}$, $R_L = 280\Omega$	2	3	4.5	ns
	$C_L = 50\text{pF}$, $R_L = 280\Omega$			4.5	
t_{PHL} Propagation delay time, high-to-low-level output	$C_L = 15\text{pF}$, $R_L = 280\Omega$	2	3	5	ns
	$C_L = 50\text{pF}$, $R_L = 280\Omega$			5	

S54/N74S03

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
V_{IH} High-level input voltage					V
V_{IL} Low-level input voltage			0.8		V
V_I Input clamp voltage		-1.2			V
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{CC} = \text{MIN}$, $V_{OH} = 5.5V$	250			μA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 20\text{mA}$		0.5		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5V$		1		mA
I_{IH} High-level input current (each input)	$V_{CC} = \text{MAX}$, $V_{CC} = \text{MAX}$, $V_I = 2.7V$		50		μA
I_{IL} Low-level input current (each input)	$V_{CC} = \text{MAX}$, $V_{CC} = \text{MAX}$, $V_I = 0.5V$		-2		mA
I_{CCH} Supply current, high-level output (average per gate)	$V_{CC} = \text{MAX}$, All inputs at 0V	1.5	3.3		mA
I_{CCL} Supply current, low-level output (average per gate)	$V_{CC} = \text{MAX}$, All inputs at 5V	5	9		mA

SWITCHING CHARACTERISTICS, $V_{CC} = 5V$, $T_A = 25^\circ C$, $N = 10$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15\text{pF}$, $R_L = 280\Omega$ $C_L = 50\text{pF}$, $R_L = 280\Omega$	2	5	7.5	ns
t_{PHL} Propagation delay time, high-to-low-level output	$C_L = 15\text{pF}$, $R_L = 280\Omega$ $C_L = 50\text{pF}$, $R_L = 280\Omega$	2	4.5	7	

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.

† Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTES:

- A. The pulse generator has the following characteristics: $V_{in(1)} = 3V$, $V_{in(0)} = 0V$, $t_1 = t_0 = 2.5\text{ns}$, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\Omega$.
- B. Inputs not under test are at 2.7V.
- C. C_L includes probe and jig capacitance.