

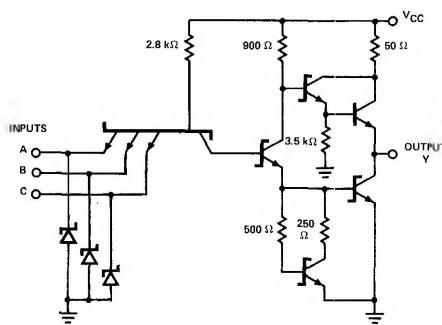
signeticsTRIPLE 3-INPUT
POSITIVE NAND GATE

S54S10

N74S10

DIGITAL 54/74 TTL SERIES

SCHEMATIC DIAGRAM



Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

			S54S10			S74S10			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}			4.5	5	6.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level				20			20	
	Low logic level				10			10	
Operating free-air, T _A			-55		125	0		70	°C

DIGITAL 54/74 TTL, ■ N54S10, S74S10

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V _{IH} High-level input voltage				2			V
V _{IL} Low-level input voltage						0.8	V
V _I Input Clamp Voltage	V _{CC} = MIN, I _I = -18 mA					-1.2	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -1 mA			2.5	3.4		V
				Series 54S	2.7	3.4	V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 20 mA					0.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V					1	mA
I _{IH} High-level input current (each input)	V _{CC} = MAX, V _I = 2.7 V					50	μA
I _{IL} Low-level input current (each input)	V _{CC} = MAX, V _I = 0.5 V					-2	mA
I _{OS} Short-circuit output current‡	V _{CC} = MAX			-40		-100	mA
I _{CCH} Supply current, high-level output (average per gate)	V _{CC} = MAX, All inputs at 0 V			2.5	4		mA
I _{CCL} Supply current, low-level output (average per gate)	V _{CC} = MAX, All inputs at 5 V				5	9	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t _{PLH} Propagation delay time, low-to-high-level output	C _L = 15 pF, R _L = 280 Ω	N O T E	2	3	4.5		ns
	C _L = 50 pF, R _L = 280 Ω				4.5		
t _{PHL} Propagation delay time, high-to-low-level output	C _L = 15 pF, R _L = 280 Ω	1	2	3	5		ns
	C _L = 50 pF, R _L = 280 Ω				5		

NOTE 1: Load circuit and waveforms are shown on page 2-293