

# 8-INPUT DATA | \$54\$151 SELECTORS/MULTIPLEXERS

\$54\$251 N74S151 N74S251

## DIGITAL 54/74 TTL SERIES

#### DESCRIPTION

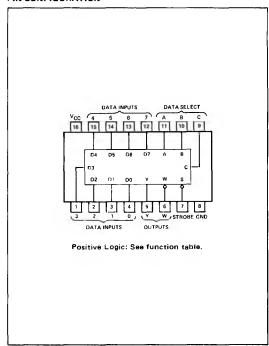
The S54S151, S54S251, N74S151, and N74S251 Schottkyclamped, high-performance, eight-input data selectors/multiplexers are designed for use in very high-speed data routing applications. These multiplexers select one of eight data sources when so directed by the binary address inputs, Both true and complementary data are presented when the strobe input goes low.

The S54S151 and N74S151 are functionally and mechanically interchangeable with the S54151 and N74151 respectively, and in most TTL systems can be utilized to upgrade the performance of existing designs as delay times are typically half that of the S54151 or N74151.

The S54S251 and N74S251 have three-state outputs which permit the outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output can neither drive nor load the bus. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

Typical power dissipation is 225 milliwatts for the S54S151 or N74S151 and 275 milliwatts for the S54S251 and N74S251, or approximately 14 and 17 milliwatts respectively per equivalent gate. The S54S151 and S54S251 are characterized for operation over the full military temperature range of -55°C to 125°C; the N74S151 and N74S251 are characterized for operation from 0°C to 70°C.

#### PIN CONFIGURATION



#### **FEATURES**

- S54S151/N74S151 INTERCHANGEABLE WITH **\$54151/N74151 IN MOST SYSTEMS**
- SCHOTTKY CLAMPED FOR SIGNIFICANT REDUCTION IN DELAY TIMES...4.5 ns TYPICAL, DATA INPUT TO W OUTPUT
- . HIGH-SPEED SELECTION FOR ONE OF EIGHT DATA SOURCES
- PERMITS MULTIPLEXING FROM N LINES TO ONE LINE
- S54S251 AND N74S251 HAVE TRI-STATE OUTPUTS
- FULLY COMPATIBLE WITH SERIES 54/74 AND OTHER **TTL MSI CIRCUITS**

## RECOMMENDED OPERATING CONDITIONS

		S54S15	1	S54S251			N74S151			N74S251			UNIT
	MIN	NOM	MAX	MIN N	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
Normalized fan-out from each output, N (at a low logic level)			10			10			10			10	
High-level output current, OH			-1			-2			-1			-6.5	mA
Operating free-air temperature, TA	-55		125	-55		125	0		70	0		70	°c

### ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITION	S*		54S15 174S15 TYP**		N	54S25 74S25 TYP**	1	UNIT
VIH	High-level input voltage			2			2			V
VIL	Low-level input voltage					0.8			0.8	٧
V <sub>I</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA				-1.2			-1.2	٧
V <sub>OH</sub>	High-level output voltage		Series 54S Series 74S	2.5	3.4		2.4	3.2		V
VOL	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA				0.5			0.5	v
O(off)	Off-state (high-impedance- state) output current	$V_{CC} = MAX, V_{O} = 2.7 V$ $V_{CC} = MAX, V_{O} = 0.4 V$							50 -50	μА
Ч	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V				1			1	mA
ΉΗ	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V				50			50	μА
ILL	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V				-2			-2	mA
Ios	Short-circuit output current‡	V <sub>CC</sub> = MAX		-40		-100	-40		-100	mA
Icc	Supply current	V <sub>CC</sub> = MAX, All inputs at 4. All outputs open	5 V,		45	70		55	85	mA

<sup>\*</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\*All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

‡Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

### SWITCHING CHARACTERISTICS, VCC = 5 V, TA = 25°C

	FROM	то	TEST	S545	S151, N74	S151	S549	S251, N74	IS251	= 05
PARAMETER	(INPUT)	(OUTPUT)	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
tPLH	A, B, or C	Y			12	18		12	18_	ns
tPHL	(4 levels)				12	18		13	19.5	115
tPLH	A, B, or C	w			10	15		10	15	
tPHL	(3 levels)	VV			9	13.5		9	13.5	ns
tPLH	Any D	Υ	0. = 15 n5		8	12		8	12	
tPHL		j •	CL = 15 pF,		8	12		8	12	ns
tPLH	Any D	w	- R <sub>L</sub> = 280 Ω, See Note 1		4.5	7		4.5	7	
tPHL .		**	See Note 1		4.5	7		4.5	7	ns
t <b>P</b> LH	Strobe	Y	1		11	16.5				
t <sub>PHL</sub>		'			12	18				⊓s
tPLH		w	1		9	13				
tPHL	Strobe	"			8.5	12				ns
tZH	Strobe	Y	0 - 50 - 5					13	19.5	
tZL	Strobe	1	CL = 50 pF,					14	21	ns
'tZΗ	Strobe	w	R <sub>L</sub> = 280 Ω, See Note 1		·			13	19.5	
<sup>t</sup> ZL	Strobe	} **	See Note I					14	21	ns
tHZ	Strobe	Υ	C 5 p.5					5.5	8.5	
tLZ	Subbe	'	CL = 5 pF,					9	14	ns
tHZ	Strobe	w	R <sub>L</sub> = 280 Ω, See Note 1					5.5	8.5	
tLZ	Strope	**	See MOLE I					9	14	ns

tpLH = Propatation delay time, low-to-high-level output

t<sub>PHL</sub> ≡ Propagation delay time, high-to-low-level output

tZH = Output enable time to high level

 $t_{ZL}$  = Output enable time to low level

tHZ = Output disable time from high level  $t_{LZ}$  = Output disable time from low level

NOTE 1: See load circuits and waveforms on page 2-293

## DIGITAL 54/74 TTL S54S151, S54S251, N74S151, N74S251

### FUNCTION TABLE

				_	INPUT	s						l	OUTPL	JTS		
:	SELECT	Т	STROBE				DA	TA				S54S151,	N74S151	N74S151 S54S251,		
С	В	Α	s	D0	D1	D2	D3	D4	D5	D6	D7	Y	W	Y	W	
X	Х	Х	Н	х	х	Х	х	х	х	X	Х	L_	Н	Z	Z	
L	L	L	L	L	Х	X	х	х	Х	X	X	L	Н	L	Н	
L	L	L	L	н	X	X	X	Х	X	X	x	н	L	н	L	
L	L	Н	Ł	Х	L	Х	Х	X	X	X	х	L	Н	L	Н	
L	L	Н	L	х	н	х	х	X	X	X	X	н	L	н	L	
L	Н	L	L	×	X	L	х	х	Х	X	х	L	Н	L	Н	
L	Н	L	L	х	х	Н	х	х	X	Х	X	н	L	н	L	
L	Н	Н	Ļ	Х	X	х	L	×	X	X	X	L	Н	L	Н	
L	Н	Н	<b>L</b>	х	х	х	н	X	X	Х	х	н	L	н	L	
Н	L	L	L	Х	х	Х	х	L	Х	х	х	L	Н	L	Н	
н	L	L	L.	х	х	х	Х	Н	Х	Х	х	Н	L	н	L	
Н	L	Н	L	Х	х	X	х	X	L	х	х	L	Н	L	Н	
н	L	н	L	х	х	х	X	X	Н	Х	X	н	L	н	L	
н	Н	L	L	Х	Х	X	X	×	Х	L	X	L	Н	L	Н	
н	Н	L	[	х	Х	х	X	<b>x</b>	Х	н	X	н	L	н	L	
Н	Н	Н	L	Х	х	х	Х	×	х	х	L	L	Н	L	Н	
Н	н	Н	L	Х	×	×	×	×	×	×	Н	н	L	н	L	

H = high logic level, L = low logic level, Z = high impedance, X = irrelevant