DESCRIPTION

These Schottky-clamped high-speed arithmetic/logic units, functionally identical to the S54181 and N74181, perform 16 binary arithmetic operations on two 4-bit words with a full look-ahead carry scheme as propagate and generate terms are available at the P and G outputs. Typical performance is 19 nanoseconds add time for a 16-bit word when used with the S54S182 or N74S182 carry look-ahead.

Typical addition times are shown in Table III. The S54S181/N74S181 can replace the S54181/N74181 in most existing systems for significant performance upgrading as they are functionally and mechanically interchangeable.

The S54S181 and N74S181 will also perform the 16 possible functions on two Boolean variables without the use of external circuitry. The carry circuit is inhibited for logic functions.

The S54S181 and N74S181 will accommodate active-high or active-low data if the pin designations are interpreted as shown below:

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A−B−1 which requires an end-around or forced carry to provide A−B.

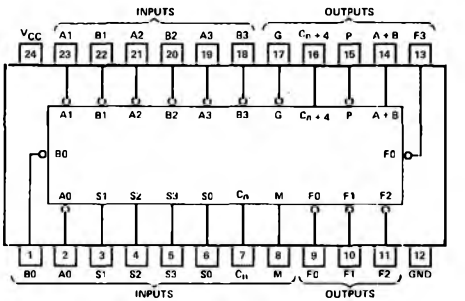
Mode of operation (arithmetic or logic) is controlled by the mode-control (M) input. Complete functions for active-high and active-low data are shown in Tables I and II.

Typical average power dissipation is 600 milliwatts, or approximately 8 milliwatts per equivalent gate. The S54S181 is characterized for operation over the full military temperature range of −55°C to 125°C; the N74S181 is characterized for operation from 0°C to 70°C.

For additional descriptive information and typical connection schemes, see the S54181/N74181 data sheet

PIN CONFIGURATION

J OR N DUAL IN-LINE OR W FLAT PACKAGE
(TOP VIEW)



Logic: See function tables

FEATURES

- SIGNIFICANT IMPROVEMENT IN ADD TIMES OVER S54181/N74181
- TYPICAL ADD TIME FOR 16 BITS OF 19 ns USING S54S182, N74S182 LOOK-AHEAD
- S54S181 IS GUARANTEED FOR OPERATION OVER THE FULL MILITARY TEMPERATURE RANGE OF −55°C TO 125°C
- FULLY COMPATIBLE WITH MOST TTL FUNCTIONS INCLUDING MSI

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-high data (Table I)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y
Active-low data (Table II)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_1$	$\overline{F}_2$	$\overline{F}_3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

TABLE I

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L: ARITHMETIC OPERATIONS	
				LOGIC	C_n = 0 = H	C_n = 1 = L
S_3	S_2	S_1	S_0	FUNCTIONS	(no carry)	(with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A plus 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) plus 1
L	L	H	L	$F = \overline{A}B$	$F = A + \overline{B}$	$F = (A + \overline{B})$ plus 1
L	L	H	H	F = 0	F = minus 1 (2's complement)	F = zero
L	H	L	L	$F = \overline{AB}$	$F = A$ plus $A\overline{B}$	$F = A$ plus $A\overline{B}$ plus 1
L	H	L	H	$F = \overline{B}$	$F = (A + B)$ plus $A\overline{B}$	$F = (A + B)$ plus $A\overline{B}$ plus 1
L	H	H	L	$F = A \oplus B$	F = A minus B minus 1	F = A minus B
L	H	H	H	$F = A\overline{B}$	$F = A\overline{B}$ minus 1	$F = A\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A plus AB	F = A plus AB plus 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A plus B	F = A plus B plus 1
H	L	H	L	F = B	$F = (A + \overline{B})$ plus AB	$F = (A + \overline{B})$ plus AB plus 1
H	L	H	H	F = AB	F = AB minus 1	F = AB
H	H	L	L	F = 1	F = A plus A*	F = A plus A plus 1
H	H	L	H	$F = A + \overline{B}$	F = (A + B) plus A	F = (A + B) plus A plus 1
H	H	H	L	F = A + B	$F = (A + \overline{B})$ plus A	$F = (A + \overline{B})$ plus A plus 1
H	H	H	H	F = A	F = A minus 1	F = A

*Each bit is shifted to the next more significant position.

TABLE II

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L: ARITHMETIC OPERATIONS	
				LOGIC	C_n = 0 = L	C_n = 1 = H
S_3	S_2	S_1	S_0	FUNCTIONS	(no carry)	(with carry)
L	L	L	L	$F = \overline{A}$	F = A minus 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB minus 1	F = AB
L	L	H	L	$F = \overline{A} + B$	$F = A\overline{B}$ minus 1	$F = A\overline{B}$
L	L	H	H	F = 1	F = minus 1 (2's complement)	F = zero
L	H	L	L	$F = \overline{A + B}$	$F = A$ plus $(A + \overline{B})$	$F = A$ plus $(A + \overline{B})$ plus 1
L	H	L	H	$F = \overline{B}$	$F = AB$ plus $(A + \overline{B})$	$F = AB$ plus $(A + \overline{B})$ plus 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A minus B minus 1	F = A minus B
L	H	H	H	$F = A + \overline{B}$	$F = A + \overline{B}$	$F = (A + \overline{B})$ plus 1
H	L	L	L	$F = \overline{A}B$	F = A plus (A + B)	F = A plus (A + B) plus 1
H	L	L	H	$F = A \oplus B$	F = A plus B	F = A plus B plus 1
H	L	H	L	F = B	$F = A\overline{B}$ plus (A + B)	$F = A\overline{B}$ plus (A + B) plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) plus 1
H	H	L	L	F = 0	F = A plus A*	F = A plus A plus 1
H	H	L	H	$F = A\overline{B}$	F = AB plus A	F = AB plus A plus 1
H	H	H	L	F = AB	$F = A\overline{B}$ plus A	$F = A\overline{B}$ plus A plus 1
H	H	H	H	F = A	F = A	F = A plus 1

*Each bit is shifted to the next more significant position.

RECOMMENDED OPERATING CONDITIONS

		S54S181			N74S181			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER			TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage, any output except A = B		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	N54S181	2.5	3.4		V
				S74S181	2.7	3.4		
I_{OH}	High-level output current, A = B output only		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V				250	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	mode input	V_{CC} = MAX, V_I = 2.4 V				50	μA
		any A or B input					150	
		any S input					200	
		carry input					250	
I_{IL}	Low-level input current	mode input	V_{CC} = MAX, V_I = 0.4 V				−2	mA
		any A or B input					−6	
		any S input					−8	
		carry input					−10	
I_{OS}	Short-circuit output current, any output except A = B		V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, T_A = 125°C See Note 1	N54S181 N pkg only			135	mA
			V_{CC} = MAX, See Note 1	N54S181		120	160	
				S74S181		120	220	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡Not more than one output should be shorted at a time.

NOTE 1: I_{CC} is measured for the following conditions:

a. S_0 through S_3, M, and A inputs are at 4.5 V, all other inputs are grounded, and all outputs are open.

b. S_0 through S_3 and M are at 4.5 V, all other inputs are grounded, and all outputs are open.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10 (C_L = 15 pF, R_L = 280 Ω see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}			7	10.5	ns
t_{PHL}					7	10.5	
t_{PLH}	Any A or B	C_{n+4}	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode)		12.5	18.5	ns
t_{PHL}					12.5	18.5	
t_{PLH}	Any A or B	C_{n+4}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		15.5	23	ns
t_{PHL}					15.5	23	
t_{PLH}	C_n	Any F	M = 0 V (SUM or DIFF mode)		7	12	ns
t_{PHL}					7	12	
t_{PLH}	Any A or B	G	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM Mode)		8	12	ns
t_{PHL}					7.5	12	
t_{PLH}	Any A or B	G	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		10.5	16	ns
t_{PHL}					10.5	15	
t_{PLH}	Any A or B	P	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode)		7.5	12	ns
t_{PHL}					7.5	12	
t_{PLH}	Any A or B	P	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		10.5	15	ns
t_{PHL}					10.5	15	
t_{PLH}	Any A or B	Any F	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode)		11	16.5	ns
t_{PHL}					11	16.5	
t_{PLH}	Any A or B	Any F	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		14	20	ns
t_{PHL}					14	22	
t_{PLH}	Any A or B	Any F	M = 4.5 V (logic mode)		14	20	ns
t_{PHL}					14	22	
t_{PLH}	Any A or B	A = B	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		15	23	ns
t_{PHL}					20	30	

¶ t_{PLH} = propagation delay time, low to high-level output

t_{PHL} = propagation delay time, low to high-level output

NOTE 2: Load circuits and waveforms are shown on p. 2-293.

Typical addition times for various configurations are given in the table below. Subtraction times are typically 3 nanoseconds longer than summation times. For typical look-ahead configurations, see the S54181/N74181 data sheet in this catalog.

TABLE III
TYPICAL ADDITION TIMES

NUMBER OF BITS	ADDITION TIMES USING S54S181 AND S64S182	ADDITION TIMES USING S54S181 AND S64182	ADDITION TIMES USING S64181 AND S54182	PACKAGE COUNT ARITHMETIC/ LOGIC UNITS	PACKAGE COUNT LOOK AHEAD CARRY GENERATORS	CARRY METHOD BETWEEN ALU's
1 to 4	11 ns	11 ns	24 ns	1		NONE
5 to 8	18 ns	18 ns	36 ns	2		RIPPLE
9 to 16	19 ns	24 ns	36 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	28 ns	45 ns	60 ns	5 to 16	2 to 5	FULL LOOK AHEAD