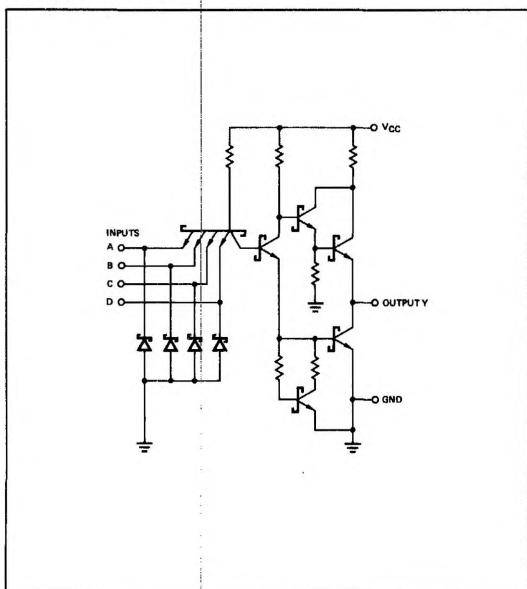


S54S40-A,F,W • S54S140-A,F,W • N74S40-A,F • N74S140-A,F

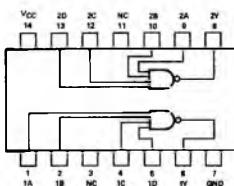
DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)



PIN CONFIGURATIONS

A,F PACKAGE



RECOMMENDED MAXIMUM FAN-OUT FROM EACH OUTPUT

Loads at a high logic level

60

Load at a low logic level

30

NC — No internal connection

ELECTRICAL CHARACTERISTICS (over operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
V_{IH} V_{IL} V_I	High-level input voltage Low-level input voltage Input clamp voltage	2		0.8	V
	$V_{CC} = \text{MIN}$, $I_I = -18\text{mA}$			-1.2	V
V_{OH}	High-level output voltage	2.5	3.4		V
	$V_{CC} = \text{MIN}$, $I_{OH} = -3\text{mA}$	2.7	3.4		V
V_{OL}	Low-level output voltage	2			V
	$V_{CC} = \text{MIN}$, $I_{OL} = 60\text{mA}$			0.5	V
I_I	Input current at maximum input voltage			1	mA
I_{IH}	High-level input current (each input)			100	μA
I_{IL}	Low-level input current (each input)			-4	mA
I_{OS}	Short-circuit output current†			-225	mA
I_{CCH}	Supply current, high-level output (average per gate)			5	mA
I_{CCL}	Supply current, low-level output (average per gate)			22	mA

DIGITAL 54/74 TTL SERIES ■ S54S40, N74S40, S54S140, N74S140

SWITCHING CHARACTERISTICS, $V_{CC} = 5V$, $T_A = 25^\circ C$, $N = 30$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	$C_L = 50\text{pF}, R_L = 93\Omega$ $C_L = 150\text{pF}, R_L = 93\Omega$	NOTE 1	2	4	6.5
t_{PHL}	$C_L = 50\text{pF}, R_L = 93\Omega$ $C_L = 150\text{pF}, R_L = 93\Omega$		2	4	6.5

- * For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable series on the second page of this section.
- All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
- † Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed 100 milliseconds.

NOTE 1: Load circuit and waveforms are shown on page 2-293