Signetics

NE/SA/SE5105/A
Precision High-Speed Comparator With Latch

Product Specification

Linear Products

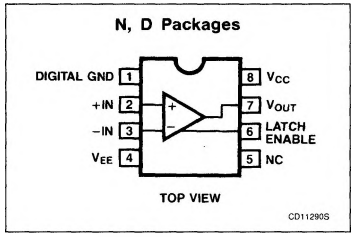
DESCRIPTION

The NE/SA/SE5105/A is a precision high-speed comparator ideally suited for applications requiring ultra-precision and speed. A typical application may be in a 12-bit successive approximation A/D converter. Input offset voltage is factory trimmed to typically 100μV (0.04 LSB for a 12-bit, 10V system); the 36ns response time (measured at 1.2mV overdrive), low input offset current, and high gain remain essentially constant over the entire operating temperature range. Thus, the same degree of precision and speed can be maintained over the specified temperature range. A latch function incorporated with the comparator allows added flexibility to the system designer. A TTL high input at the latch enable pin forces the output of the comparator to stay at its existing logical state irrespective of subsequent signal transitions at the input.

FEATURES

- **Precision input stage:**
  Input offset voltage 100μV
  Input offset current 3nA
- **Fast response time:**
  5mV overdrive 32ns
  1.2mV overdrive 36ns
- **High voltage gain 26,000V/V**
- **Low power dissipation 100mW**
- **TTL output capable of driving 10 TTL gates**
- **Latch function with TTL compatible input**

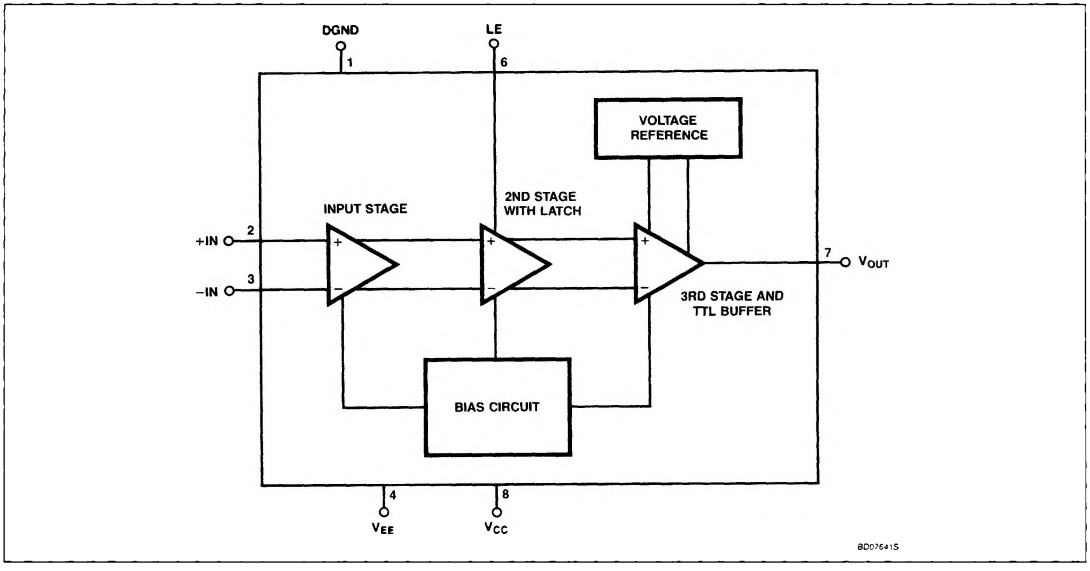
PIN CONFIGURATION



APPLICATIONS

- **High-speed, high-resolution successive approximation A/D converters**
- **Precision zero-crossing detectors**
- **Precision latching window comparators**
- **Fast latching ECL-to-TTL line translators**
- **Precision signal regenerators**

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5105AN
8-Pin Plastic DIP	0 to +70°C	NE5105N
8-Pin Plastic DIP	-40°C to +85°C	SA5105AN
8-Pin Plastic DIP	-40°C to +85°C	SA5105N
8-Pin Plastic SO	0 to +70°C	NE5105AD
8-Pin Plastic SO	0 to +70°C	NE5105D
8-Pin Plastic SO	-40°C to +85°C	SA5105AD
8-Pin Plastic SO	-40°C to +85°C	SA5105D
8-Pin Plastic DIP	-55°C to +125°C	SE5105AN
8-Pin Plastic DIP	-55°C to +125°C	SE5105N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	+6	V
V_{EE}	Power supply	-18	V
$P_{D\ MAX}$	Maximum power dissipation, T_A = 25°C (still-air)[1]		
	FE package	885	mW
	N package	1160	mW
	D package	780	mW
	Differential input voltage	±5	V
	LATCH ENABLE input voltage	V_{CC} to V_{EE}	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating temperature range		
	SE5105 (FE package)	-55 to +125	°C
	SA5105 (N and D package)	-40 to +85	°C
	NE5105 (N and D package)	0 to +70	°C
I_{SC}	Output short-circuit duration		
	To ground	Indefinite	
	To V_{CC}	1	Minute

NOTE:
1. Derate above 25°C, at the following rates:
   FE package at 6.75mW/°C.
   N package at 9.3mW/°C.
   D package at 6.2mW/°C.

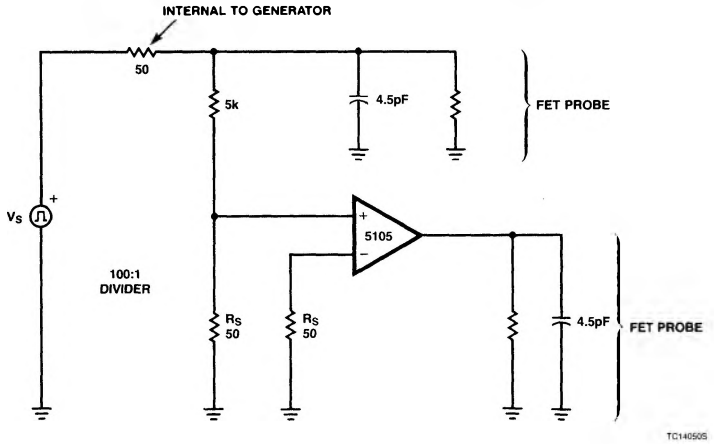
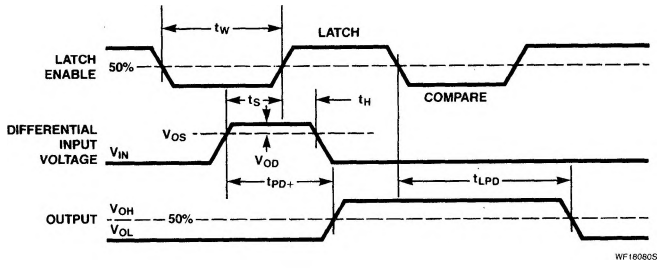


Figure 1. Test Setup for Delay Measurement

TIMING DIAGRAMS



SYMBOL	PARAMETER	CONDITIONS	MINIMUM LIMIT	UNIT
t_S	Setup time	V_{IN} = 100mV	28	ns
t_H	Hold time	V_{OD} = 5mV	10	
t_W	Latch pulse width		20	

DC ELECTRICAL CHARACTERISTICS $V_{CC} = +5V$, $V_{EE} = -5V$, $T_A = 25°C$; $V_{+IN} = V_{-IN} = 0V$ and Latch Enable grounded, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	5105A			5105			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S = 25\Omega$, $V_{CM} = 0V$ $R_S = 25\Omega$, $V_{CM} = \pm 3V$		100 140	250 400			600 750	μV
I_{OS}	Input offset current	$V_{LATCH} = V_{CC}$		3	20			40	nA
I_B	Input bias current	$V_{LATCH} = V_{CC}$		400	1200			1400	nA
A_{VO}	Voltage gain[1]		18	26		18	26		V/mV
CMVR	Input voltage range		±3	±3.3		±3	±3.3		V
CMRR	Common mode rejection ratio	$V_{CM} = \pm 3V$	86	99		84			dB
PSRR	Power supply rejection ratio	$V_{CC}/V_{EE} = \pm 4.5V$ to $\pm 5.5V$ $V_{CC} = +5V$ and $V_{EE} = -4.5V$ to $-15V$	78 86	94 104		78 84			dB dB
V_{OH}	Output high voltage	$V_{IN} \geq 10mV$, $I_{OH} = 0\mu A$ $V_{IN} \geq 10mV$, $I_{OH} = 400\mu A$	2.4 2.4	2.8 2.6		2.4 2.4	2.8 2.6		V V
V_{OL}	Output low voltage	$V_{IN} \leq 10mV$, $I_{OL} = 0\mu A$ $V_{IN} \leq 10mV$, $I_{OL} = 16mA$		0.2 0.3	0.4 0.4		0.2 0.3	0.4 0.4	V V
I_{CC}	Positive supply current	$V_O \leq 0.4V$, $I_O = 0\mu A$		11	14			16	mA
I_{EE}	Negative supply current	$V_O \leq 0.4V$, $I_O = 0\mu A$		9	12			14	mA
P_D	Power dissipation			100	130			150	mW
V_{LH}	Logic 1 at latch input		2			2			V
V_{LL}	Logic 0 at latch input				0.8			0.8	V
	Latch input current								
I_{LH}	Logic 1	$V_{LATCH} = 3V$		4	20		4	20	μA
I_{LL}	Logic 0	$V_{LATCH} = 0.8V$		1	5		1	5	μA
R_{IN}	Differential input resistance			1000			1000		MΩ

NOTE:
1. Guaranteed by design.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V, V_{EE} = −5V; −55°C ≤ T_A ≤ +125°C for SE5105A/5105; −40°C ≤ T_A ≤ +85°C for SA5105A/5105; and, 0°C ≤ T_A ≤ +70°C for NE5105A/5105. V_{+IN} = V_{-IN} = 0V and Latch Enable grounded, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	5105A			5105			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	R_S = 25Ω, V_{CM} = 0V R_S = 25Ω, V_{CM} = ±3V		0.25 0.3	0.6 0.75			1 1.2	mV
TC V_{OS}	Input offset voltage drift	V_{CM} = 0V		1.5	7.5			10	µV/°C
I_{OS}	Input offset current	V_{LATCH} = V_{CC}		4	25			60	nA
I_B	Input bias current	V_{LATCH} = V_{CC}		0.5	1.5			1.8	µA
A_{VO}	Voltage gain[1]		16	23		16	23		V/mV
CMVR	Input voltage range		±3	±3.2		±3	±3.2		V
CMRR	Common mode rejection ratio	V_{CM} = ±3V	83	93		80			dB
PSRR	Power supply rejection ratio	V_{CC}/V_{EE} = ±4.5V to ±5.5V V_{CC} = +5V and V_{EE} = −4.5V to −15V	75 75	94 94		72 72			dB dB
V_{OH}	Output high voltage	V_{IN} ≥ 10mV, I_{OH} = 0µA V_{IN} ≥ 10mV, I_{OH} = 320µA	2.4 2.4			2.4 2.4			V V
V_{OL}	Output low voltage[2]	V_{IN} ≤ 10mV, I_{OL} = 9.6mA V_{IN} ≤ 10mV, I_{OL} = 12.8mA		0.28 0.35	0.4 0.45		0.28 0.35	0.4 0.45	V V
I_{CC}	Positive supply current	V_O < 0.4V, I_O = 0µA		15	19			22	mA
I_{EE}	Negative supply current	V_O ≤ 0.4V, I_O = 0µA		12	17			20	mA
P_D	Power dissipation			135	180			210	mW
V_{LH}	Logic 1 at latch input		2			2			V
V_{LL}	Logic 0 at latch input				0.8			0.8	V
I_{LH} I_{LL}	Latch input current Logic 1 Logic 0	V_{LATCH} = 3V V_{LATCH} = 0.8V		6 1	20 10		6 1	20 10	µA µA
R_{IN}	Differential input resistance			1000			1000		MΩ

NOTES:
1. Guaranteed by design.
2. V_{OL} = 0.45V max at T_A ≤ −40°C and I_{OL} = 12.8mA.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V; V_{EE} = −5V; T_A = 25°C and Latch Enable grounded, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	5105A/5105			UNIT
			Min	Typ	Max	
t_{PD+}	Input to output high propagation delay[1, 2]	V_{OD} = 1.2mV V_{OD} = 5mV		36 32	 50	ns ns
t_{PD-}	Input to output low propagation delay[1, 2]	V_{OD} = 1.2mV V_{OD} = 5mV		34 32	 50	ns ns
t_{LPD}	Latch disable time[1, 2]			25	38	ns

NOTES:
1. Guaranteed by design.
2. Times are for 100mV step inputs. See Timing Diagrams, Figures 3 and 4.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V; V_{EE} = -5V; -55°C ≤ T_A ≤ +125°C for SE5105A/5105; -40°C ≤ T_A ≤ +85°C for SA5105/5105A, and, 0°C ≤ T_A ≤ +70°C for NE5105A/5105 Latch Enable grounded, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	5105A/5105			UNIT
			Min	Typ	Max	
t_{PD+}	Input to output high propagation delay[1, 2]	V_{OD} = 1.2mV V_{OD} = 5mV		50 45		ns ns
t_{PD-}	Input to output low propagation delay[1, 2]	V_{OD} = 1.2mV V_{OD} = 5mV		43 40		ns ns
t_{LPD}	Latch disable time[1, 2]			34		ns

NOTES:
1. Guaranteed by design.
2. Times are for 100mV step inputs. See Timing Diagrams, Figures 3 and 4.

SYMBOLS AND DEFINITIONS

Common-Mode Rejection Ratio (CMRR)
The ratio of the change in common-mode voltage to the corresponding change in V_{OS}. CMRR is expressed in dB, CMRR = 20 log ($\Delta CMV/\Delta V_{OS}$).

Differential Input Resistance (R_{IN})
Resistance looking into either input terminal with the other referred to a specified voltage.

Input Bias Current (I_{BIAS})
The current into either input terminal with both inputs referred to a specified voltage.

Input Offset Current (I_{OS})
The difference between the two input bias currents with both inputs referred to a specified voltage

Input Offset Voltage (V_{OS})
The minimum potential difference required between the input terminals to force the output to a specified voltage.

Input Offset Voltage Drift (TCV_{OS})
The ratio of the change in V_{OS} to the change in temperature as that temperature deviates from a +25°C ambient.

Input to Output Propagation Delay (t_{PD+} and t_{PD-})
The propagation delay measured from the time the input signal crosses V_{OS} to the 50% transition point of the output signal. Delay is measured with a specified input step size (V_{IN}) and overdrive (V_{OD}).

Input Voltage Range (CMVR)
The range of common-mode voltage at the input for which operation within specifications is guaranteed.

Latch Disable Propagation Delay (t_{LPD})
The propagation delay measured between the 50% transition points of the LATCH ENABLE signal falling edge and the output signal transition point.

Latch Hold Time (t_H)
The minimum time after the positive transition of the LATCH ENABLE signal that the input signal must remain unchanged in order to be acquired and held at the output. Hold time is measured from the 50% transition point of the LATCH ENABLE signal to the point where comparator input signal crosses V_{OS}.

Latch Pulse Width (t_W)
The minimum time that the LATCH ENABLE signal must be low in order to acquire and subsequently hold the input signal change. Pulse width is measured between the 50% transition points of the falling and rising edges of the latch pulse.

Latch Setup Time (t_S)
The minimum time before the positive transition of the LATCH ENABLE signal that an input signal change must be present in order to be acquired and held at the output. Setup time is measured from the point the input signal crosses V_{OS} to the 50% transition point of the LATCH ENABLE signal.

Output High Current (I_{OH})
The current that the comparator output can source at a specified output voltage and input overdrive.

Output High Voltage (V_{OH})
The high output voltage with a specified source current and input overdrive.

Output Low Voltage (V_{OL})
The low output voltage with a specified sink current and input overdrive.

Output Sink Current (I_{OL})
The current that the comparator output can sink at a specified output voltage and input overdrive.

Overdrive (V_{OD})
The applied input differential voltage in excess of input offset voltage (V_{OS}).

Power Supply Rejection Ratio (PSRR)
The ratio of the change in input offset voltage to the specified change in power supply voltage.

Voltage Gain (A_V)
The ratio of the change in output voltage (over a specified range) to the change in differential input voltage.

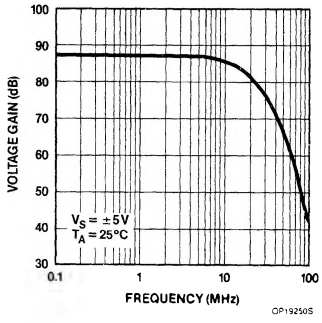
APPLYING THE NE/SA/SE5105/A

PC Board Layout

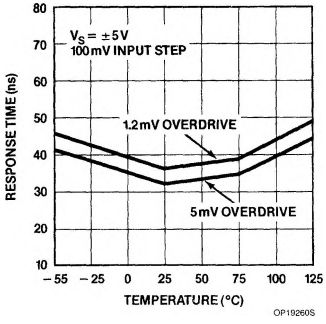
As with any high-speed circuit, layout of the PC board becomes critical for optimum performance. The supplies should be bypassed with good high frequency capacitors mounted as close to the IC as possible. A combination of high frequency ceramic and tantalum capacitors provide adequate suppression of transients on the supply lines. Since the comparator is an uncompensated amplifier with high gain, even a small amount of feedback from the output to the input can cause oscillation. A poor layout of the PC board not only increases the uncertainty region (due to oscillation) of the comparator, but also introduces hysteresis. Use of ground planes is essential since ground planes not only minimize inductance, but also reduce stray feedback capacitances by referring them to ground. Separate analog and digital ground planes should be used; the inputs are referred to the analog ground while the supplies and output are referred to the digital ground (Pin 1). Furthermore, the analog and digital ground planes should only meet at one point. Comparator output and input pins should be isolated from each other along with the traces from the respective pins. Stray capacitance from the IC pins to ground can be minimized by keeping the lead lengths and traces as short as possible.

TYPICAL PERFORMANCE CHARACTERISTICS

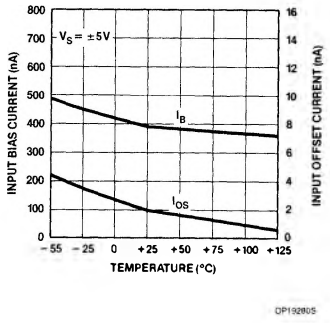
Voltage Gain vs Frequency



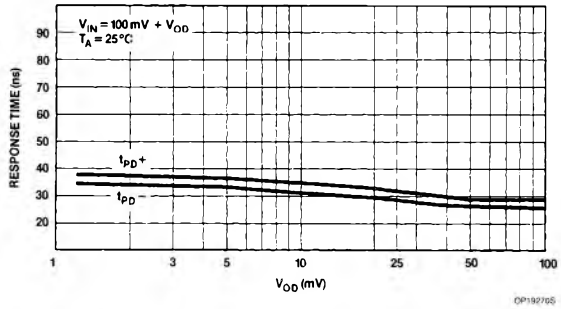
Response Time vs Temperature



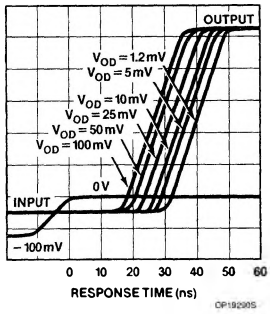
Input Current vs Temperature



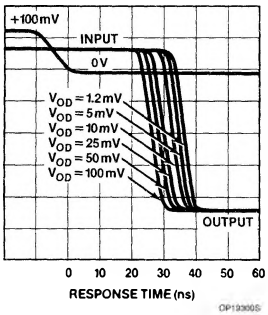
Response Time vs Overdrive Voltage



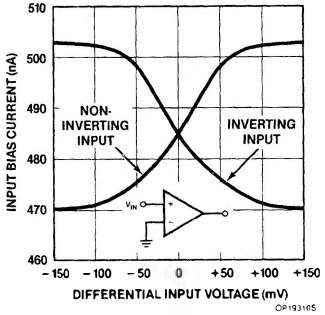
$t_{PD}+$ Response Time



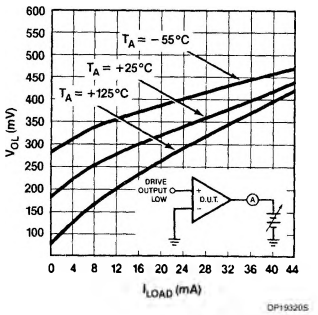
$t_{PD}-$ Response Time



Input Bias Current vs Differential Input Voltage

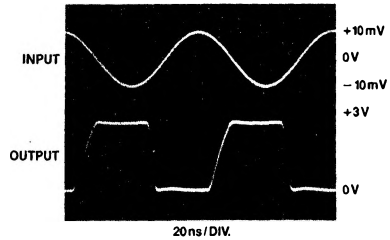


V_{SAT} vs Load Current

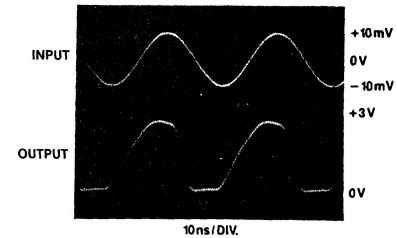


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Response to 10MHz Sine Wave



Response to 25MHz Sine Wave



Response Time to 5mV and 1.2mV Overdrive