**Signetics**

**Linear Products**

# NE/SA/SE5205
## Wide-band High-Frequency Amplifier

***Product Specification***

## DESCRIPTION

The NE/SA/SE5205 is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ± 0.5dB from DC to 450MHz, and the -3dB bandwidth is greater than 600MHz in the EC package. This performance makes the amplifier ideal for cable TV applications. For lower frequency applications, the part is also available in industrial standard dual in-line and small outline packages. The NE/SA/SE5205 operates with a single supply of 6V, and only draws 24mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high-power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA/SE5205 solves these problems by incorporating a wide-band amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output from DC to the -3dB bandwidth limit.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects. A TO-46 metal can is also available that has a case connection for RF grounding which increases the -3dB frequency to 600MHz. The Cerdip package is hermetically sealed, and can operate over the full -55°C to +125°C range.

No external components are needed other than AC coupling capacitors because the NE/SA/SE5205 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA/SE5205s in series as required, without any degradation in amplifier stability.

## FEATURES

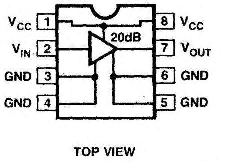
- **600MHz bandwidth**
- **20dB insertion gain**
- **4.8dB (6dB) noise figure $Z_O = 75\Omega$ ($Z_O = 50\Omega$)**
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**
- **Surface mount package available**
- **MIL-STD processing available**

## APPLICATIONS

- **75Ω cable TV decoder boxes**
- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broad-band LANs**
- **Fiber-optics**
- **Modems**
- **Mobile radio**
- **Security systems**
- **Telecommunications**

## PIN CONFIGURATIONS

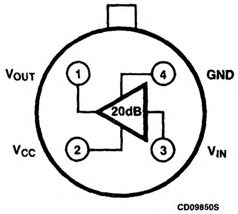
**N, FE, D Packages**



TOP VIEW

CD12760S

**EC Package**



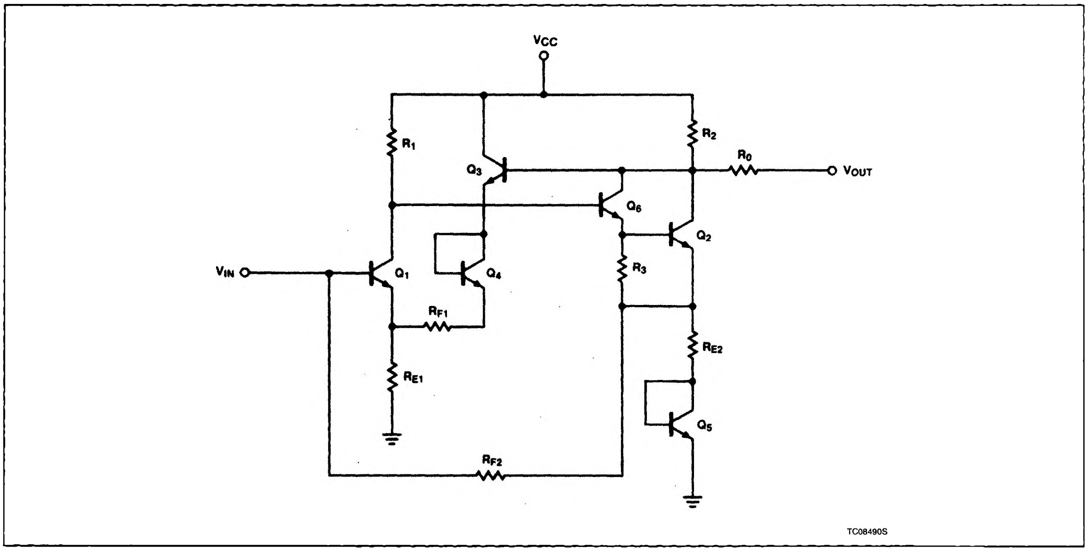
CD09850S

**NOTE:**
Tab denotes Pin 1.

## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 8-Pin Plastic SO | 0 to +70°C | NE5205D |
| 4-Pin Metal can | 0 to +70°C | NE5205EC |
| 8-Pin Cerdip | 0 to +70°C | NE5205FE |
| 8-Pin Plastic DIP | 0 to +70°C | NE5205N |
| 8-Pin Plastic SO | −40°C to +85°C | SA5205D |
| 8-Pin Plastic DIP | −40°C to +85°C | SA5205N |
| 8-Pin Cerdip | −40°C to +85°C | SA5205FE |
| 8-Pin Cerdip | −55°C to +125°C | SE5205FE |
| 8-Pin Plastic DIP | −55°C to +125°C | SE5205N |

## EQUIVALENT SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 9 | V |
| $V_{AC}$ | AC input voltage | 5 | $V_{P-P}$ |
| $T_A$ | Operating ambient temperature range<br>NE grade<br>SA grade<br>SE grade | <br>0 to +70<br>-40 to +85<br>-55 to +125 | <br>°C<br>°C<br>°C |
| $P_{DMAX}$ | Maximum power dissipation, $T_A = 25°C$ (still-air)[1, 2]<br>FE package<br>N package<br>D package<br>EC package | <br>780<br>1160<br>780<br>1250 | <br>mW<br>mW<br>mW<br>mW |

**NOTES:**

1. Derate above 25°C, at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C
   EC package at 10.0mW/°C
2. See "Power Dissipation Considerations" section.

## DC ELECTRICAL CHARACTERISTICS at $V_{CC} = 6V$, $Z_S = Z_L = Z_O = 50\Omega$ and $T_A = 25°C$, in all packages, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | SE5205 |  |  | NE/SA5205 |  |  | UNIT |
|---|---|---|---|---|---|---|---|---|---|
|  |  |  | Min | Typ | Max | Min | Typ | Max |  |
|  | Operating supply voltage range | Over temperature | 5<br>5 |  | 6.5<br>6.5 | 5<br>5 |  | 8<br>8 | V<br>V |
| $I_{CC}$ | Supply current | Over temperature | 20<br>19 | 24 | 30<br>31 | 20<br>19 | 24 | 30<br>31 | mA<br>mA |
| S21 | Insertion gain | f = 100MHz<br>Over temperature | 17<br>16.5 | 19 | 21<br>21.5 | 17<br>16.5 | 19 | 21<br>21.5 | dB |
| S11 | Input return loss | f = 100MHz D, N, FE |  | 25 |  |  | 25 |  | dB |
|  |  | DC - $f_{MAX}$ D, N, FE | 12 |  |  | 12 |  |  | dB |
| S11 | Input return loss | f = 100MHz EC package |  |  |  |  | 24 |  | dB |
|  |  | DC - $f_{MAX}$ EC |  |  |  | 10 |  |  | dB |
| S22 | Output return loss | f = 100MHz D, N, FE |  | 27 |  |  | 27 |  | dB |
|  |  | DC - $f_{MAX}$ | 12 |  |  | 12 |  |  | dB |
| S22 | Output return loss | f = 100MHz EC package |  |  |  |  | 26 |  | dB |
|  |  | DC - $F_{MAX}$ |  |  |  | 10 |  |  | dB |
| S12 | Isolation | f = 100MHz |  | -25 |  |  | -25 |  | dB |
|  |  | DC - $f_{MAX}$ | -18 |  |  | -18 |  |  | dB |
| $t_R$ | Rise time |  |  | 5 |  |  | 5 |  | ps |
|  | Propagation delay |  |  | 5 |  |  | 5 |  | ps |

**DC ELECTRICAL CHARACTERISTICS** at $V_{CC}$ = 6V, $Z_S = Z_L = Z_O$ = 50Ω and $T_A$ = 25°C, in all packages, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | SE5205 | | | NE/SA5205 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| BW | Bandwidth | ±0.5dB D, N | | | | | 450 | | MHz |
| $f_{MAX}$ | Bandwidth | ±0.5dB EC | | | | | 500 | | MHz |
| $f_{MAX}$ | Bandwidth | ±0.5dB FE | | 300 | | | 300 | | MHz |
| $f_{MAX}$ | Bandwidth | −3dB D, N | | | | 550 | | | MHz |
| $f_{MAX}$ | Bandwidth | −3dB EC | | | | 600 | | | MHz |
| $f_{MAX}$ | Bandwidth | −3dB FE | 400 | | | 400 | | | MHz |
| | Noise figure (75Ω) | f = 100MHz | | 4.8 | | | 4.8 | | dB |
| | Noise figure (50Ω) | f = 100MHz | | 6.0 | | | 6.0 | | dB |
| | Saturated output power | f = 100MHz | | +7.0 | | | +7.0 | | dBm |
| | 1dB gain compression | f = 100MHz | | +4.0 | | | +4.0 | | dBm |
| | Third-order intermodulation intercept (output) | f = 100MHz | | +17 | | | +17 | | dBm |
| | Second-order intermodulation intercept (output) | f = 100MHz | | +24 | | | +24 | | dBm |

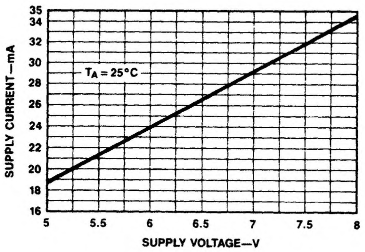


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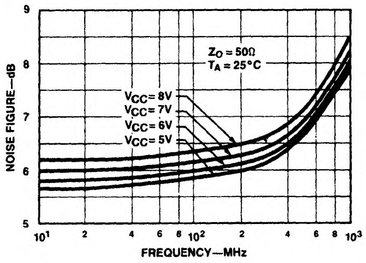
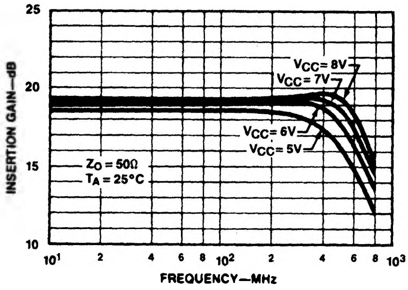
Figure 1. Supply Current vs Supply Voltage



OP04650S

Figure 2. Noise Figure vs Frequency



OP04660S

Figure 3. Insertion Gain vs Frequency ($S_{21}$)

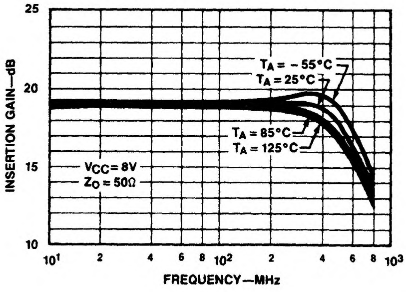


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Figure 4. Insertion Gain vs Frequency ($S_{21}$)

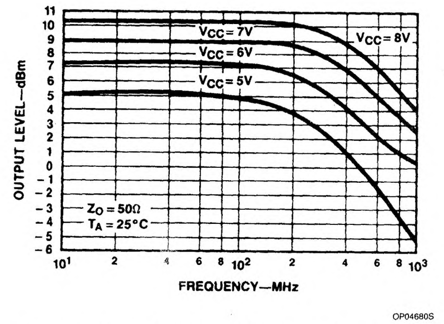

Figure 5. Saturated Output Power vs Frequency

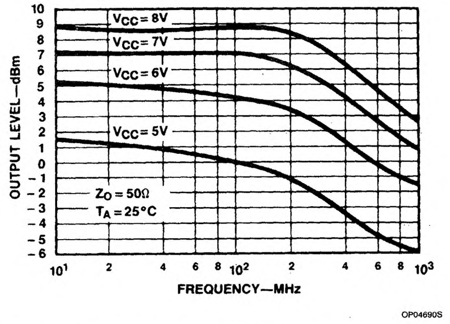

Figure 6. 1dB Gain Compression vs Frequency

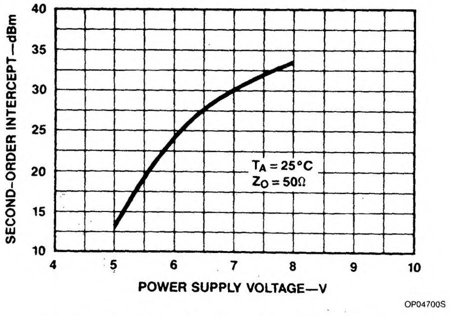

Figure 7. Second-Order Output Intercept vs Supply Voltage

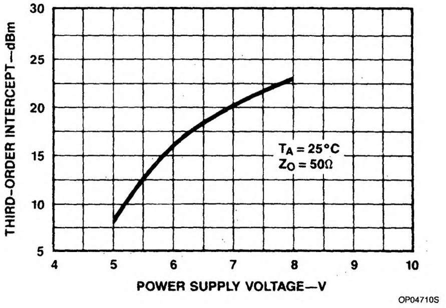

Figure 8. Third-Order Intercept vs Supply Voltage

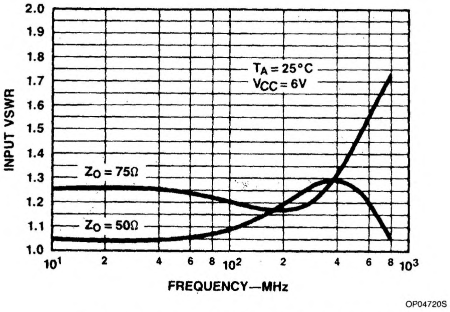

Figure 9. Input VSWR vs Frequency

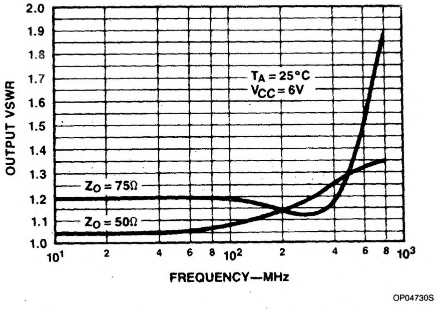

Figure 10. Output VSWR vs Frequency

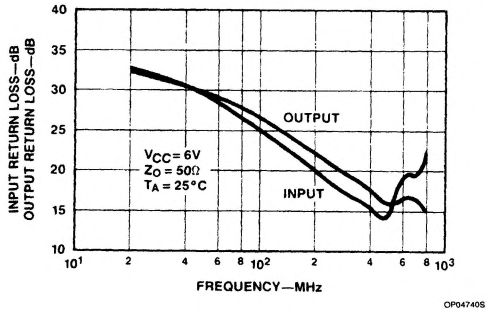

**Figure 11. Input ($S_{11}$) and Output ($S_{22}$) Return Loss vs Frequency**

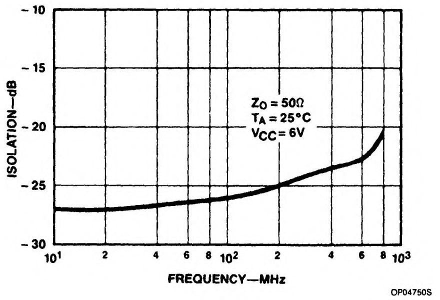

**Figure 12. Isolation vs Frequency ($S_{12}$)**

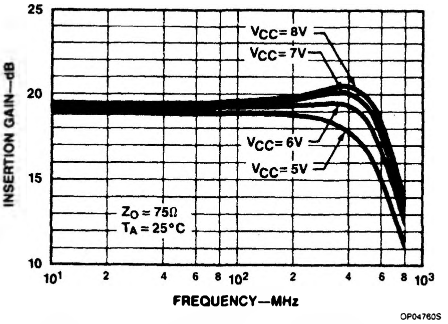

**Figure 13. Insertion Gain vs Frequency ($S_{21}$)**

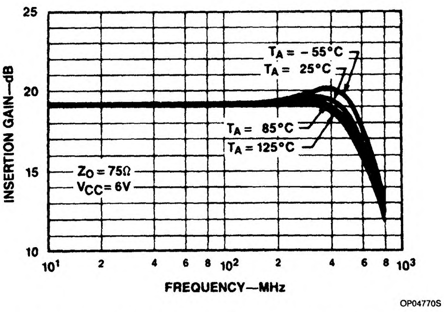

**Figure 14. Insertion Gain vs Frequency ($S_{21}$)**

## THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1})/R_{E1} \qquad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to $R_{F2}$ and $R_{E2}$ which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, $R_{E1}$ and the base resistance of $Q_1$ are kept as low as possible while $R_{F2}$ is maximized.

The noise figure is given by the following equation:

$$NF = 10 \text{ Log} \left\{ 1 + \frac{\left[ r_b + R_{E1} + \frac{KT}{2qI_{C1}} \right]}{R_O} \right\} \text{ dB} \qquad (2)$$

where $I_{C1} = 5.5mA$, $R_{E1} = 12\Omega$, $r_b = 130\Omega$, $KT/q = 26mV$ at 25°C and $R_O = 50$ for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level $V_{IN}$ can be determined by the equation:

$$V_{IN} = V_{BE1} + (I_{C1} + I_{C3})\ R_{E1}$$

where $R_{E1} = 12\Omega$, $V_{BE} = 0.8V$, $I_{C1} = 5mA$ and $I_{C3} = 7mA$ (currents rated at $V_{CC} = 6V$).

Under the above conditions, $V_{IN}$ is approximately equal to 1V.

Level shifting is achieved by emitter-follower $Q_3$ and diode $Q_4$ which provide shunt feedback to the emitter of $Q_1$ via $R_{F1}$. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. The value of $R_{F1} = 140\Omega$ is chosen to give the desired nominal gain. The DC output voltage $V_{OUT}$ can be determined by:

$$V_{OUT} = V_{CC} - (I_{C2} + I_{C6})R2, \qquad (4)$$

where $V_{CC} = 6V$, $R_2 = 225\Omega$, $I_{C2} = 7mA$ and $I_{C6} = 5mA$.

From here it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode $Q_5$ is included for bias purposes to allow direct coupling of $R_{F2}$ to the base of $Q_1$. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair ($Q_6$ and $Q_2$) which increases the DC bias voltage on the input stage ($Q_1$) to a more desirable value, and also increases the feedback loop gain. Resistor $R_O$ optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors $L_1$ and $L_2$ are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

## POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (30mA Max). For operation at supply voltages other than 6V, see Figure 1 for $I_{CC}$ versus $V_{CC}$ curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat sinking benefits can be realized by mounting the D and EC package body against the PC board plane.

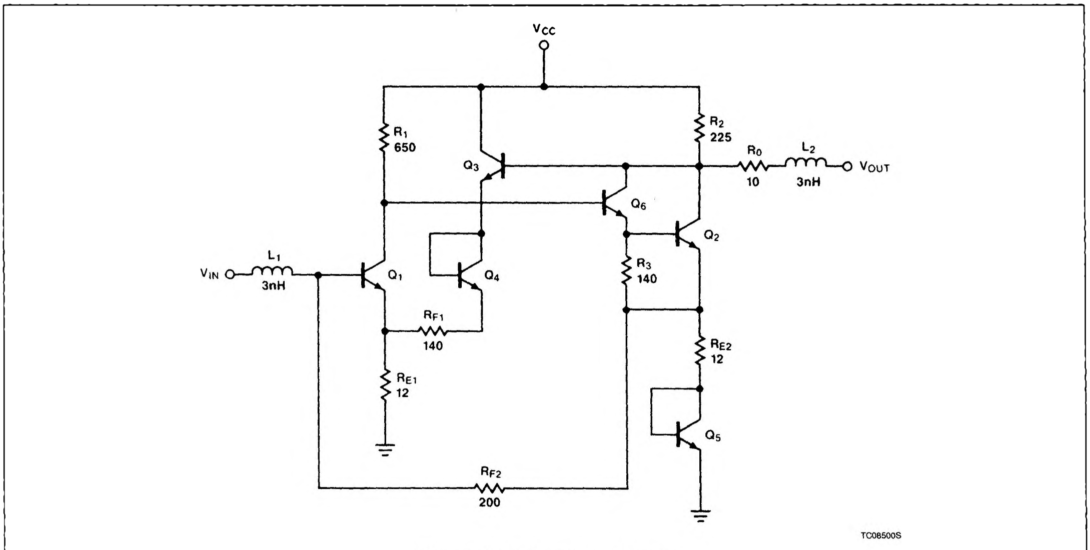

Figure 15. Schematic Diagram

## PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5205 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and $V_{CC}$ pins on the SO package). In addition, if the EC package is used, the case should be soldered to the ground plane. The power supply should be decoupled with a capacitor as close to the $V_{CC}$ pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC coupled. This is because at $V_{CC}$ = 6V, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low impedance system or the DC bias on the output of the amplifier will be loaded down causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

## SCATTERING PARAMETERS

The primary specifications for the NE/SA/SE5205 are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.

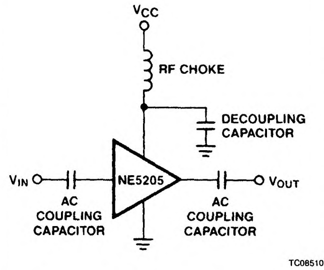

**Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling**

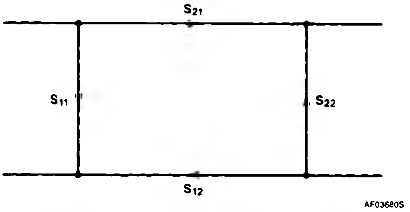

**Figure 17a. Two-Port Network Defined**

$S_{11}$ — INPUT RETURN LOSS

$$S_{11} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

$S_{12}$ — REVERSE TRANSMISSION LOSS OR ISOLATION

$$S_{12} \equiv \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

$S_{21}$ — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} \equiv \sqrt{\text{TRANSDUCER POWER GAIN}}$$

$S_{22}$ — OUTPUT RETURN LOSS

$$S_{22} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

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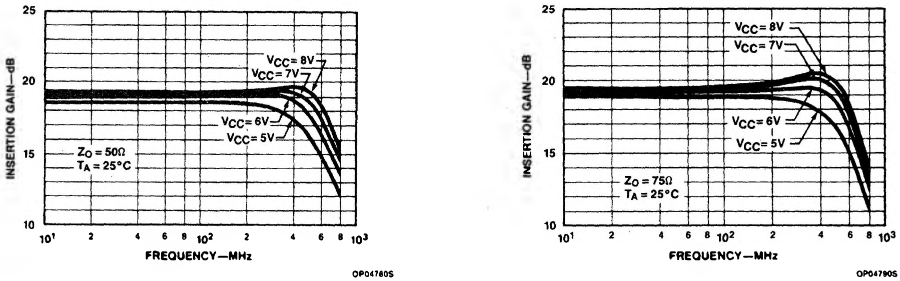
**Figure 17b**

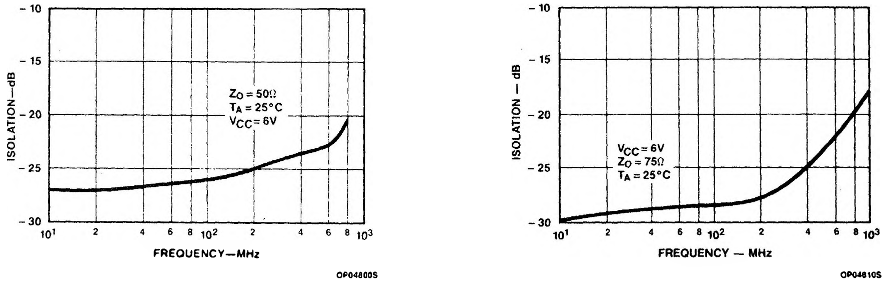
Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 18.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5205 to other high-frequency amplifiers.

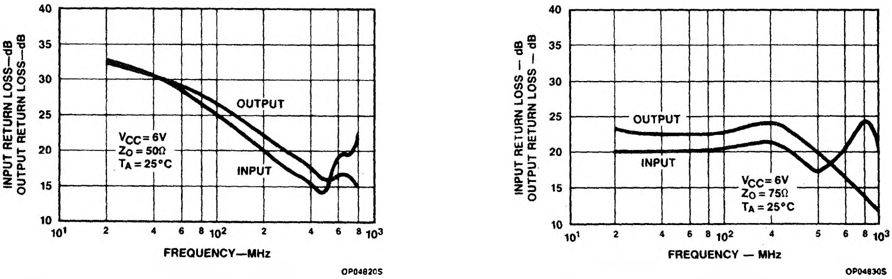
**50Ω System** **75Ω System**



a. Insertion Gain vs Frequency ($S_{21}$) b. Insertion Gain vs Frequency ($S_{21}$)



c. Isolation vs Frequency ($S_{12}$) d. $S_{12}$ Isolation vs Frequency



e. Input ($S_{11}$) and Output ($S_{22}$) Return Loss vs Frequency f. Input ($S_{11}$) and Output ($S_{22}$) Return Loss vs Frequency

Figure 18

## Wide-band High-Frequency Amplifier NE/SA/SE5205

The most important parameter is $S_{21}$. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE/SA/SE5205

$P_{IN} = \frac{V_{IN}^2}{Z_D}$

$P_{OUT} = \frac{V_{OUT}^2}{Z_D}$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$P_I = V_I^2$

$P_I$ = Insertion Power Gain

$V_I$ = Insertion Voltage Gain

Measured value for the NE/SA/SE5205 = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20dB$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20dB$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20dB$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS = $S_{11}$dB
$S_{11}dB = 20 \text{ Log } |S_{11}|$

OUTPUT RETURN LOSS = $S_{22}$dB
$S_{22}dB = 20 \text{ Log } |S_{22}|$

$$\text{INPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leq 1.5$$

$$\text{OUTPUT VSWR} = \frac{|1 + S_{22}|}{|1 - S_{22}|} \leq 1.5$$

### 1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

### INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

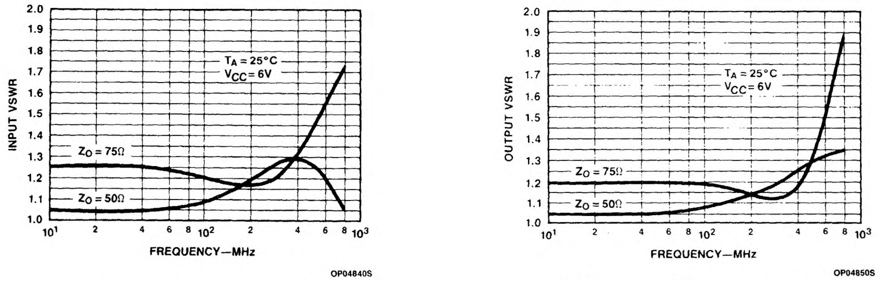
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$IP_2 = P_{OUT} + IMR_2$

$IP_3 = P_{OUT} + IMR_3/2$

where $P_{OUT}$ is the power level in dBm of each of a pair of equal level fundamental output signals, $IP_2$ and $IP_3$ are the second and third order output intercepts in dBm, and $IMR_2$ and $IMR_3$ are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure $IP_2$ and $IP_3$ at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA/SE5205 we have chosen an output level of −10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.



a. Input VSWR vs Frequency

b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

## ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to *High-Frequency Amplifiers* by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

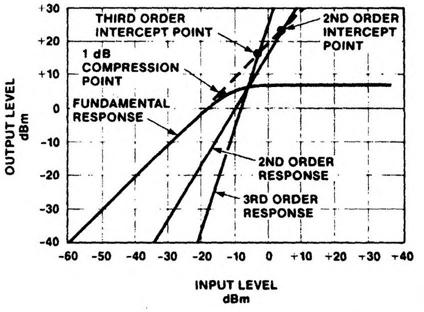


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Figure 20