Signetics

Linear Products

SAA1064

4-Digit LED Driver with I^2C Bus Interface

Objective Specification

DESCRIPTION

The LED driver is a bipolar integrated circuit made in an I^2L compatible 18V process. The circuit is especially designed to drive four 7-segment LED displays with decimal point by means of multiplexing between two pairs of digits. It features an I^2C bus slave transceiver interface with the possibility to program four different slave addresses, a power reset flag, 16 current sink outputs, controllable by software up to 21mA, two multiplex drive outputs for common anode segments, an on-chip multiplex oscillator, control bits to select static, dynamic and blank mode, and one bit for segment test.

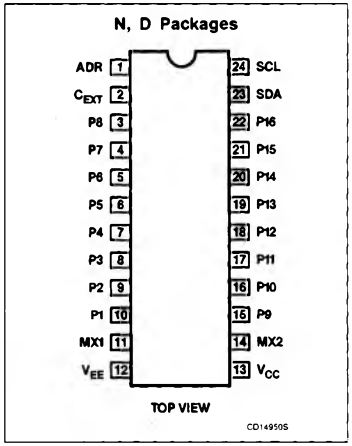
FEATURES

- **Programmable brightness**
- **SO package**
- **May be multiplexed to 16 digits**

APPLICATIONS

- **Digital displays requiring 4, 8, or 16 seven-segment characters**

PIN CONFIGURATION



ORDERING INFORMATION

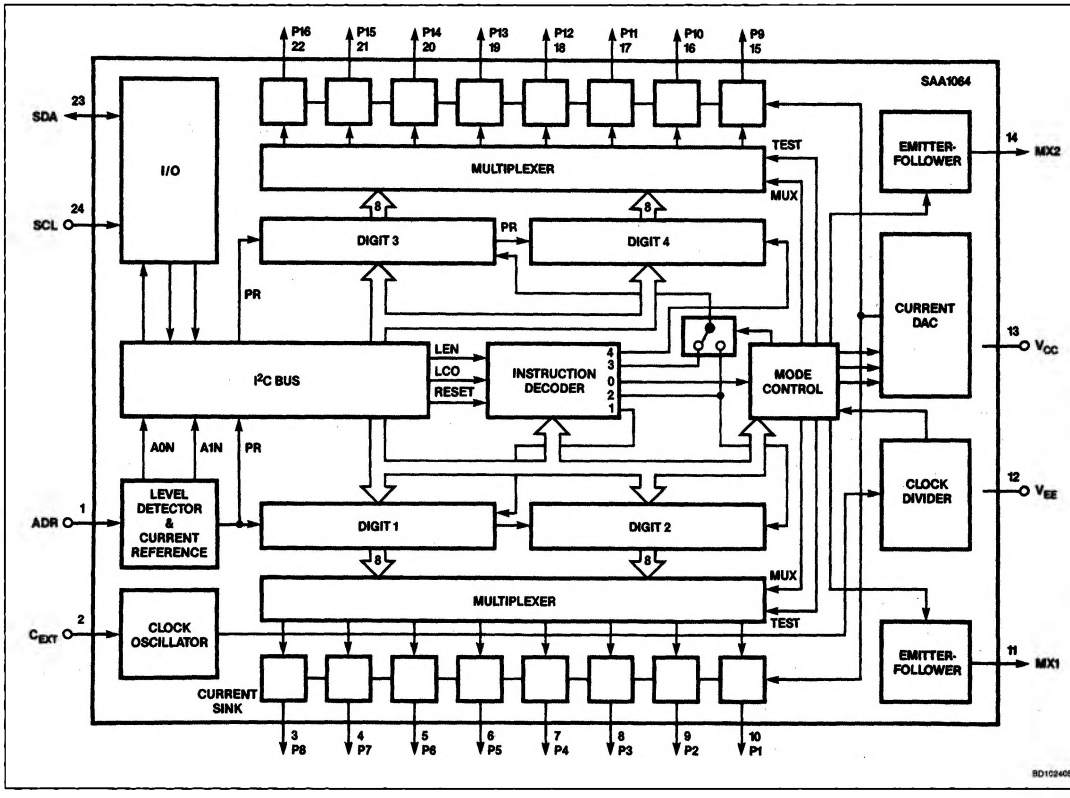
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP (SOT-101BE)	−20°C to +70°C	SAA1064PN
24-Pin Plastic SOL (SO-24, SOT-137BE)	−20°C to +70°C	SAA1064TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (V_{13-12})	−0.5 to 18	V
I_{CC}	Supply current (I_{13})	−50 to 200	mA
	Total power dissipation		
P_D	SOT-101 (24-pin DIP)	1000	mW
P_D	SO-24, SOT-137 (24-pin SOL)	500	mW
$V_{23,\ 24-12}$	SDA, SCL voltages	−0.5 to 5.9	V
$V_{1-11,\ 14-22}$	Voltages A0 − MX1 and MX2 − P16	−0.5 to V_{CC} +0.5	V
	Input/output current all pins		
±1	outputs off	10	mA
T_A	Operating ambient temperature	−20 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C
	Thermal resistance from crystal to ambient		
θ_{CRA}	24-Pin DIP	35	°C/W
	SO-24 on a Ceramic Substrate	115	°C/W
	SO-24 on a Printed Circuit Board	145	°C/W

4-Digit LED Driver with I²C Bus Interface SAA1064

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V, V_{EE} = 0V (ground), T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage (V_{13-12})	4.5	5.0	18.0	V
I_{CC}	Supply current all outputs off		8.6		mA
P_D	Power dissipation all outputs off		43.0		mW
SDA, SCL, Bus (Pins 23 and 24)					
$V_{23,\ 24-12}$	Input voltages	0		5.5	V
$V_{IL(L)}$	Logic input voltage Low			1.5	V
$V_{IL(H)}$	Logic input voltage High	3.0			V
$-I_{IL}$	Input current Low			10.0	μA
$V_{OL(L)}$	SDA logic output Low (Pin 23)			0.4	V
I_O	SDA output sink current (Pin 23)	3.0	5.0		mA
V_{1-12}	Address input voltage (Pin 1)	0		V_{CC}	V
V_{1-12}	Address input voltage (Pin 1) at programmable address bits: A0 = 0, A1 = 0 A0 = 1, A1 = 0 A0 = 0, A1 = 1 A0 = 1, A1 = 1		 V_{EE} $\frac{1}{3}$ V_{CC} $\frac{2}{3}$ V_{CC} V_{CC}		 V V V V
$-I_I$	Address input current Low			10.0	μA
I_I	Address input current High			10.0	μA
C_{EXT} Switch Level (Pin 2)					
V_{IL}	Input voltage Low		$V_{CC}-3$		V
V_{IH}	Input voltage High		$V_{CC}-1.4$		V
$\pm I_2$	Input/output current		150		μA
Segments (Pins 3 to 10 and 15 to 22)					
V_O	Output voltages	0.3		V_{CC}	V
$\pm I_O$	Output current High			10.0	μA
I_O	Output current Low; control bits C4, C5, and C6 High	17.85	21.0	24.15	mA
I_O	Contribution of control bit C4	2.55	3.0	3.45	mA
I_O	Contribution of control bit C5	5.10	6.0	6.90	mA
I_O	Contribution of control bit C6	10.20	12.0	13.80	mA
Relative Segment Output Current Accuracy					
$\triangle I_O$	at $I_{3\ to\ 10}$ and $I_{15\ to\ 22}$ = 3mA at $I_{3\ to\ 10}$ and $I_{15\ to\ 22}$ = 21mA		±7		% %
Multiplex 1 and 2 (Pins 11 and 14)					
V_O	Output voltage	0		$V_{CC}-1$	V
$-I_{11};\ I_{14}$	Output current High	50			mA
$I_{11,14}$	Output current Low	100	150	200	μA
f_{MPX}	Output frequency at C_{2-12} = 2.7nF	100		200	Hz
d	Output duty cycle		49.2		%

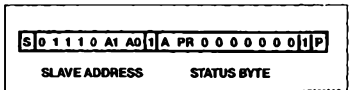


Figure 1. I²C Bus Format; Read Mode

ADDRESS PIN ADR

Four different slave addresses can be chosen by connecting ADR either to V_{EE}, $\frac{1}{3}$ V_{CC}, $\frac{2}{3}$ V_{CC} or V_{CC}. This results in the corresponding valid addresses HEX 70, 72, 74 and 76 for writing and 71, 73, 75 and 77 for reading. All other addresses cannot be acknowledged by the circuit.

STATUS BYTE

Only one bit is present in the status byte, the power reset flag. A "1" indicates the occurrence of a power failure since the last time it was read out. After completion of the read action, this flag will be set to "0."

SUBADDRESSING

The bits SC, SB and SA form a pointer and determine to which register the data byte following the instruction byte will be written. All other bytes will then be stored in the registers with consecutive subaddresses. This feature is called Auto-Increment (AI) of the subaddress and enables a quick initialization by the master. The subaddress pointer will wrap around from 7 to 0.

The subaddresses are given as follow:

SC	SB	SA	Subaddress	Function
0	0	0	00	Control Register
0	0	1	01	Digit 1
0	1	0	02	Digit 2
0	1	1	03	Digit 3
1	0	0	04	Digit 4
1	0	1	05	Reserved
1	1	0	06	Reserved
1	1	1	07	Reserved

CONTROL BITS (See Figure 3)

The control bits C0 to C6 have the following meaning:

- C0 = 0 Static mode, i.e., continuous display of digits 1 and 2
- C0 = 1 Dynamic mode, i.e., alternating display of digit 1 + 3 and 2 + 4
- C1 = 0/1 Digits 1 + 3 are blanked/not blanked
- C2 = 0/1 Digits 2 + 4 are blanked/not blanked
- C3 = 1 All outputs are switched on for segment test[1]
- C4 = 1 Adds 3mA to segment output current
- C5 = 1 Adds 6mA to segment output current
- C6 = 1 Adds 12mA to segment output current

NOTE:

1. At a current determined by C4, C5, and C6; C3 overrules C0, C1, and C2.

DATA

A segment is switched on if the corresponding data bit is one. Data bits D17 to D10 correspond with digit 1, D27 to D20 with digit 2, D37 to D30 with digit 3 and D47 to D40 with digit 4. The MSBs correspond with outputs P8 and P16, the LSBs with P1 and P9. Digit number is equal to its subaddress.

SDA, SCL

The SDA and SCL I/O meet the I_2C bus specification. For protection against positive voltage pulses on these inputs, voltage regulator diodes are connected to V_{EE}. This means that normal line voltage should not exceed 5.5V. Data will be latched on the positive-going edge of the acknowledge-related clock pulse.

POWER-ON RESET

The power-on reset signal is generated and sets all bits to zero, and results in a completely blanked display. Only the power reset flag is set.

C_{EXT}

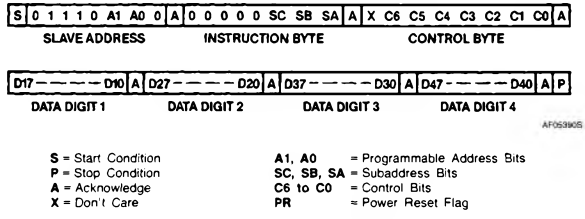
With a capacitor on Pin 2 the multiplex frequency can be set. In case of only static use this pin can be connected to V_{EE} or V_{CC} or left floating since the oscillator will be switched off.

SEGMENT OUTPUTS

The segment outputs P1 to P16 are controllable current sink sources, which are switched on by the corresponding data bits and whose current is adjustable by control bits C4, C5 and C6.

MULTIPLEX OUTPUTS

The multiplex outputs MX1 and MX2 are switched alternately in dynamic mode with a frequency derived from the clock oscillator. In static mode, MX1 is switched on. The outputs consist of an emitter-follower, which can be used to drive the common anodes of two displays directly as long as the total power dissipation of the circuit will not be exceeded. If so, an external transistor should be added as drawn in the application diagram of Figure 4.



S = Start Condition
P = Stop Condition
A = Acknowledge
X = Don't Care

A1, A0 = Programmable Address Bits
SC, SB, SA = Subaddress Bits
C6 to C0 = Control Bits
PR = Power Reset Flag

Figure 2. I²C Bus Format; Write Mode

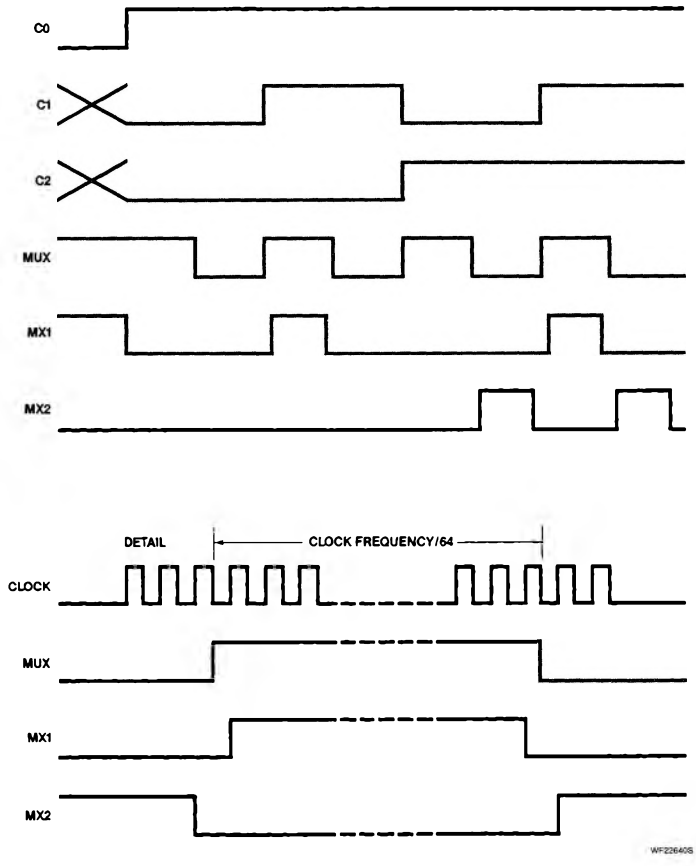


Figure 3. Timing Diagram

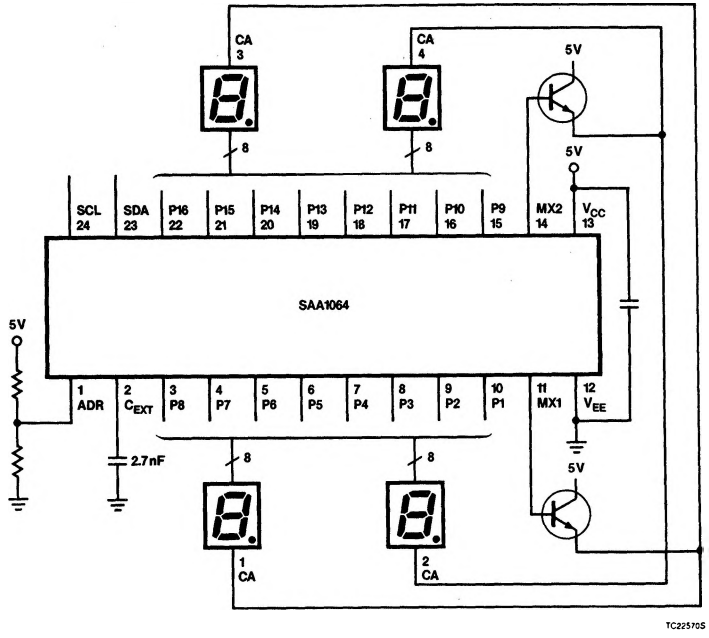


Figure 4. Dynamic Mode Application Diagram

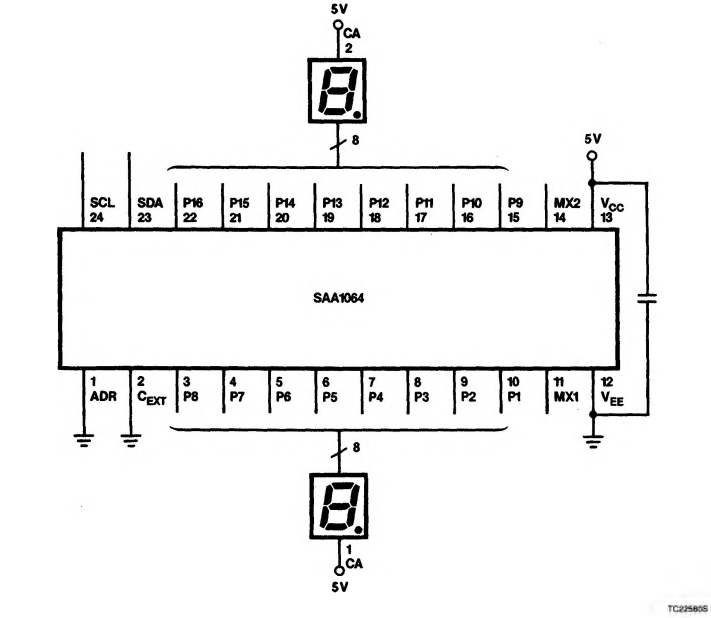


Figure 5. Static Mode Application Diagram