Signetics

SAA5045

Gearing and Address Logic Array for USA Teletext

Product Specification

Linear Products

DESCRIPTION

The SAA5045 is a PCF0700 CMOS process gate array designed to interface the SAA5040B Teletext Acquisition Control (TAC) IC to the SAA5030 Video Processor (VIP) data output for modified UK standard 525-line Teletext. It also provides an address interface between SAA5040B, SAA5025D Teletext Timing Chain for USA 525-line system (USTIC) and the page memory RAM. The memory interface includes read/write control compatible with the geared 32 + 8 transmission system at 5.727272MHz data rate employed in the modified UK system.

FEATURES

- **Implements the gearing function, allowing 40 characters/row display**
- **Generates memory control signals**
- **Gate array-based implementation**

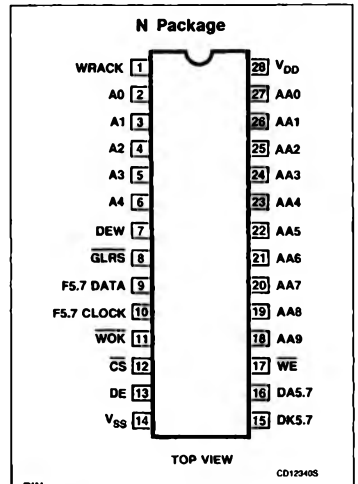
APPLICATION

- **Teletext**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117D)	−20°C to +70°C	SAA5045N

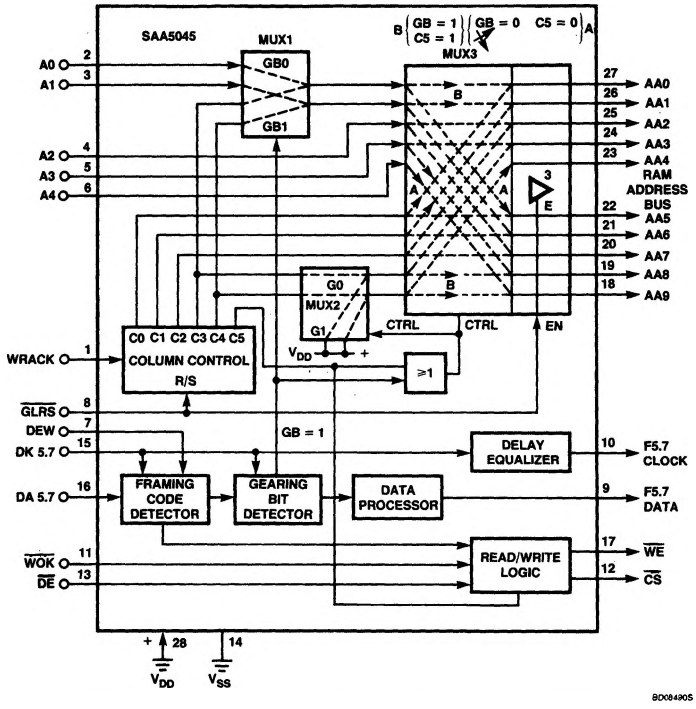
PIN CONFIGURATION



PIN NO.	SYMBOL	DESCRIPTION
1	WRACK	Input clock to column counter
2	A0	Row address system inputs
3	A1	
4	A2	
5	A3	
6	A4	
7	DEW	Data entry window input
8	$\overline{GLRS}$	General line reset starting output
9	F5.7 DATA	5.7MHz data output
10	F5.7 CLOCK	5.7MHz clock output
11	$\overline{WOK}$	Write enable input
12	$\overline{CS}$	Chip select output
13	DE	Display enable input
14	V_{SS}	Ground
15	DK5.7	5.7MHz data clock input
16	DA5.7	5.7MHz data input
17	$\overline{WE}$	Write enable output
18	AA9	Memory address outputs
19	AA8	
20	AA7	
21	AA6	
22	AA5	
23	AA4	
24	AA3	
25	AA2	
26	AA1	
27	AA0	
28	V_{DD}	Positive supply (+4.5V to +5.5V)

Gearing and Address Logic Array for USA Teletext SAA5045

BLOCK DIAGRAM



SYSTEM CONTENT

Functionally the chip contains two main sections which operate during the acquisition and display periods.

Gearing Control Section

The data from the SAA5030 (VIP) and data clock are processed to detect the presence of the gearing bit and convert the data for correct operation of the SAA5040B (TAC). Data and clock outputs to the TAC are internally compensated for processing delays, so that correct clocking-in of data is ensured.

Addressing Section

Column counters are included, which operate from the WACK (TAC) and RACK (USTIC) column clock signals during acquisition and display respectively.

Five row-address input circuits (pins A0 to A4) are provided for (TAC) and (USTIC) address outputs. These are multiplexed with the column address from the internal counters for correct mapping of the RAM via ten output address pins (AA0 to AA9). During acquisition, the multiplexer is controlled by the gearing bit detection to give correct assembly of the 40-character per row page structure.

The address output buffers are 3-State devices controlled by the line reset signal (Pin 8; $\overline{GLRS}$). During the horizontal flyback period, the address pins are 3-State to allow alternative addressing for customized applications.

Read/Write Control to RAM

An internal counter prevents overwriting if more than 32 character WOK pulses are received from TAC due to poor transmission conditions. Two control outputs, one for read/write ($\overline{WE}$) and the other for chip select ($\overline{CS}$), are provided to eliminate conflicts on the input/output RAM bus.

Framing Code Detection

When a valid data line is received and the framing code is detected in the gearing section, then flag pulses (pair of pulses) are available at output $\overline{WE}$, before the $\overline{CS}$ output is driven Low for normal writing into the RAM. If a framing-code-present signal is required, it can be obtained by gating $\overline{WE}$ and $\overline{CS}$ outputs such that an output from the $\overline{WE}$, when output $\overline{CS}$ is High indicates the detection of a framing code; N.B., each framing code produces a pair of pulses.

RAM ADDRESS CONTROL

The Block Diagram shows that the ten RAM address outputs are controlled by a multiplexer (MUX3) which interchanges the two groups of five address lines when a gearing bit equal to logic "1" is received during data input. During display, MUX3 is switched by Bit 6 of the column counter. MUX1, which is switched by the gearing bit, controls stepping of the row address when fill-in rows are received. MUX2 is switched by either the gearing bit or Bit 6 of the column counter to access the part of RAM storing the last eight bytes of each row of data.

The mapping of the 1024-byte RAM is shown in Figure 1. Area "A" stores data corresponding to the left-hand side (32 bytes wide) of the display and area "B" stores the remainder for the right-hand side.

Access to the RAM for custom operations can be made during the time that $\overline{GLRS}$ (Pin 8) is Low, which causes all ten address buffers to be in the open state. It should be noted that $\overline{GLRS}$ Low also resets the column counters and the gearing-bit detection system to logic "0". This normally occurs during the horizontal interval (between 5 and 8μs) after the horizontal sync pulse falling edge.

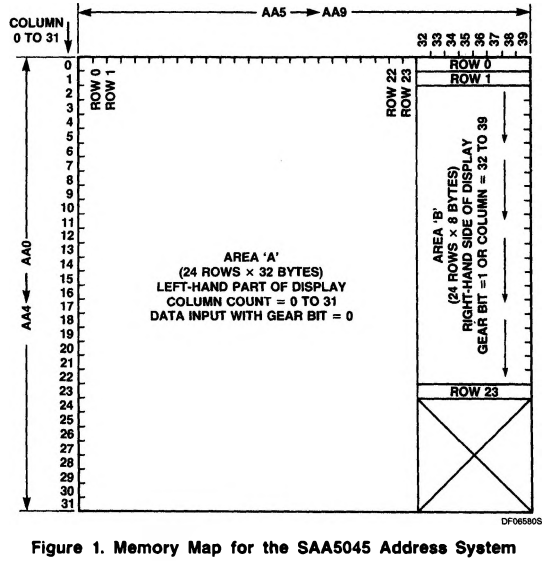


Figure 1. Memory Map for the SAA5045 Address System

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1 WRACK Input Clock to Column Counter — Input clock to column counter during data input or display; WACK from SAA5040B (TAC) or RACK from SAA5025D (USTIC).

2 to 6 A0 to A4 Row Address System Inputs — Inputs to row address system during data input or display. Row address numbers greater than 0 to 23 disable writing to the RAM during input.

7 DEW Data Entry Window Input — Data entry window input enables gearing bit detection and data processing part of system.

8 $\overline{\text{GLRS}}$ General Line Reset Starting Output — Input from the SAA5025D is a negative reset pulse at line rate for column counters and gearing system. When this input is Low, it opens 3-State address buffers.

9 F5.7 DATA 5.7MHz Data Output — Data output at 5.7MHz rate to SAA5040B (TAC) during the data acquisition period when DEW is High.

10 F5.7 CLOCK 5.7MHz Clock Output — Data clock output at 5.7MHz rate to SAA5040B (TAC), synchronized to data at Pin 9 (F5.7 DATA).

11 $\overline{\text{WOK}}$ Write Enable Input — Write enable input from SAA5040B (TAC) during data acquisition, when correct data is received, for RAM write/read control (via output $\overline{\text{WE}}$; Pin 17).

12 $\overline{\text{CS}}$ Chip Select Output — Output to drive the RAM chip enable during data input and display periods controlled by the display enable output (DE) and write O.K. ($\overline{\text{WOK}}$) output of the SAA5040B (TAC), avoiding input/output bus conflict.

13 DE Display Enable Input — Display enable input from SAA5040B (TAC) to control $\overline{\text{CS}}$.

14 V_{SS} — Ground.

15 DK5.7 5.7MHz Data Clock Input — Data clock input at 5.7MHz rate from the SAA5030 (VIP); this pin is capacitively-coupled with a DC restoring diode and is externally connected to V_{SS}.

16 DA5.7 5.7MHz Data Input — Data input at 5.7MHz rate from SAA5030 (VIP); this pin is capacitively-coupled with a DC restoring diode and is externally connected to V_{SS}.

17 $\overline{\text{WE}}$ Write Enable Output — Write enable output to control RAM write/read. This output is the gated and delay version of the $\overline{\text{WOK}}$ from the SAA5040B, but limited to 32. A pair of pulses which are possible before the WACK count is equal to 32. A pair of pulses on this output precedes the $\overline{\text{WOK}}$ pulses, while $\overline{\text{CS}}$ is High whenever a framing code is detected.

18 to 27 AA9 to AA0 Memory Address Outputs — Memory address outputs; 3-State buffered outputs, open when $\overline{\text{GLRS}}$ is Low for auxiliary access to the RAM address bus if required.

N.B.: AA9 and AA8 are simultaneously High whenever a gear bit with logic "1" is received during DEW is High. This enables detection of gearing bit reception, following $\overline{\text{GLRS}}$ reset on each line, which always resets AA0 to AA9 to logic "0".

28 V_{DD} Positive Supply (4.5V to 5.5V)

NOTE:

Input pins other than 15 and 16 have internal 15kΩ pull-up resistors for compatibility with SAA5025D and SAA5040B output signal ranges. Pins 15 and 16 are CMOS inputs for DC restored drive from the SAA5030 (VIP) clock and data output signals.

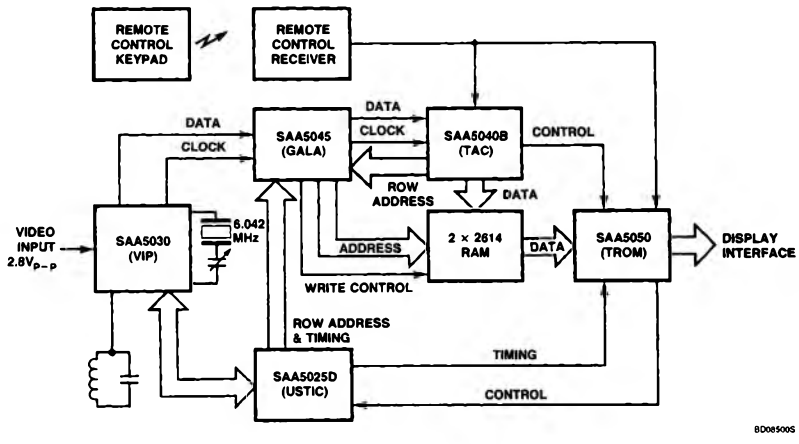


Figure 2. Schematic Diagram of the 5-Chip Decoder