Signetics

Linear Products

SAA5230
Teletext Video Processor

Product Specification

DESCRIPTION

The SAA5230 is a bipolar integrated circuit intended as a successor to SAA5030. It extracts teletext data from the video signal, regenerates teletext clock, and synchronizes the text display to the television syncs. The integrated circuit is intended to work in conjunction with CCT (SAA5040, Computer Controlled Teletext), EUROM SAA5350 or other compatible devices.

FEATURES

- Adaptive data slicer
- Data clock regenerator
- Sync separator, line phase detector, and 6MHz VCO forming display phase-locked loop (PLL)
- Performs all of the functions of the SAA5030 except field sync integration and signal quality detection
- When used with the SAA5240, a microprocessor-controlled teletext/data acquisition system can be easily implemented
- Good data slicing capability in the presence of echoes and noise with high-frequency loss compensation
- On-chip clock regeneration circuitry can operate with different data rates
- On-chip PLL allows display to be easily locked to a VCR
- Minimal number of external components/adjustments

APPLICATIONS

- Teletext
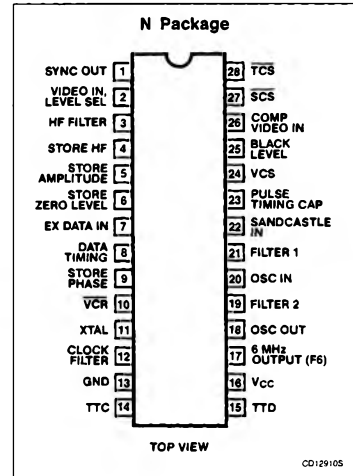- Data slicing and clock regeneration
- Phase locking with incoming video

PIN CONFIGURATION

N Package

Pin	Name		Pin	Name
1	SYNC OUT		28	TCS
2	VIDEO IN, LEVEL SEL		27	SCS
3	HF FILTER		26	COMP VIDEO IN
4	STORE HF		25	BLACK LEVEL
5	STORE AMPLITUDE		24	VCS
6	STORE ZERO LEVEL		23	PULSE TIMING CAP
7	EX DATA IN		22	SANDCASTLE IN
8	DATA TIMING		21	FILTER 1
9	STORE PHASE		20	OSC IN
10	VCR		19	FILTER 2
11	XTAL		18	OSC OUT
12	CLOCK FILTER		17	6 MHz OUTPUT (F6)
13	GND		16	Vcc
14	TTC		15	TTD

TOP VIEW

CD12910S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117)	−25°C to +70°C	SAA5230N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 16)	13.2	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +70	°C

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BLOCK DIAGRAM

SAA5230

Block	Pins
PULSE GENERATOR	24, 23
PHASE DETECTOR	21, 19, 10
VOLTAGE CONTR. OSCILLATOR	20, 18
SENSE SVS	
ADAPTIVE DATA SLICER	22
LATCHES	
ADAPTIVE SYNC SEPARATOR	27
DUAL POLARITY BUFFER	
CLOCK PHASE DETECTOR	
SENSE 'NO LOAD'	
SENSE EXTERNAL DATA	
PHASE SHIFTER	
GAIN SWITCH	
HF LOSS COMPENSATOR	
OSCILLATOR ÷2	

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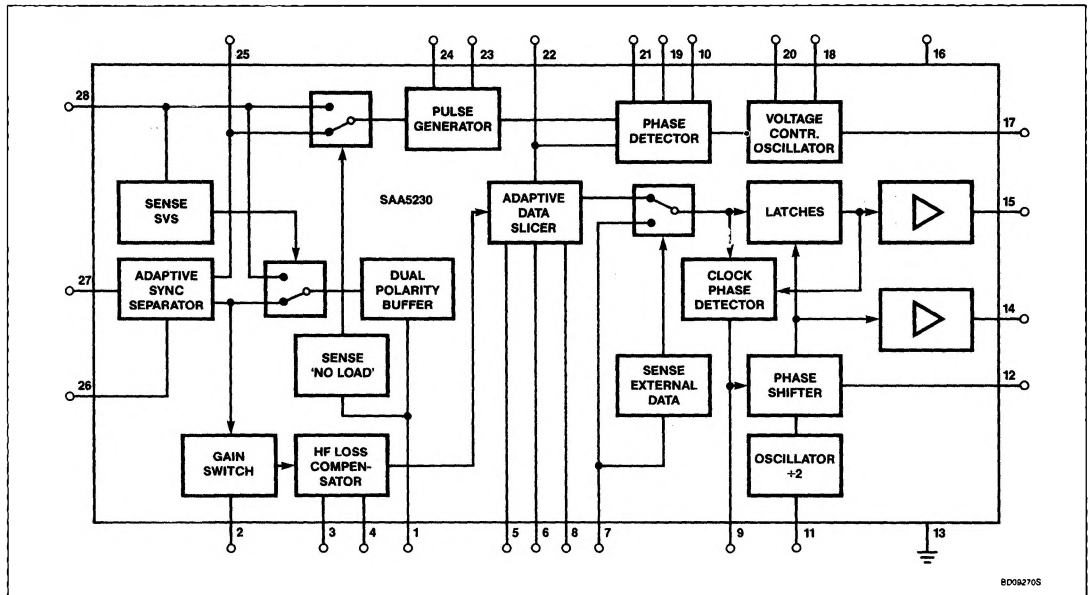
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DC AND AC ELECTRICAL CHARACTERISTICS V_{CC} = 12V; T_A = 25°C with external components as shown in Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	10.8	12.0	13.2	V
I_{CC}	Supply current		70		mA
Video input and sync separator					
$V_{27-13(P-P)}$ $V_{27-13(P-P)}$	Video input amplitude (sync to white) Pin 2 Low Pin 2 High	0.7 1.75	1 2.5	1.4 3.5	V V
$|Z_S|$	Source impedance			250	Ω
$V_{27-13(P-P)}$	Sync amplitude			1	V
Video level select input					
V_{2-13}	Input voltage Low	0		0.8	V
V_{2-13}	Input voltage High	2.0		5.5	V
I_2	Input current Low	0		-150	μA
I_2	Input current High	0		1	mA
Text composite sync input ($\overline{TCS}$)					
V_{28-13}	Input voltage Low	0		0.8	V
V_{28-13}	Input voltage High	2.0		7.0	V
Scan composite sync input ($\overline{SCS}$)					
V_{28-13}	Input voltage Low	0		1.5	V
V_{28-13}	Input voltage High	3.5		7.0	V
Select video sync from Pin 1					
I_{28} I_{28}	Input current V_I = 0 to 7V V_I = 10V to V_{CC}	-40 -5	-70	-100 +5	μA μA
Video composite sync output (VCS)					
V_{25-13}	Output voltage Low	0		0.4	V
V_{25-13}	Output voltage High	2.4		5.5	V
I_{25}	Output DC current Low			0.5	mA
I_{25}	Output DC current High			-1.5	mA
t_D	Sync separator delay time		0.5		μs
Dual polarity buffer output					
$V_{1(P-P)}$	$\overline{TCS}$ sync amplitude		0.45		V
$V_{1(P-P)}$	Video sync amplitude			1	V
I_1	Output current	-3		+3	mA
V_1 V_1	DC output voltage R_L to ground (0V) R_L to V_{CC} (12V)		1.4 10.1		V V

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = 12V$; $T_A = 25°C$ with external components as shown in Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Sandcastle input					
V_{22} V_{22}	Phase-lock pulse PL on (Low) PL off (High)	0 3.9		3 5.5	V V
V_{22} V_{22}	Blanking pulse CBB on (Low) CBB off (High)	0 1.0		0.5 5.5	V V
I_{22}	Input current	−10		+10	μA
PLL					
t_P t_P	Line sync timing pulse width (using composite video) pulse width (using scan composite sync)		2 3		μs μs
t_P	Pulse duration period PL must be Low to make VCO free-run	100			μs
6MHz-VCO (F6)					
$V_{17(P-P)}$	AC output voltage	1	2	3	V
V_{17-13}	DC output voltage	4		8	V
t_R, t_F	Rise and fall time	20		40	ns
C_{17-13}	Load capacitance			40	pF
VCR					
V_{10-13}	VCR-mode on (Low)	0		0.8	V
V_{10-13}	VCR-mode off (High)	2.0		V_{CC}	V
I_{10}	Input current	−10		+10	μA
Data slicer					
V_{27} V_{27}	Data amplitude of video input Pin 2 Low Pin 2 High	0.30 0.75	0.46 1.15	0.70 1.75	V V
Teletext clock output					
$V_{14(P-P)}$	AC output voltage	2	3	4	V
V_{14-13}	DC output voltage	4		8	V
C_L	Load capacitance			40	pF
t_R, t_F	Rise and fall times	20	30	45	ns
t_D	Delay of falling edge relative to other edges of TTD	−20	0	+20	ns
Teletext data output					
$V_{15(P-P)}$	AC output voltage	2.0	3.0	4.0	V
V_{15-13}	DC output voltage	4		8	V
C_L	Load capacitance			40	pF
$t_R = t_F$	Rise and fall times	20	30	45	ns

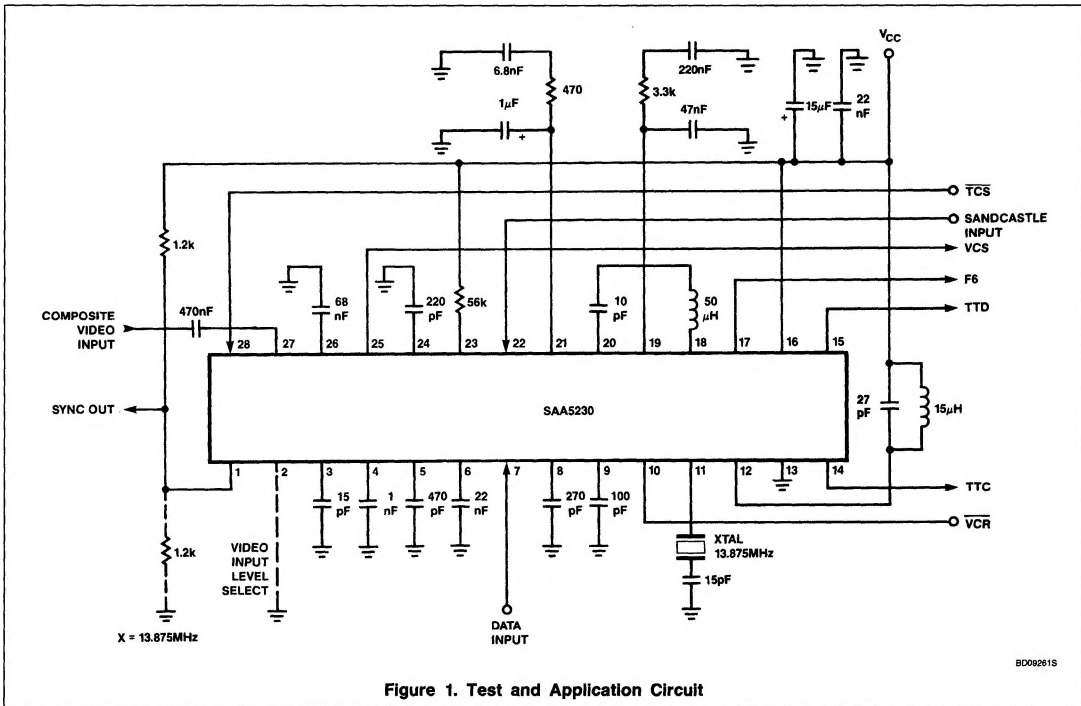# Teletext Video Processor — SAA5230

Figure 1. Test and Application Circuit

APPLICATION DATA

The function is quoted against the corresponding pin number.

1 Sync output to TV — Output with dual polarity buffer, a load resistor to 0V or +12V selects positive-going or negative-going syncs.

2 Video Input Level Select — Low level selects 1V input video level. With no connection, level floats High, selecting 2.5V level.

3 HF Filter — A capacitor connected to this pin filters the video signal for the HF loss compensator.

4 Store HF — The HF amplitude is stored by a capacitor connected to this pin.

5 Store Amplitude — Store capacitor stores the amplitude for the adaptive data slicer.

6 Store Zero Level — Store capacitor stores the zero level for the adaptive data slicer.

7 External Data Input — Current input for sliced teletext data from external device. Active High level (current), low impedance input.

8 Data Timing — A capacitor is connected to this pin for timing of the adaptive data slicer.

9 Store Phase — A capacitor connected to this pin stores the output signal from the clock phase detector.

10 Video Tape Recorder Mode ($\overline{VCR}$) — Signal input to command PLL into (short time constant mode), enable text to synchronize to a video tape recorder. Active is Low. If not connected, the level is High.

11 Crystal — A 13.875MHz crystal (2 × data rate) in series with a capacitor is connected to this pin.

12 Clock Filter — A filter for the clock signal is connected to this pin (6.938MHz).

13 Ground (0V)

14 Teletext Clock Output — TTC for CCT (Computer Controlled Teletext).

15 Teletext Data Output — TTD for CCT.

16 Supply Voltage V_{CC} — Typical value +12V.

17 F6 — 6MHz output clock for timing and sandcastle generation in CCT.

18 Oscillator Output (6MHz) — A series-resonant circuit is connected between this pin and Pin 20 to control the nominal frequency of the VCO.

19 Filter 2 — A filter for the line phase detector is connected to this pin. The filter has a short time constant and is used in video recorder mode and while the loop is locking up.

20 Oscillator Input (6MHz) — See Pin 18.

21 Filter 1 — A long time constant filter for the line phase detector is connected to this pin.

22 Sandcastle Input — This input accepts a sandcastle waveform, which is formed from PL and CBB from the CCT. For signal timing, see Figure 2.

23 Pulse Timing Resistor — A connected resistor defines the current for the pulse generator.

24 Pulse Timing Capacitor — A connected capacitor is used for timing of the pulse generator.

25 VCS Output — Video composite sync output signal for CCT.

26 Black Level — A capacitor connected to this pin stores the black level for the adaptive sync separator.

27 Composite Video Input — The composite video is fed to this input via a clamp capacitor.

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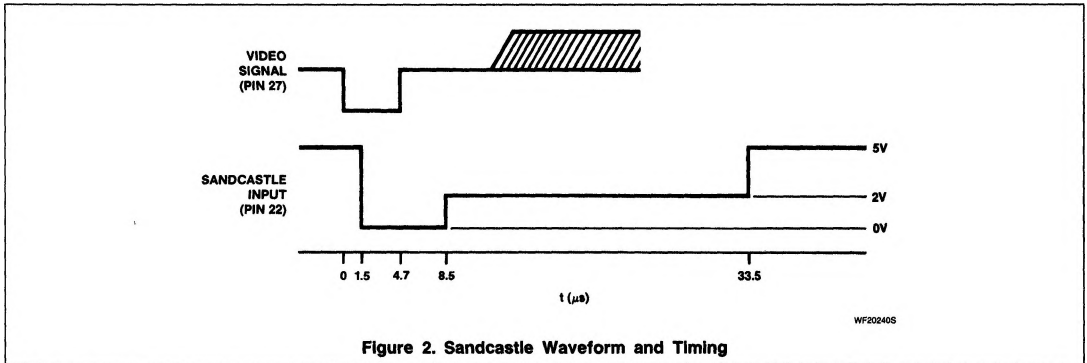**28 Sync Input** — Input for text composite sync (TCS) from CCT or SCS from external sync circuit. SCS is expected if there is no load resistor at Pin 1.

Figure 2. Sandcastle Waveform and Timing