

## SAB1164/65 1GHz Divide-by-64 Prescaler

### Product Specification

#### Linear Products

#### DESCRIPTION

This silicon monolithic integrated circuit is a prescaler in current-mode logic. It contains an amplifier, a divide-by-64 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a television tuner, with frequencies from 70MHz up to 1GHz, for a supply voltage of  $5V \pm 10\%$  and an ambient temperature of 0 to 70°C. It features a high sensitivity and low harmonic contents of the output signal.

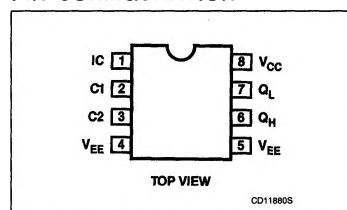
#### FEATURES

- 3mV (typ) sensitivity
- Differential Inputs
- AC input coupling; Internally based
- Outputs edge-controlled for low RFI
- Power consumption: 210mW (typ)
- Mini-DIP package
- Low output impedance (SAB1165)

#### APPLICATIONS

- PLL or FLL tuning systems, FM/communications/TV
- Frequency counters

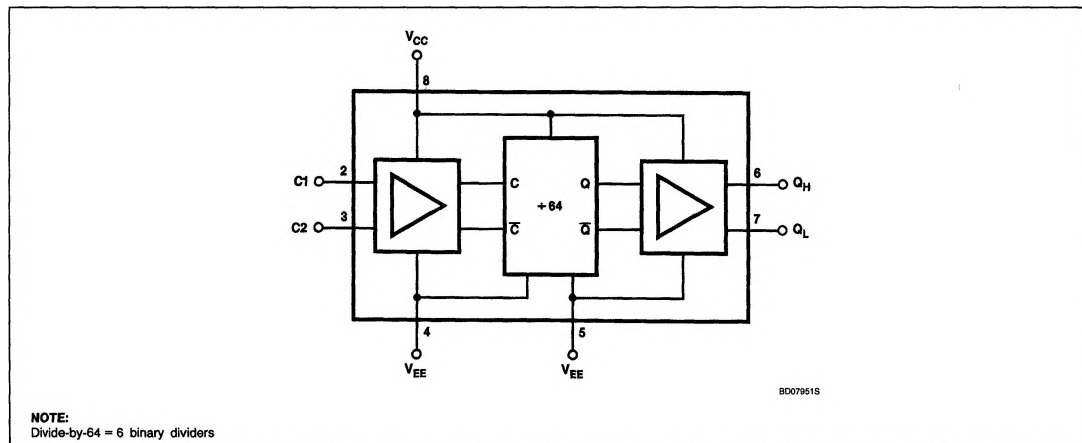
#### PIN CONFIGURATION



#### ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP (SOT-97A)	0 to +70°C	SAB1164N
8-Pin Plastic DIP (SOT-97A)	0 to +70°C	SAB1165N

#### BLOCK DIAGRAM



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## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage (DC)	7	V
V <sub>I</sub>	Input voltage	0 to V <sub>CC</sub>	V
T <sub>STG</sub>	Storage temperature range	-65 to +125	°C
T <sub>J</sub>	Junction temperature	125	°C
θ <sub>CA</sub>	Thermal resistance from crystal to ambient	120	°C/W

DC ELECTRICAL CHARACTERISTICS V<sub>EE</sub> = 0V (ground); V<sub>CC</sub> = 5V; T<sub>A</sub> = 25°C, unless otherwise specified.

The circuit has been designed to meet the DC specifications as shown below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V <sub>OH</sub> V <sub>OL</sub>	Output voltage HIGH level LOW level			V <sub>CC</sub> V <sub>CC</sub> - 0.8	V V
I <sub>CC</sub>	Supply current		42	50	mA

AC ELECTRICAL CHARACTERISTICS V<sub>EE</sub> = 0V (ground); V<sub>CC</sub> = 5V ± 10%; T<sub>A</sub> = 0 to +70°C

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V <sub>I(RMS)</sub>	Input voltage RMS value (see Figure 2)				
	input frequency 70MHz		9	17.5	mV
	150MHz		4	10	mV
	300MHz		3	10	mV
	500MHz		3	10	mV
	900MHz		2	10	mV
	1GHz		3	17.5	mV
V <sub>I(RMS)</sub>	Input overload voltage RMS value input frequency range 70MHz up to 1GHz			200	mV
V <sub>O(P-P)</sub>	Output voltage swing	0.8	1		V
R <sub>O</sub> R <sub>O</sub>	Output resistance SAB1164 SAB1165		1 0.5		kΩ kΩ
ΔV <sub>O</sub>	Output unbalance			0.1	V
t <sub>TLH</sub>	Output rise time <sup>1</sup> f <sub>i</sub> = 1GHz		25		ns
t <sub>THL</sub>	Output fall time <sup>1</sup> f <sub>i</sub> = 1GHz		25		ns

## NOTE:

1. Between 10% and 90% of observed waveform.

## FUNCTIONAL DESCRIPTION

The circuit contains an amplifier, a divide-by-64 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a TV tuner, with frequencies from 70MHz up to 1GHz, for a supply voltage of 5V ± 10% and an ambient temperature of 0 to +70°C.

The inputs are differential and are internally biased to permit capacitive coupling. For asymmetrical drive the unused input should be connected to ground via a capacitor.

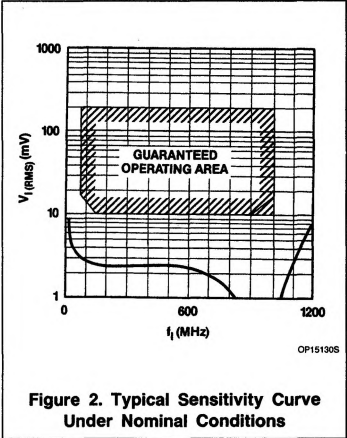
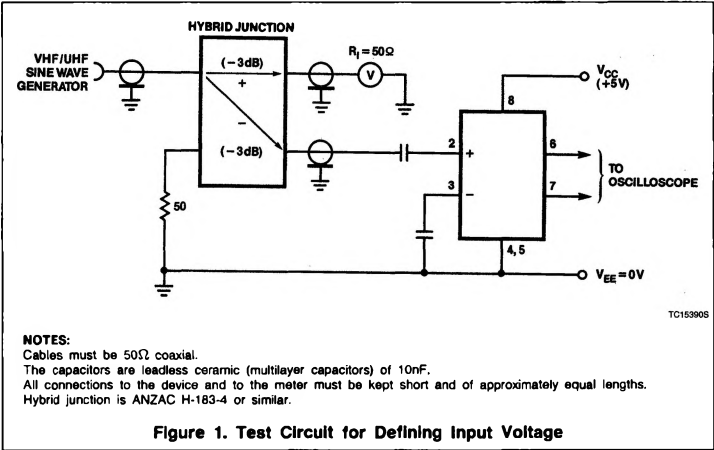
The first divider stage will oscillate in the absence of an input signal; an input signal within the specified range will suppress this oscillation.

The output differential stage has two complementary outputs. The output voltage edges are slowed down internally to reduce the harmonic contents of the signal.

Wide, low-impedance ground connections and a short capacitive bypass from the V<sub>CC</sub> pin to ground are recommended.

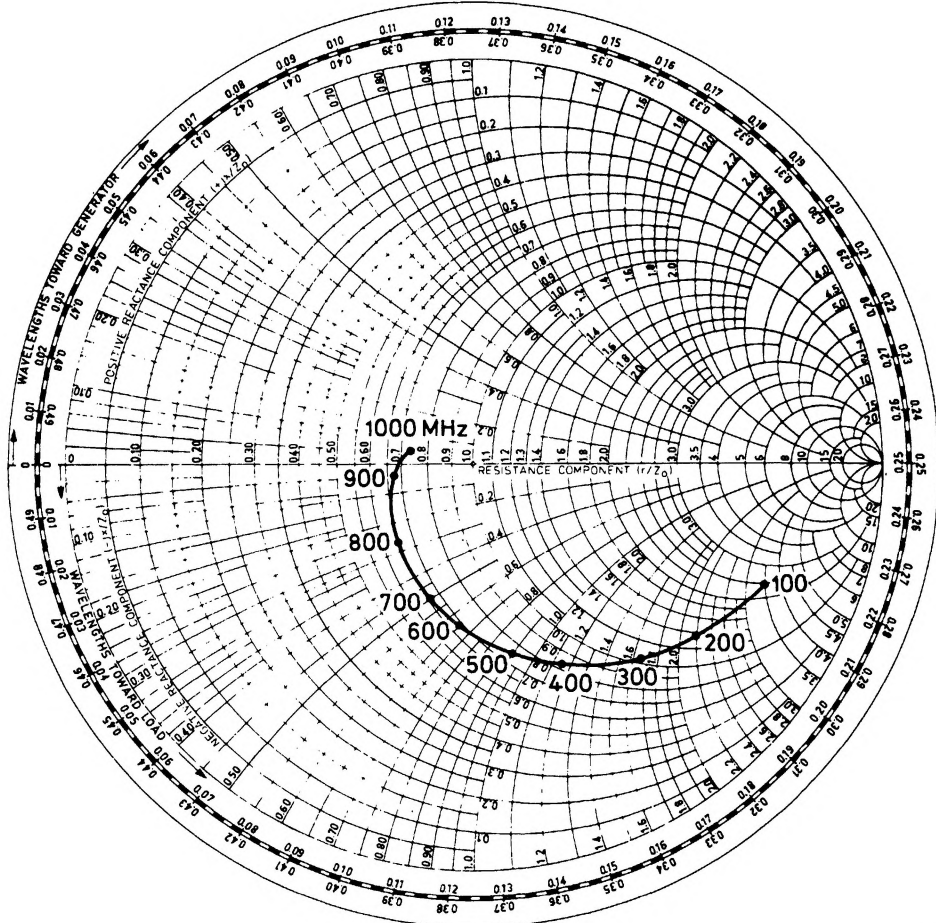
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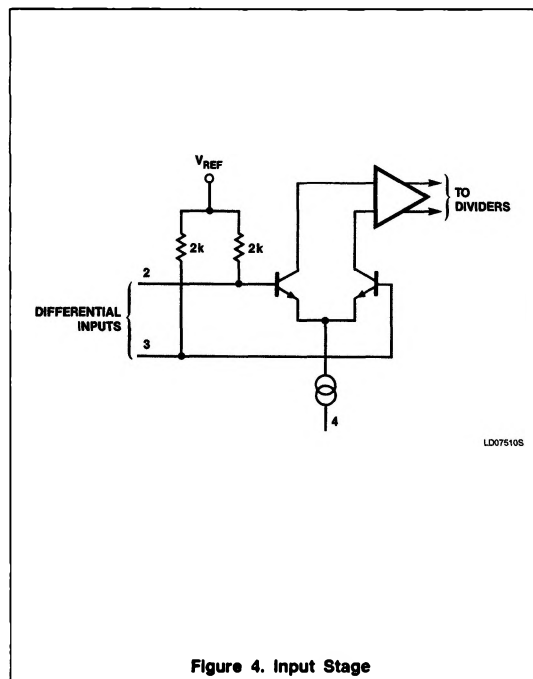
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NOTE:  
 $V_{I(RMS)} = 25mV$ ;  $V_{CC} = 5V$ ; reference value =  $50\Omega$ .

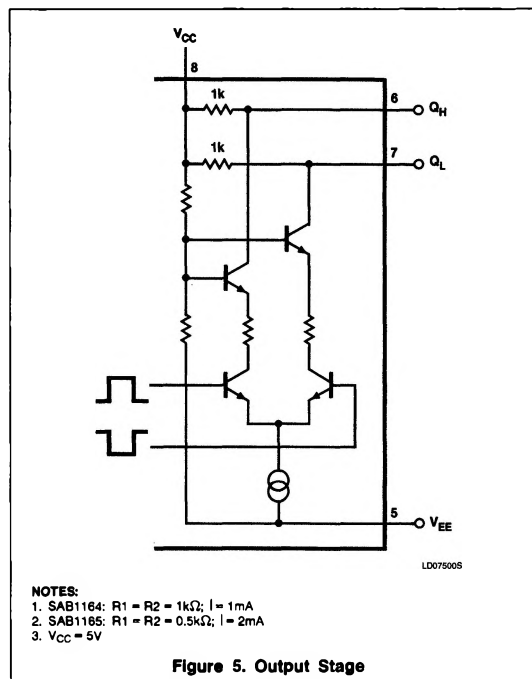
Figure 3. Smith Chart of Typical Input Impedance

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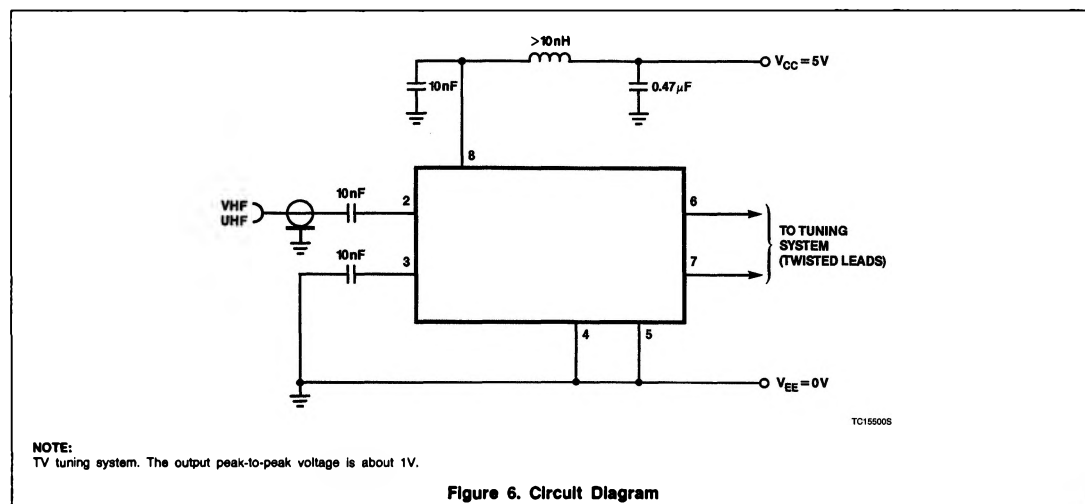
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### Figure 4. Input Stage



### Figure 5. Output Stage



**Figure 6. Circuit Diagram**