

# SAB3036

## FLL Tuning and Control Circuit

### Product Specification

### Linear Products

### DESCRIPTION

The SAB3036 provides closed-loop digital tuning of TV receivers, with or without AFC, as required. It also controls 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bi-directional I<sup>2</sup>C bus.

### FEATURES

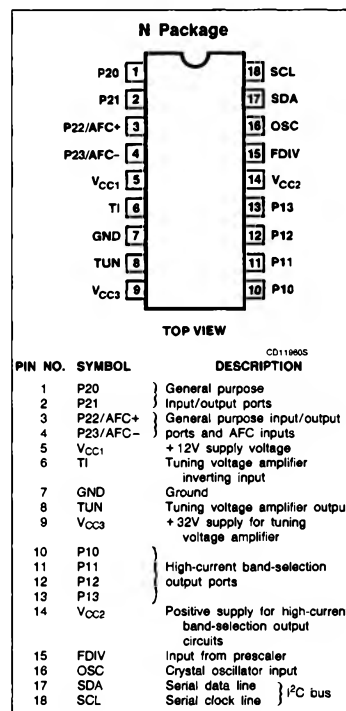
- Combined analog and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50kHz
- Selectable prescaler divisor of 64 or 256
- 32V tuning voltage amplifier

- 4 high-current outputs for direct band selection
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without AFC
- Single-pin, 4MHz on-chip oscillator
- I<sup>2</sup>C bus slave transceiver

### APPLICATIONS

- TV receivers
- Satellite receivers
- CATV converters

### PIN CONFIGURATION



### ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102HE)	-20°C to +70°C	SAB3036N

### ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
VCC1	Supply voltage ranges: (Pin 5)	-0.3 to +18	V
VCC2	(Pin 14)	-0.3 to +18	V
VCC3	(Pin 9)	-0.3 to +36	V
VSDA	Input/output voltage ranges: (Pin 17)	-0.3 to +18	V
VSCL	(Pin 18)	-0.3 to +18	V
VP20, P21	(Pins 1 and 2)	-0.3 to +18	V
VP22, P23, AFC	(Pins 3 and 4)	-0.3 to VCC1 <sup>1</sup>	V
VTI	(Pin 6)	-0.3 to VCC1 <sup>1</sup>	V
VTUN	(Pin 8)	-0.3 to VCC3	V
VP1X	(Pins 10 to 13)	-0.3 to VCC2 <sup>2</sup>	V
VFDIV	(Pin 15)	-0.3 to VCC1 <sup>1</sup>	V
VOSC	(Pin 16)	-0.3 to +5	V
PTOT	Total power dissipation	1000	mW
TSTG	Storage temperature range	-65 to +150	°C
TA	Operating ambient temperature range	-20 to +70	°C

### NOTES:

1. Pin voltage may exceed supply voltage if current is limited to 10mA.
2. Pin voltage must not exceed 18V but may exceed VCC2 if current is limited to 200mA.

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The diagram illustrates the internal architecture of the SAB3036, a tunable circuit. It features several input and output pins: VCC1 (5), GND (7), OSC (16), FDIV (15), VCC2 (14), VCC3 (9), SDA (17), and SCL (18). The internal blocks are interconnected as follows:

- Power and Oscillation:** VCC1, VCC2, and VCC3 supply power to various sections. The OSC pin is connected to a crystal and the Reference Oscillator.
- Control and Data:** The i2C BUS (pins 17, 18) interfaces with the POWER-DOWN DETECTOR, 2-BIT ADC, and TIME REFERENCE COUNTER. The TIME REFERENCE COUNTER also receives FDIV (pin 15) and provides signals to the GATE and 15-BIT FREQUENCY COUNTER.
- Frequency Synthesis:** The 15-BIT FREQUENCY COUNTER (pin 15) outputs to the 15-BIT FREQUENCY BUFFER (pin 15) and the TUNING CONTROL CIRCUIT. The TUNING CONTROL CIRCUIT includes blocks for FOV, FLOCK, FL, TDIR, AFCT, TUV, AFCT, and VTMI.
- Tuning and Frequency Control:** The 12-BIT TUNING COUNTER (pin 12) outputs to the DIVISOR SELECTOR and the CHARGE PUMP. The DIVISOR SELECTOR also receives signals from the TIME REFERENCE COUNTER and the 15-BIT FREQUENCY COUNTER. The CHARGE PUMP (pin 3) outputs to the TUNING VOLTAGE AMPLIFIER.
- Output and Feedback:** The TUNING VOLTAGE AMPLIFIER (pin 8) outputs to the TUNER (pin 8). The AFC AMPLIFIER (pin 6) provides feedback to the TUNING VOLTAGE AMPLIFIER and the COIB CORRECTION-IN-BAND CIRCUIT. The COIB CORRECTION-IN-BAND CIRCUIT (pin 6) outputs to the TUNING VOLTAGE AMPLIFIER.
- Other Components:** The TUNER (pin 10) is connected to the TUNING VOLTAGE AMPLIFIER. The COIB CORRECTION-IN-BAND CIRCUIT (pin 6) is connected to the TUNING VOLTAGE AMPLIFIER. The TUNING VOLTAGE AMPLIFIER (pin 8) is connected to the TUNER (pin 8).

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**DC AND AC ELECTRICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ;  $V_{CC1}$ ,  $V_{CC2}$ ,  $V_{CC3}$  at typical voltages, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
$V_{CC1}$ $V_{CC2}$ $V_{CC3}$	Supply voltages	10.5 4.7 30	12 13 32	13.5 16 35	V V V
$I_{CC1}$ $I_{CC2}$ $I_{CC3}$	Supply currents (no outputs loaded)	14 0 0.2	23  0.6	40 0.1 2	mA mA mA
$I_{CC2A}$ $I_{CC3A}$	Additional supply currents (A) <sup>1</sup>	-2 0.2		$I_{OHP1X}$ 2	mA mA
$P_{TOT}$	Total power dissipation		300		mW
$T_A$	Operating ambient temperature	-20		+70	°C
<b>I<sup>2</sup>C bus inputs/outputs</b> SDA input (Pin 17); SCL input (Pin 18)					
$V_{IH}$	Input voltage HIGH <sup>2</sup>	3		$V_{CC1} - 1$	V
$V_{IL}$	Input voltage LOW	-0.3		1.5	V
$I_{IH}$	Input current HIGH <sup>2</sup>			10	μA
$I_{IL}$	Input current LOW <sup>2</sup>			10	μA
	SDA output (Pin 17, open-collector)				
$V_{OL}$	Output voltage LOW at $I_{OL} = 3\text{mA}$			0.4	V
$I_{OL}$	Maximum output sink current		5		mA
<b>Open-collector I/O ports</b> P20, P21, P22, P23 (Pins 1 to 4, open-collector)					
$V_{IH}$	Input voltage HIGH (P20, P21)	2		16	V
$V_{IH}$	Input voltage HIGH (P22, P23) AFC switched off	2		$V_{CC1} - 2$	V
$V_{IL}$	Input voltage LOW	-0.3		0.8	V
$I_{IH}$	Input current HIGH			25	μA
$-I_{IL}$	Input current LOW			25	μA
$V_{OL}$	Output voltage LOW at $I_{OL} = 2\text{mA}$			0.4	V
$I_{OL}$	Maximum output sink current		4		mA
<b>AFC amplifier</b> Inputs AFC+, AFC- (Pins 3, 4)					
	Transconductance for input voltage up to 1V differential: AFCS1      AFCS2				
$g_{00}$	0      0	100	250	800	nA/V
$g_{01}$	0      1	15	25	35	μA/V
$g_{10}$	1      0	30	50	70	μA/V
$g_{11}$	1      1	60	100	140	μA/V
$\Delta M_g$	Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	-20		+20	%
$V_{IOFF}$	Input offset voltage	-75		+75	mV
$V_{COM}$	Common-mode input voltage	3		$V_{CC1} - 2.5$	V
CMRR	Common-mode rejection ratio		50		dB
PSRR	Power supply ( $V_{CC1}$ ) rejection ratio		50		dB
$I_i$	Input current (P22 and P23 programmed HIGH)			500	nA

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued)  $T_A = 25^\circ\text{C}$ ;  $V_{CC1}$ ,  $V_{CC2}$ ,  $V_{CC3}$  at typical voltages, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Tuning voltage amplifier Input TI, output TUN (Pins 6, 8)					
V <sub>TUN</sub>	Maximum output voltage at I <sub>LOAD</sub> = ±2.5mA	V <sub>CC3</sub> – 1.6		V <sub>CC3</sub> – 0.4	V
	Minimum output voltage at I <sub>LOAD</sub> = ±2.5mA:				
	VTMI1 VTMI0				
V <sub>TM00</sub>	0 0	300		500	mV
V <sub>TM10</sub>	1 0	450		650	mV
V <sub>TM11</sub>	1 1	650		900	mV
–I <sub>TUNH</sub>	Maximum output source current	2.5		8	mA
I <sub>TUNL</sub>	Maximum output sink current		40		mA
I <sub>TI</sub>	Input bias current	–5		+ 5	nA
PSRR	Power supply (V <sub>CC3</sub> ) rejection ratio		60		dB
	Minimum charge IT to tuning voltage amplifier				
	TUHN1 TUHN0				
CH <sub>00</sub>	0 0	0.4	1	1.7	μA/μs
CH <sub>01</sub>	0 1	4	8	14	μA/μs
CH <sub>10</sub>	1 0	15	30	48	μA/μs
CH <sub>11</sub>	1 1	130	250	370	μA/μs
ΔCH	Tolerance of charge (or ΔV <sub>TUN</sub> ) multiplying factor when COIB and/or TUS are used	–20		+ 20	%
	Maximum current I into tuning amplifier				
	TUHN1 TUHN0				
I <sub>T00</sub>	0 0	1.7	3.5	5.1	μA
I <sub>T01</sub>	0 1	15	29	41	μA
I <sub>T10</sub>	1 0	65	110	160	μA
I <sub>T11</sub>	1 1	530	875	1220	μA
Correction-in-band					
ΔV <sub>QIB</sub>	Tolerance of correction-in-band levels 12V, 18V and 24V	–15		+ 15	%
Band-select output ports P10, P11, P12, P13 (Pins 10 to 13)					
V <sub>OH</sub>	Output voltage HIGH at –I <sub>OH</sub> = 50mA <sup>3</sup>	V <sub>CC2</sub> – 0.6			V
V <sub>OL</sub>	Output voltage LOW at I <sub>OL</sub> = 2mA			0.4	V
–I <sub>OH</sub>	Maximum output source current <sup>3</sup>		130	200	mA
I <sub>OL</sub>	Maximum output sink current		5		mA
FDIV Input (Pin 15)					
V <sub>FDIV (P-P)</sub>	Input voltage (peak-to-peak value) (t <sub>RISE</sub> and t <sub>FALL</sub> ≤ 40ns)	0.1		2	V
	Duty cycle	40		60	%
f <sub>MAX</sub>	Maximum input frequency	16			MHz
Z <sub>I</sub>	Input impedance		8		kΩ
C <sub>I</sub>	Input capacitance		5		pF

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**DC AND AC ELECTRICAL CHARACTERISTICS (Continued)**  $T_A = 25^\circ\text{C}$ ;  $V_{CC1}$ ,  $V_{CC2}$ ,  $V_{CC3}$  at typical voltages, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
OSC Input (Pin 24)					
R <sub>X</sub>	Crystal resistance at resonance (4MHz)			150	Ω
Power-down reset					
V <sub>PD</sub>	Maximum supply voltage V <sub>CC1</sub> at which power-down reset is active	7.5		9.5	V
t <sub>R</sub>	V <sub>CC1</sub> rise time during power-up (up to V <sub>PD</sub> )	5			μs
Voltage level for valid module address					
	Voltage level at P20 (Pin 1) for valid module address as a function of MA1, MA0				
	MA1      MA0				
V <sub>VA00</sub>	0          0	-0.3		16	V
V <sub>VA01</sub>	0          1	-0.3		0.8	V
V <sub>VA10</sub>	1          0	2.5		V <sub>CC1</sub> - 2	V
V <sub>VA11</sub>	1          1	V <sub>CC1</sub> - 0.3		V <sub>CC1</sub>	V

**NOTES:**

- For each band-select output which is programmed at logic 1, sourcing a current  $I_{OHP1X}$ , the additional supply currents (A) shown must be added to  $I_{CC2}$  and  $I_{CC3}$ , respectively.
- If  $V_{CC1} < 1\text{V}$ , the input current is limited to  $10\mu\text{A}$  at input voltages up to  $16\text{V}$ .
- At continuous operation the output current should not exceed  $50\text{mA}$ . When the output is short-circuited to ground for several seconds the device may be damaged.
- Values are proportional to  $V_{CC1}$ .

# PLL Tuning and Control Circuit

**SAB3036**

## FUNCTIONAL DESCRIPTION

The SAB3036 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I<sup>2</sup>C bus.

## Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50kHz within a programmable tuning window (TUW).

The system cycles over a period of 6.4ms (or 2.56ms), controlled by the time reference counter which is clocked by an on-chip 4MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation  $\Delta f$  in steps of 50kHz. For loop gain control, the relationship  $\Delta IT/\Delta f$  is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at  $\Delta f = 50\text{kHz}$  equals  $250\mu\text{A} \mu\text{s}$  (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge

IT at  $\Delta f = 50\text{kHz}$  equals  $2^6 \times 2^3 \times 250\mu\text{A} \mu\text{s}$  (typical).

The maximum tuning current I is  $875\mu\text{A}$  (typical). In the tuning-hold (TUHN) mode (TUHN is Active-LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable AFC hold range (AFCH), which always occurs if AFCH is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, AFC will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCH. If the frequency of the tuning oscillator does not remain within AFCH, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The AFC has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will

react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and AFC to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTML to prevent the tuner being driven into an unspecified low tuning voltage region.

## Control

For tuner band selection there are four outputs — P10 to P13 — which are capable of sourcing up to 50mA at a voltage drop of less than 600mV with respect to the separate power supply input V<sub>CC2</sub>.

For additional digital control, four open-collector I/O ports — P20 to P23 — are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals and are connected with the AFC+ and AFC- inputs, respectively. The AFC amplifier must be switched off when P22 and/or P23 are used. When AFC is used, P22 and P23 must be programmed HIGH (high impedance state). With the aid of port P20, up to three independent module addresses can be programmed.

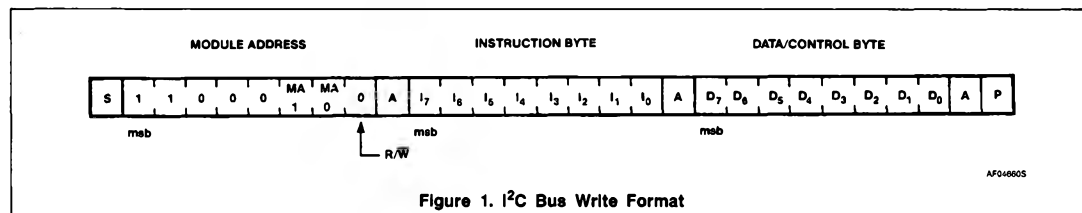
## Reset

CITAC goes into the power-down reset mode when V<sub>CC1</sub> is below 8.5V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

## OPERATION

### Write

CITAC is controlled via a bidirectional two-wire I<sup>2</sup>C bus. For programming, a module address, R/W bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Figure 1.



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The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down reset mode ( $V_{CC1} > 8.5V$  (typical)).

## Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Figure 2.

### Frequency

Frequency is set when Bit  $I_7$  of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50kHz. All frequency bits are set to logic 1 at reset.

### Tuning Hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at  $\Delta f = 50kHz$ ) into the tuning amplifier.

During tuning but before lock-in, the highest current value should be selected. After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (maximum 5nA). However, it is good practice to program the lowest current value during tuner band switching.

### Tuning Sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at  $\Delta f = 50kHz$ ; TUHN0 and TUHN1 = logic 1.

**Table 1. Valid Module Addresses**

MA1	MA0	P20
0	0	Don't care
0	1	GND
1	0	$\frac{1}{2} V_{CC1}$
1	1	$V_{CC1}$

**Table 2. Tuning Current Control**

TUHN1	TUHN0	TYP. $I_{MAX}$ ( $\mu A$ )	TYP. $I_{TMIN}$ ( $\mu A/\mu s$ )	TYP. $\Delta V_{TUNmin}$ at $C_{INT} = 1\mu F$ ( $\mu V$ )
0	0	3.5 <sup>1</sup>	1 <sup>1</sup>	1 <sup>1</sup>
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

NOTE:

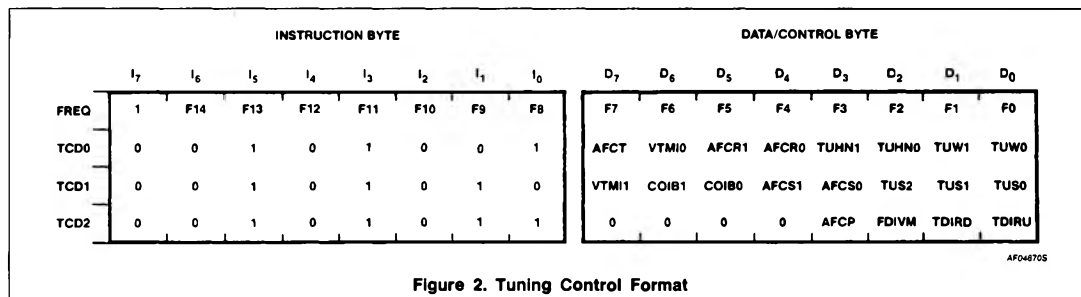
1. Values after reset.

**Table 3. Minimum Charge IT as a Function of TUS  $\Delta f = 50kHz$ ;  
TUHN0 = Logic 1; TUHN1 = Logic 1**

TUS2	TUS1	TUS0	TYP. $I_{TMIN}$ (mA/ $\mu s$ )	TYP. $\Delta V_{TUNmin}$ at $C_{INT} = 1\mu F$ (mV)
0	0	0	0.25 <sup>1</sup>	0.25 <sup>1</sup>
0	0	1	0.5	0.5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

NOTE:

1. Values after reset.


**Figure 2. Tuning Control Format**

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**Correction-In-Band**

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation 1T and takes into account the tuning voltage  $V_{TUN}$  to give charge multiplying factors as shown in Table 4.

The transconductance multiplying factor of the AFC amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

**Tuning Window**

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation  $|\Delta f|$  between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUN value (see Table 5). If  $|\Delta f|$  is up to 50kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

**AFC**

When AFCT is set to logic 1 it will not be cleared and the AFC will remain on as long as  $|\Delta f|$  is less than the value programmed for the AFC hold range AFCH (see Table 6). It is possible for the AFC to remain on for values of up to 50kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

**Transconductance**

The transconductance (g) of the AFC amplifier is programmed via the AFC sensitivity bits AFCS as shown in Table 7.

**AFC Polarity**

If a positive differential input voltage is applied to the (switched on) AFC amplifier, the tuning voltage  $V_{TUN}$  falls when the AFC polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1,  $V_{TUN}$  rises.

**Minimum Tuning Voltage**

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

**Frequency Measuring Window**

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

**Tuning Direction**

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

**Table 4. Programming Correction-In-Band**

COIB1	COIB0	CHARGE MULTIPLYING FACTORS AT TYPICAL VALUES OF $V_{TUN}$ AT:			
		< 12V	12 to 18V	18 to 24V	> 24V
0	0	1 <sup>1</sup>	1 <sup>1</sup>	1 <sup>1</sup>	1 <sup>1</sup>
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

**NOTE:**

1. Values after reset.

**Table 5. Tuning Window Programming**

TUN1	TUN0	$ \Delta f $ (kHz)	TUNING WINDOW (kHz)
0	0	0 <sup>1</sup>	0 <sup>1</sup>
0	1	50	100
1	0	150	300

**NOTE:**

1. Values after reset.

**Table 6. AFC Hold Range Programming**

AFCH1	AFCH0	$ \Delta f $ (kHz)	AFC HOLD RANGE (kHz)
0	0	0 <sup>1</sup>	0 <sup>1</sup>
0	1	350	700
1	0	750	1500

**NOTE:**

1. Values after reset.

**Table 7. Transconductance Programming**

AFCS1	AFCS0	TYP. TRANSCONDUCTANCE ( $\mu A/V$ )
0	0	0.25 <sup>1</sup>
0	1	25
1	0	50
1	1	100

**NOTE:**

1. Value after reset.

**Table 8. Frequency Measuring Window Programming**

FDIVM	PRESALER DIVISION FACTOR	CYCLE PERIOD (ms)	MEASURING WINDOW (ms)
0	256	6.4 <sup>1</sup>	5.12 <sup>1</sup>
1	64	2.56	1.28

**NOTE:**

1. Values after reset.



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### Control

The instruction byte POD (port output data) is shown in Figure 3, together with the corresponding data/control byte. Control is implemented as follows:

**P13, P12, P11, P10** — Band select outputs. If a logic 1 is programmed on any of the POD bits D<sub>3</sub> to D<sub>0</sub>, the relevant output goes HIGH. All outputs are LOW after reset.

**P23, P22, P21, P20** — Open-collector I/O ports. If a logic 0 is programmed on any of the POD bits D<sub>7</sub> to D<sub>4</sub>, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

## Read

Information is read from CITAC when the R/W bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Figure 4.

### Tuning/Reset Information Bits

**FLOCK** — Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.

**FL/1N** — Set to logic 0 (Active-LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.

**FL/ON** — As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.

**FOV** — Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.

**RESN** — Set to logic 0 (Active-LOW) by a programmed reset or a power-down reset. It is reset to logic 1 automatically after tuning/reset information has been read.

**MWN** — MWN (frequency measuring window, Active-LOW) is at logic 1 for a period of 1.28ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured.

When slightly different frequencies are programmed repeatedly and AFC is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being

loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

### Port Information Bits

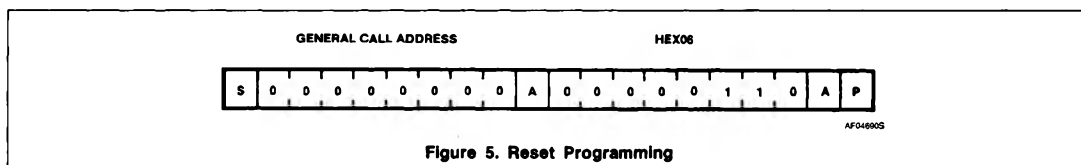
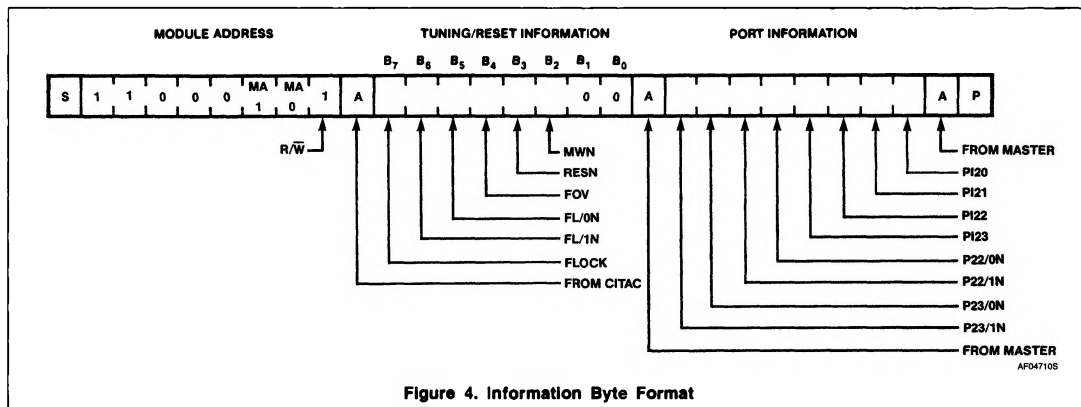
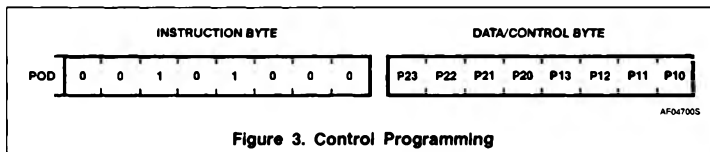
**P23/1N, P22/1N** — Set to logic 0 (Active-LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22, respectively. Both are reset to logic 1 after the port information has been read.

**P23/0N, P22/0N** — As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.

**P123, P122, P121, P120** — Indicate input voltage levels at P23, P22, P21 and P20, respectively. A logic 1 indicates a HIGH input level.

## Reset

The programming to reset all registers is shown in Figure 5. Reset is activated only at data byte HEX06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.



## FLL Tuning and Control Circuit

SAB3036

**I<sup>2</sup>C Bus Timing**

I<sup>2</sup>C bus load conditions are as follows:

4k $\Omega$  pull-up resistor to +5V; 200pF capacitor to GND.

All values are referred to  $V_{IH} = 3V$  and  $V_{IL} = 1.5V$ .

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
$t_{BUF}$	Bus free before start	4			$\mu s$
$t_{SU}, t_{STA}$	Start condition setup time	4			$\mu s$
$t_{HD}, t_{STA}$	Start condition hold time	4			$\mu s$
$t_{LOW}$	SCL, SDA LOW period	4			$\mu s$
$t_{HIGH}$	SCL HIGH period	4			$\mu s$
$t_R$	SCL, SDA rise time			1	$\mu s$
$t_F$	SCL, SDA fall time			0.3	$\mu s$
$t_{SU}, t_{DAT}$	Data setup time (write)	1			$\mu s$
$t_{HD}, t_{DAT}$	Data hold time (write)	1			$\mu s$
$t_{SU}, t_{CAC}$	Acknowledge (from CITAC) setup time			2	$\mu s$
$t_{HD}, t_{CAC}$	Acknowledge (from CITAC) hold time	0			$\mu s$
$t_{SU}, t_{STO}$	Stop condition setup time	4			$\mu s$
$t_{SU}, t_{RDA}$	Data setup time (read)			2	$\mu s$
$t_{HD}, t_{RDA}$	Data hold time (read)	0			$\mu s$
$t_{SU}, t_{MAC}$	Acknowledge (from master) setup time	1			$\mu s$
$t_{HD}, t_{MAC}$	Acknowledge (from master) hold time	2			$\mu s$

**NOTE:**

1. Timings  $t_{SU}$ ,  $t_{DAT}$  and  $t_{HD}$ ,  $t_{DAT}$  deviate from the I<sup>2</sup>C bus specification.

After reset has been activated, transmission may only be started after a 50 $\mu s$  delay.

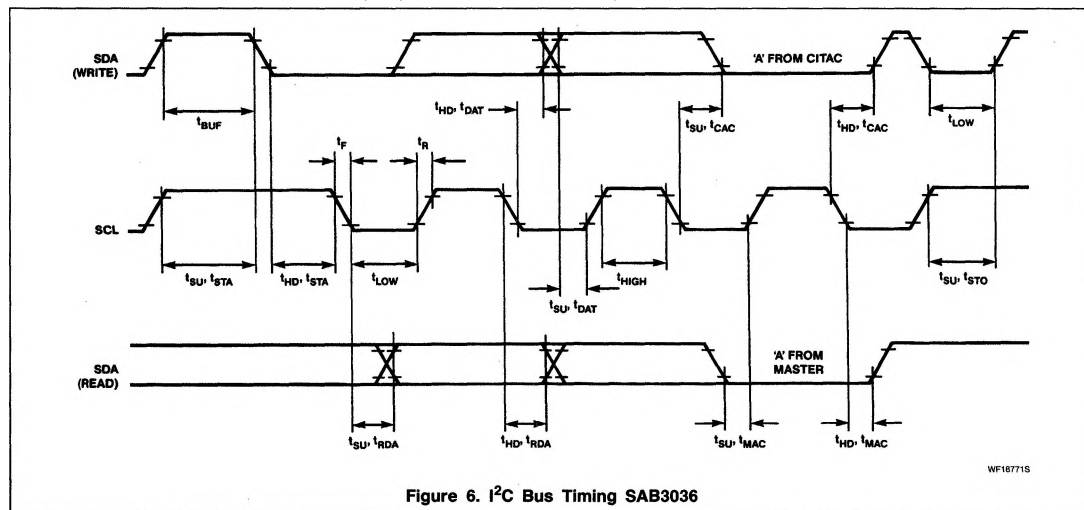


Figure 6. I<sup>2</sup>C Bus Timing SAB3036

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