SIEMENS

High-Performance
8-Bit CMOS Single-Chip Microcontroller SAB 80C515/80C535

Preliminary

SAB 80C515/80C515-16 CMOS microcontroller with factory mask-programmable ROM
SAB 80C535/80C535-16 CMOS microcontroller for external ROM

- 8 K × 8 ROM (SAB 80C515 only)
- 256 × 8 RAM
- Six 8-bit I/O ports, one input port for digital or analog input
- Three 16-bit timer/counters
- Highly flexible reload, capture, compare capabilities
- Full-duplex serial channel
- Twelve interrupt vectors, four priority levels
- 8-bit A/D converter with 8 multiplexed inputs and programmable internal reference voltages
- 16-bit watchdog timer
- Boolean processor
- Most instructions execute in 1 μs (750 ns)
- 4 μs (3 μs) multiply and divide
- External memory expandable up to 128 Kbytes
- Backwardly compatible with SAB 8051
- Functionally compatible with SAB 80515
- Idle and power-down mode
- Plastic leaded chip carrier package: P-LCC-68
- Plastic Metric Quad Flat Package P-MQFP-80
- Two temperature ranges available:
  0 to 70 °C (for 12, 16, 20 MHz)
  – 40 to 85 °C (for 12, 16 MHz)

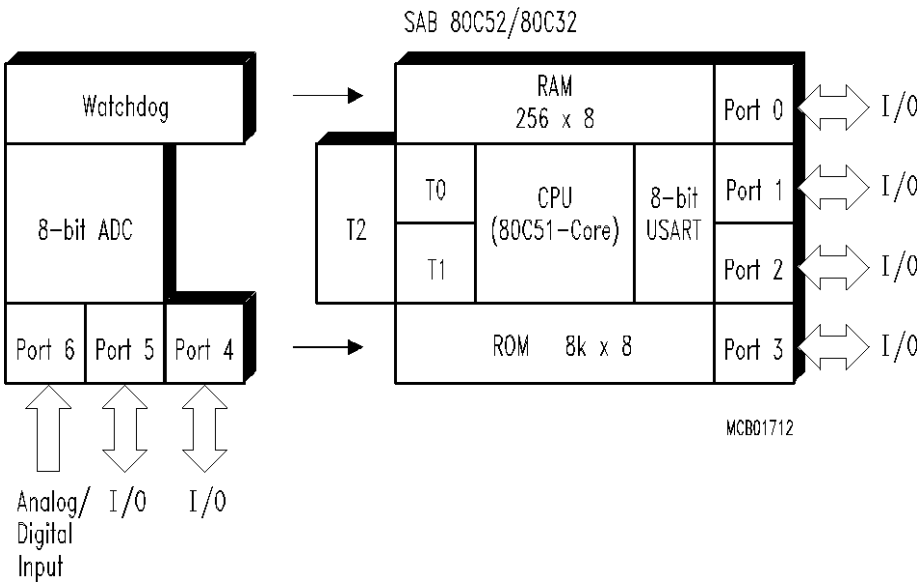
The SAB 80C515/80C535 is a powerful member of the Siemens SAB 8051 family of 8-bit microcontrollers. It is designed in Siemens ACMOS technology and is functionally compatible with the SAB 80515/80535 devices designed in MYMOS technology.

The SAB 80C515/80C535 is a stand-alone, high-performance single-chip microcontroller based on the SAB 8051/80C51 architecture. While maintaining all the SAB 80C51 operating characteristics, the SAB 80C515/80C535 incorporates several enhancements which significantly increase design flexibility and overall system performance.

In addition, the low-power properties of Siemens ACMOS technology allow applications where power consumption and dissipation are critical. Furthermore, the SAB 80C515/80C535 has two software-selectable modes of reduced activity for further power reduction: idle and power-down mode.

The SAB 80C535 is identical with the SAB 80C515 except that it lacks the on-chip program memory. The SAB 80C515/80C535 is supplied in a 68-pin plastic leaded chip carrier package (P-LCC-68) or in a plastic metric quad flat package (P-MQFP-80).

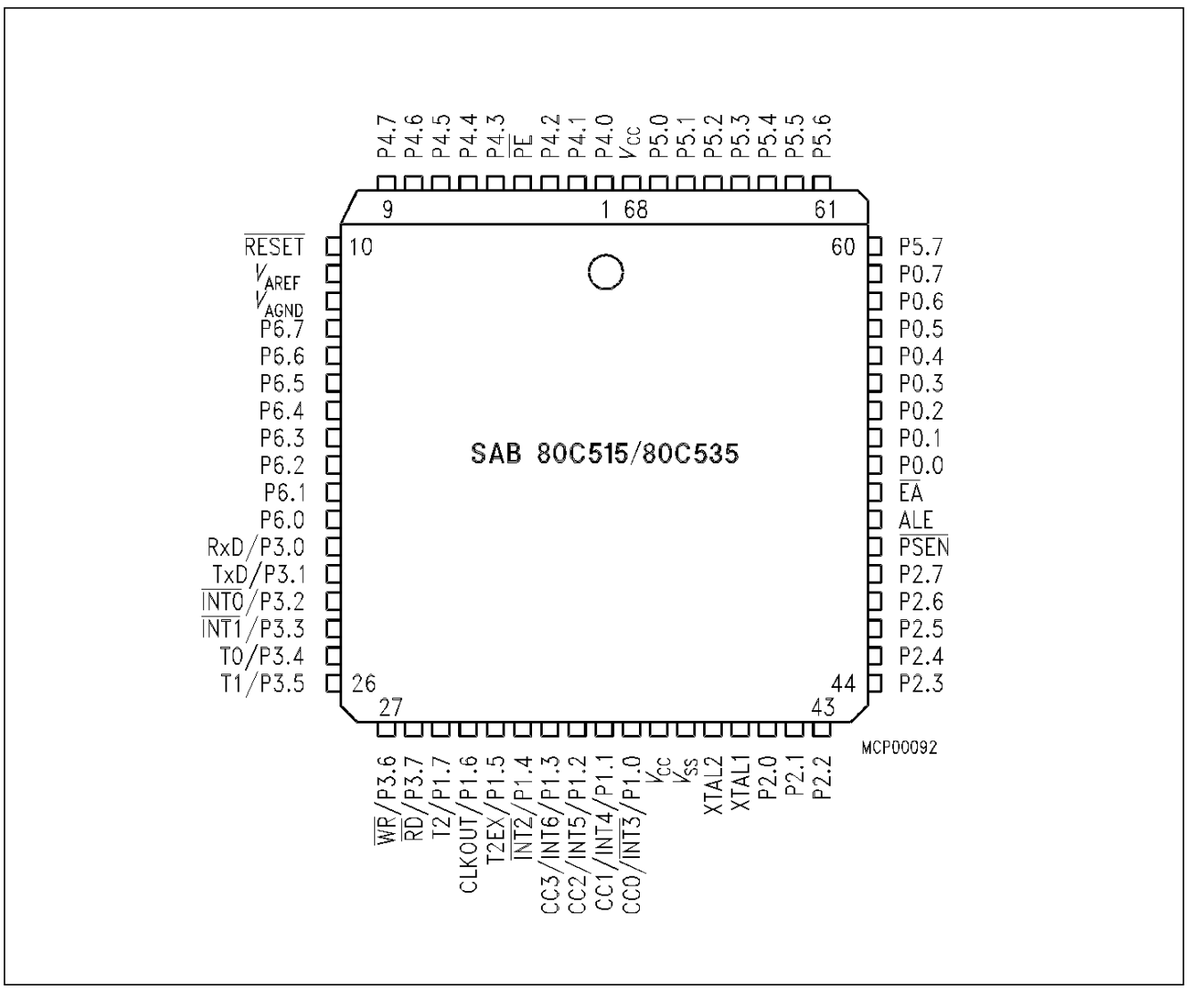
There are versions for 12, 16 and 20 MHz operation and for 16 MHz operation and for extended temperature ranges – 40 to 85 °C. Versions for extended temperature range – 40 to + 110 °C are available on request.


SAB 80C52/80C32
Watchdog
8-bit ADC
Port 6
Port 5
Port 4
Analog/
Digital
Input
I/O
I/O
RAM
256 x 8
T2
T0
T1
CPU
(80C51-Core)
8-bit
USART
ROM 8k x 8
Port 0
Port 1
Port 2
Port 3
I/O
I/O
I/O
I/O
MCB01712

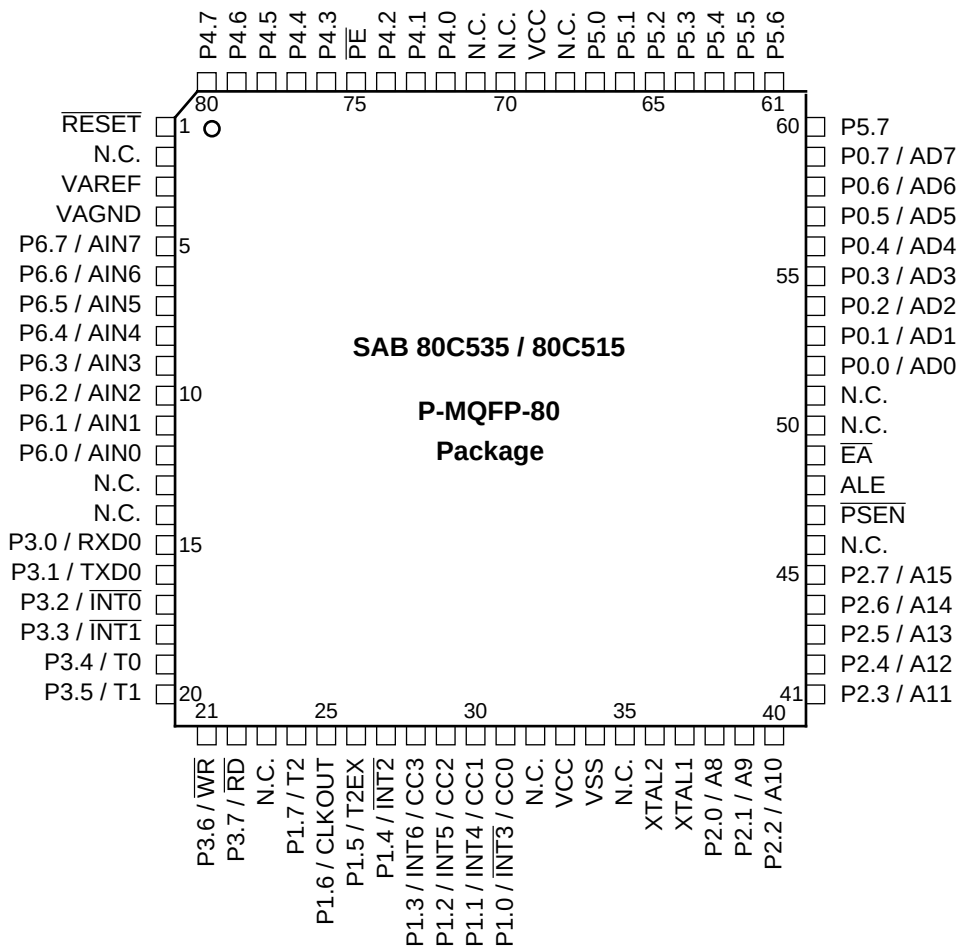
Ordering Information

Type	Ordering Code	Package	Description 8-Bit CMOS Microcontroller
SAB 80C515-N	Q 67120-DXXXX	P-LCC-68	with mask-programmable ROM, 12 MHz
SAB 80C535-N	Q 67120-C0508	P-LCC-68	for external memory, 12 MHz
SAB 80C515-N-T40/85	Q 67120-DXXXX	P-LCC-68	with mask-programmable ROM, 12 MHz ext. temperature – 40 to + 85 ˚C
SAB 80C535-N-T40/85	Q 67120-C0510	P-LCC-68	for external memory, 12 MHz ext. temperature – 40 to + 85 ˚C
SAB 80C515-16-N	Q 67120-DXXXX	P-LCC-68	with mask-programmable ROM, 16 MHz
SAB 80C535-16-N	Q 67120-C0509	P-LCC-68	for external memory, 16 MHz
SAB 80C535-16-N-T40/85	Q 67120-C0562	P-LCC-68	for external memory, 16 MHz ext. temperature – 40 to + 85 ˚C
SAB 80C535-20-N	Q 67120-C0778	P-LCC-68	for external memory, 20 MHz
SAB 80C535-M	Q67120-C0857	P-MQFP-80	for external memory, 12 MHz
SAB 80C515-M	Q67120-DXXXX	P-MQFP-80	with mask-programmable ROM, 12 MHz
SAB 80C535-M-T40/85	Q67120-C0937	P-MQFP-80	for external memory, 12 MHz ext. temperature – 40 to + 85 ˚C
SAB 80C515-M-T40/85	Q67120-DXXXX	P-MQFP-80	with mask-programmable ROM, 12 MHz ext. temperature – 40 to + 85 ˚C

Notes: Versions for extended temperature range – 40 to + 110 ˚C on request.
The ordering number of ROM types (DXXXX extension) is defined after program release (verification) of the customer.

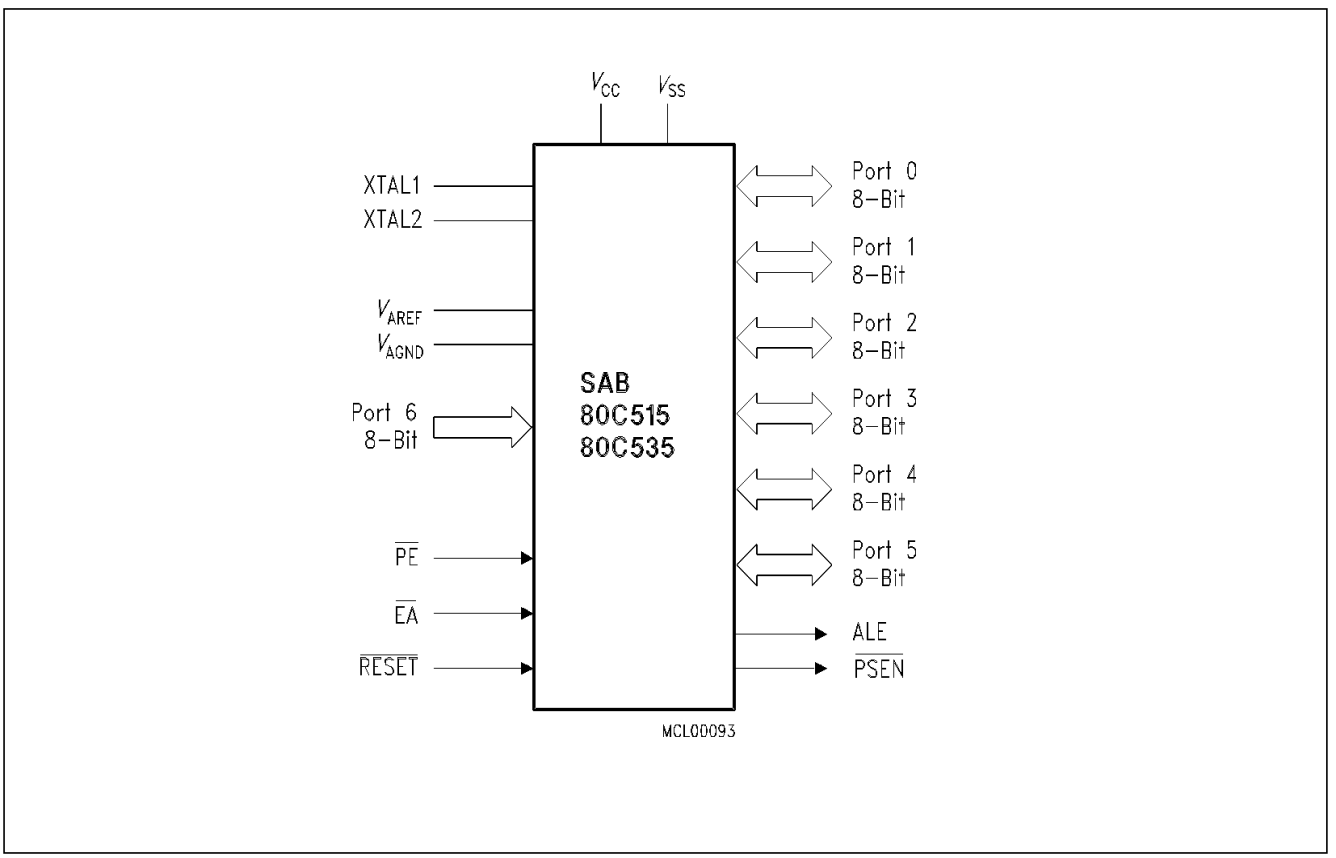


Pin Configuration
(P-LCC-68)



N.C. pins must not be connected.

Pin Configuration
(P-MQFP-80)



Logic Symbol

Pin Definitions and Functions

Symbol	Pin P-LCC-68	Pin P-MQFP-80	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	72-74, 76-80	I/O	**Port 4** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 4 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors.
$\overline{PE}$	4	75	I	**$\overline{\text{Power saving mode enable}}$** A low level on this pin enables the use of the power saving modes (idle mode and power-down mode). When $\overline{PE}$ is held on high level it is impossible to enter the power saving modes.
$\overline{RESET}$	10	1	I	**$\overline{\text{Reset}}$ pin** A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80C515. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11	3		**Reference voltage** for the A/D converter
V_{AGND}	12	4		**Reference ground** for the A/D converter
P6.7-P6.0	13-20	5-12		**Port 6** is an 8-bit undirectional input port. Port pins can be used for digital input if voltage levels simultaneously meet the specifications for high/low input voltages and for the eight multiplexed analog inputs of the A/D converter.

Pin Definitions and Functions (cont'd)

Symbol	Pin P-LCC-68	Pin P-MQFP-80	Input (I) Output (O)	Function
P3.0-P3.7	21-28	15-22	I/O	**Port 3** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 3 pins that have1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – R×D (P3.0): serial port's receiver data input (asynchronous) or data input/ output (synchronous) – T×D (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{INT0}$ (P3.2): interrupt 0 input/timer 0 gate control input – $\overline{INT1}$ (P3.3): interrupt 1 input/timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{WR}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{RD}$ (P3.7): the read control signal enables the external data memory to port 0

Pin Definitions and Functions (cont'd)

Symbol	Pin P-LCC-68	Pin P-MQFP-80	Input (I) Output (O)	Function
P1.7-P1.0	29-36	24-31	I/O	**Port 1** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL} in the DC characteristics) because of the internal pullup resistors. The port is used for the low-order address byte during program verification. Port 1 also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows: – $\overline{\text{INT3}}$/CC0 (P1.0): interrupt 3 input/ compare 0 output/capture 0 input – INT4/CC1 (P1.1): interrupt 4 input/ compare 1 output/capture 1 input – INT5/CC2 (P1.2): interrupt 5 input/ compare 2 output/capture 2 input – INT6/CC3 (P1.3): interrupt 6 input/ compare 3 output/capture 3 input – $\overline{\text{INT2}}$ (P1.4): interrupt 2 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input

Pin Definitions and Functions (cont'd)

Symbol	Pin P-LCC-68	Pin P-MQFP-80	Input (I) Output (O)	Function
XTAL2 XTAL1	39 40	36 37		**XTAL2** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. **XTAL1** Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times and rise/fall times specified in the AC characteristics must be observed.
P2.0-P2.7	41-48	38-45	I/O	**Port 2** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current ($I_{IL,}$ in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application it uses strong internal pullup resistors when issuing 1's. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register.

Pin Definitions and Functions (cont'd)

Symbol	Pin P-LCC-68	Pin P-MQFP-80	Input (I) Output (O)	Function
$\overline{\text{PSEN}}$	49	47	O	The **Program store enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. The signal remains high during internal program execution.
ALE	50	48	O	The **Address latch enable** output is used for latching the address into external memory during normal operation. It is activated every six oscillator periods, except during an external data memory access.
$\overline{\text{EA}}$	51	49	I	**External access enable** When held high, the SAB 80C515 executes instructions from the internal ROM as long as the PC is less than 8192. When held low, the SAB 80C515 fetches all instructions from external program memory. For the SAB 80C535 this pin must be tied low.
P0.0-P0.7	52-59	52-59	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1's. Port 0 also outputs the code bytes during program verification in the SAB 80C515. External pullup resistors are required during program verification.

Pin Definitions and Functions (cont'd)

Symbol	Pin P-LCC-68	Pin P-MQFP-80	Input (I) Output (O)	Function
P5.7-P5.0	60-67	60-67	I/O	**Port 5** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 5 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL} in the DC characteristics) because of the internal pullup resistors.
V_{CC}	37	33	–	**Supply voltage** during normal, idle, and power-down operation. Internally connected to pin 68.
V_{SS}	38	34	–	**Ground** (0 V)
V_{CC}	68	69	–	**Supply voltage** during normal, idle, and power-down operation. Internally connected to pin 37.
N. C.	–	2, 13, 14, 23, 32, 35, 46, 50, 51, 68, 70, 71	–	**Not connected** These pins of the P-MQFP-80 package must not be connected

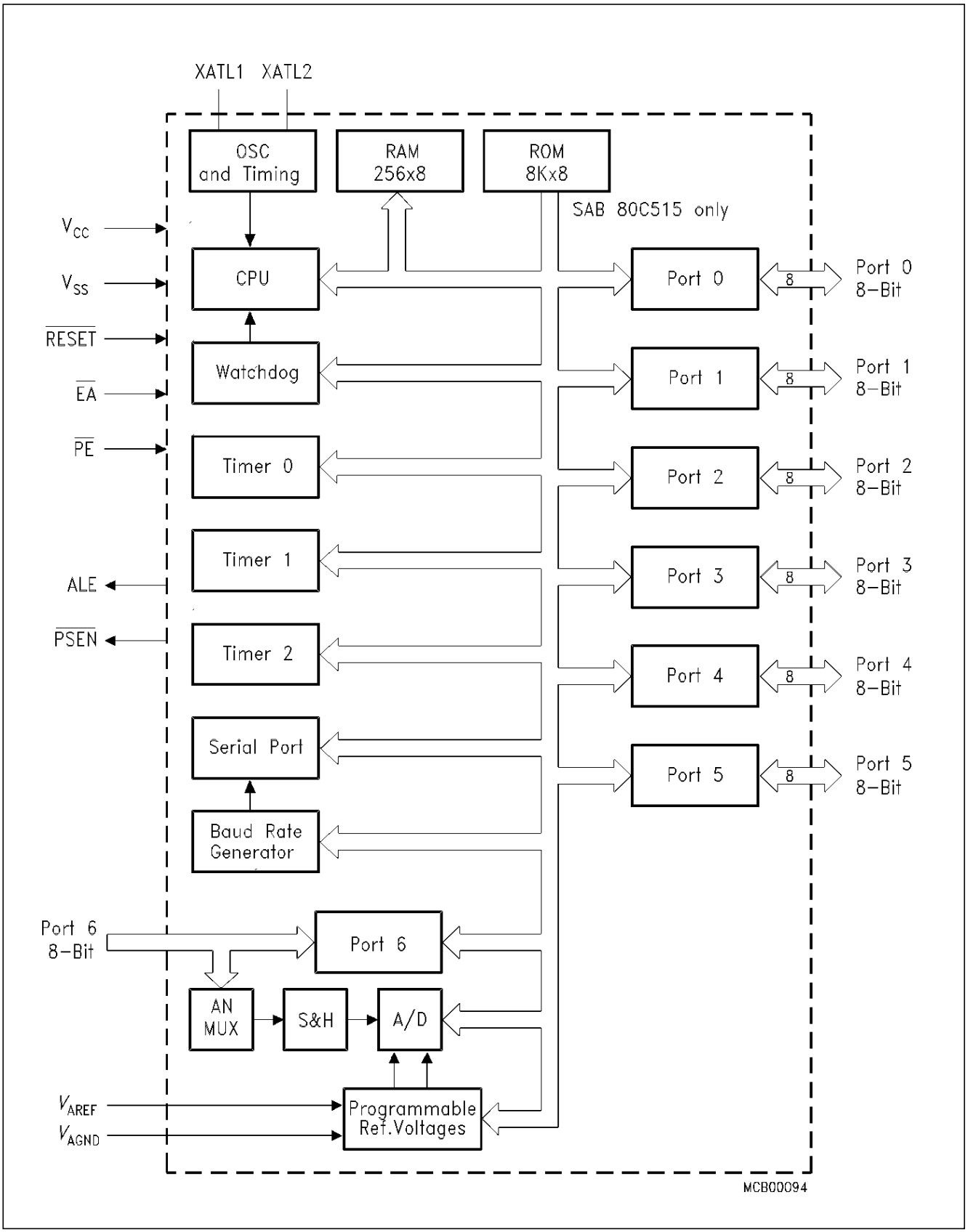


Figure 1
Block Diagram

Functional Description

The members of the SAB 80515 family of microcontrollers are:

- SAB 80C515: Microcontroller, designed in Siemens ACMOS technology, with 8 Kbyte factory mask-programmable ROM
- SAB 80C535: ROM-less version of the SAB 80C515
- SAB 80515: Microcontroller, designed in Siemens MYMOS technology, with 8 Kbyte factory mask-programmable ROM
- SAB 80535: ROM-less version of the SAB 80515

The SAB 80C535 is identical to the SAB 80C515, except that it lacks the on-chip ROM. In this data sheet the term "SAB 80C515" is used to refer to both the SAB 80C515 and SAB 80C535, unless otherwise noted.

Principles of Architecture

The architecture of the SAB 80C515 is based on the SAB 8051/SAB 80C51 microcontroller family. The following features of the SAB 80C515 are fully compatible with the SAB 80C51 features:

- Instruction set
- External memory expansion interface (port 0 and port 2)
- Full-duplex serial port
- Timer/counter 0 and 1
- Alternate functions on port 3
- The lower 128 bytes of internal RAM and the lower 4 Kbytes of internal ROM

The SAB 80C515 additionally contains 128 bytes of internal RAM and 4 Kbytes of internal ROM, which results in a total of 256 bytes of RAM and 8 Kbytes of ROM on-chip.
The SAB 80C515 has a new 16-bit timer/counter with a 2:1 prescaler, reload mode, compare and capture capability. It also contains at 16-bit watchdog timer, an 8-bit A/D converter with programmable reference voltages, two additional quasi-bidirectional 8-bit ports, one 8-bit input port for analog or digital signals, and a programmable clock output (f_{OSC}/12).
Furthermore, the SAB 80C515 has a powerful interrupt structure with 12 vectors and 4 programmable priority levels.
Figure 1 shows a block diagram of the SAB 80C515.

CPU

The SAB 80C515 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15 % three-byte instructions. With a 12 MHz crystal, 58 % of the instructions execute in 1.0 μs.

Memory Organization

The SAB 80C515 manipulates operands in the four memory address spaces described below: Figure 1 illustrates the memory address spaces of the SAB 80C515.

Program Memory

The SAB 80C515 has 8 Kbyte of on-chip ROM, while the SAB 80C535 has no internal ROM. The program memory can be externally expanded up to 64 Kbytes. If the $\overline{EA}$ pin is held high, the SAB 80C515 executes out of internal ROM unless the address exceeds 1FFFH. Locations 2000H through 0FFFFH are then fetched from the external program memory. If the $\overline{EA}$ pin is held now, the SAB 80C515 fetches all instructions from the external program memory. Since the SAB 80C535 has no internal ROM, pin $\overline{EA}$ must be tied low when using this component.

Data Memory

The data memory address space consists of an internal and an external memory space. The internal data memory is divided into three physically separate and distinct blocks:
the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128 byte special function register (SRF) area. While the upper 128 bytes of data memory and the SFR area share the same address locations, they are accessed through different addressing modes. The lower 128 bytes of data memory can be accessed through direct or register indirect addressing; the upper 128 bytes of RAM can be accessed through register indirect addressing; the special function registers are accessible through direct addressing.
Four 8-register banks, each bank consisting of eight 8-bit multi-purpose registers, occupy locations 0 through 1FH in the lower RAM area. The next 16 bytes, locations 20H through 2FH, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal data memory address space, and the stack depth can be expanded up to 256 bytes. The external data memory can be expanded up to 64 Kbytes and can be accessed by instructions that use a 16-bit or an 8-bit address.

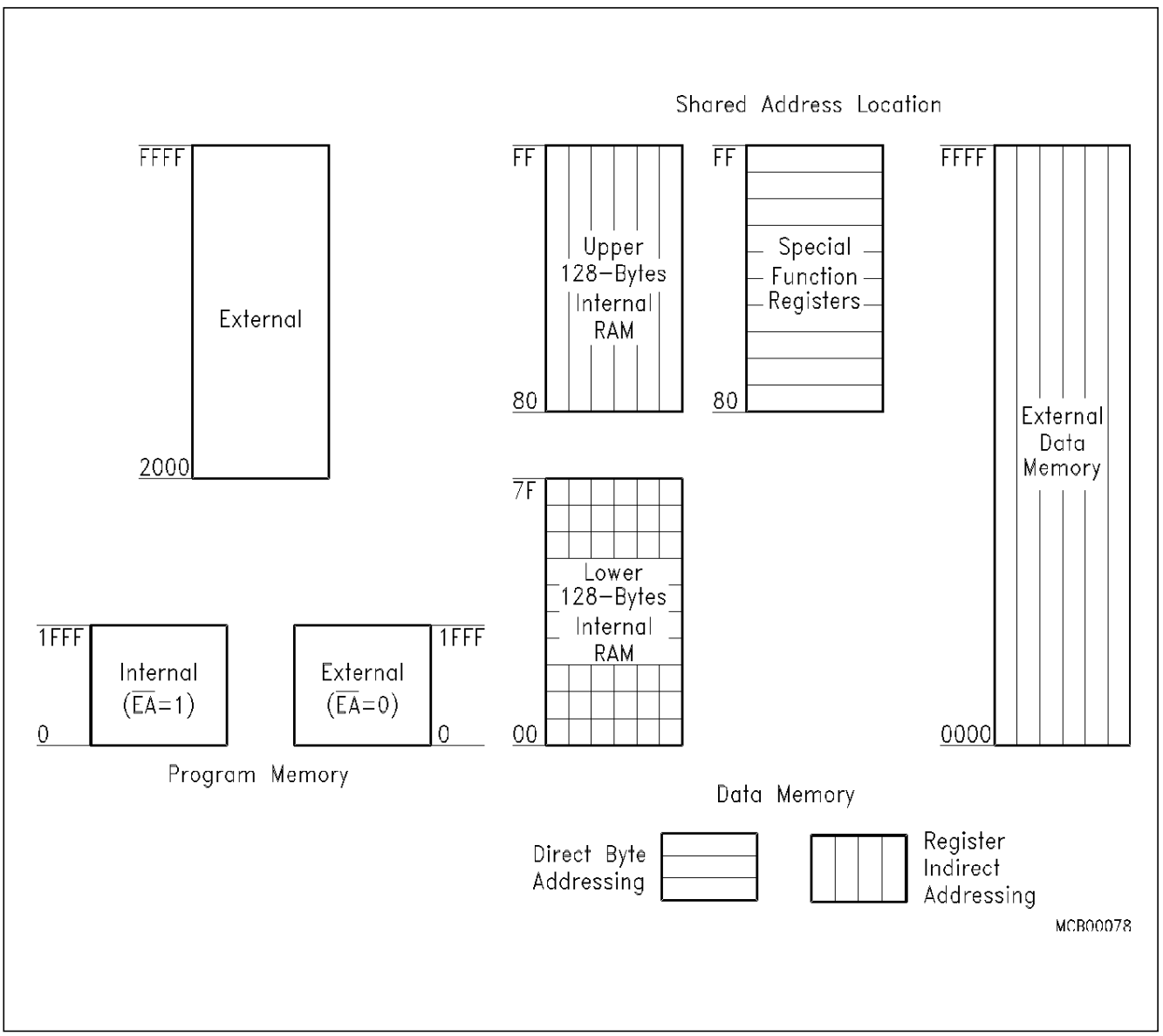


Figure 2
Memory Address Spaces

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function registers include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripherals. There are also 128 directly addressable bits within the SFR area. All special function registers are listed in table 1 and table 2.

In table 1 they are organized in numeric order of their addresses. In table 3 they are organized in groups which refer to the functional blocks of the SAB 80C515.

Table 1: Special Function Register

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80H	**P0** [1]	**0FFH**	**98H**	**SCON** [1]	**00H**
81H	SP	07H	99H	SBUF	XXH [2]
82H	DPL	00H	9AH	reserved	XXH [2]
83H	DPH	00H	9BH	reserved	XXH [2]
84H	reserved	XXH [2]	9CH	reserved	XXH [2]
85H	reserved	XXH [2]	9DH	reserved	XXH [2]
86H	reserved	XXH [2]	9EH	reserved	XXH [2]
87H	PCON	000X 0000B [2]	9FH	reserved	XXH [2]
88H	**TCON** [1]	**00H**	**A0H**	**P2** [1]	**0FFH**
89H	TMOD	00H	A1H	reserved	XXH [2]
8AH	TL0	00H	A2H	reserved	XXH [2]
8BH	TL1	00H	A3H	reserved	XXH [2]
8CH	TH0	00H	A4H	reserved	XXH [2]
8DH	TH1	00H	A5H	reserved	XXH [2]
8EH	reserved	XXH [2]	A6H	reserved	XXH [2]
8FH	reserved	XXH [2]	A7H	reserved	XXH [2]
90H	**P1** [1]	**0FFH**	**A8H**	**IEN0** [1]	**00H**
91H	reserved	XXH [2]	A9H	IP0	X000 0000B [2]
92H	reserved	XXH [2]	AAH	reserved	XXH [2]
93H	reserved	XXH [2]	ABH	reserved	XXH [2]
94H	reserved	XXH [2]	ACH	reserved	XXH [2]
95H	reserved	XXH [2]	ADH	reserved	XXH [2]
96H	reserved	XXH [2]	AEH	reserved	XXH [2]
97H	reserved	XXH [2]	AFH	reserved	XXH [2]

[1] Bit-addressable Special Function Register
[2] X means that the value is indeterminate and the location is reserved

Table 1:Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
B0H	**P3** 1)	**0FFH**	**D0H**	**PSW** 1)	**00H**
B1H	reserved	XXH 2)	D1H	reserved	XXH 2)
B2H	reserved	XXH 2)	D2	reserved	XXH 2)
B3H	reserved	XXH 2)	D3H	reserved	XXH 2)
B4H	reserved	XXH 2)	D4H	reserved	XXH 2)
B5H	reserved	XXH 2)	D5H	reserved	XXH 2)
B6H	reserved	XXH 2)	D6H	reserved	XXH 2)
B7H	reserved	XXH 2)	D7H	reserved	XXH 2)
B8H	**IEN1** 1)	**00H**	**D8H**	**ADCON**1)	**00X0 0000B** 2)
B9H	IP1	XX00 0000B 2)	D9H	ADDAT	00H
BAH	reserved	XXH 2)	DAH	DAPR	00H
BBH	reserved	XXH 2)	DBH	P6	XXH 2)
BCH	reserved	XXH 2)	DCH	reserved	XXH 2)
BDH	reserved	XXH 2)	DDH	reserved	XXH 2)
BSH	reserved	XXH 2)	DEH	reserved	XXH 2)
BFH	reserved	XXH 2)	DFH	reserved	XXH 2)
C0H	**IRCON** 1)	**00H**	**E0H**	**ACC** 1)	**00H**
C1H	CCEN	00H	E1H	reserved	XXH 2)
C2H	CCL1	00H	E2H	reserved	XXH 2)
C3H	CCH1	00H	E3H	reserved	XXH 2)
C4H	CCL2	00H	E4H	reserved	XXH 2)
C5H	CCH2	00H	E5H	reserved	XXH 2)
C6H	CCL3	00H	E6H	reserved	XXH 2)
C7H	CCH3	00H	E7H	reserved	XXH 2)
C8H	**T2CON** 1)	**00H**	**E8H**	**P4** 1)	**0FFH**
C9H	reserved	XXH 2)	E9H	reserved	XXH 2)
CAH	CRCL	00H	EAH	reserved	XXH 2)
CBH	CRCH	00H	EBH	reserved	XXH 2)
CCH	TL2	00H	ECH	reserved	XXH 2)
CDH	TH2	00H	EDH	reserved	XXH 2)
CEH	reserved	XXH 2)	EEH	reserved	XXH 2)
CFH	reserved	XXH 2)	EFH	reserved	XXH 2)

1) Bit-addressable Special Function Register
2) X means that the value is indeterminate and the location is reserved

Table 1:Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
F0H	**B** [1]	**00H**	**F8H**	**P5** [1]	**0FFH**
F1H	reserved	XXH [2]	F9H	reserved	XXH [2]
F2H	reserved	XXH [2]	FAH	reserved	XXH [2]
F3H	reserved	XXH [2]	FBH	reserved	XXH [2]
F4H	reserved	XXH [2]	FCH	reserved	XXH [2]
F5H	reserved	XXH [2]	FDH	reserved	XXH [2]
F6H	reserved	XXH [2]	FEH	reserved	XXH [2]
F7H	reserved	XXH [2]	FFH	reserved	XXH [2]

[1] Bit-addressable Special Function Register
[2] X means that the value is indeterminate and the location is reserved

Table 2: Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**0E0H** 1)	00H
	B	B-Register	**0F0H** 1)	00H
	DPH	Data Pointer, High Byte	83H	00H
	DPL	Data Pointer, Low Byte	82H	00H
	PSW	Program Status Word Register	**0D0H** 1)	00H
	SP	Stack Pointer	81H	07H
A/D-Converter	ADCON	A/D Converter Control Register	**0D8H** 1)	00X0 0000B 2)
	ADDAT	A/D Converter Data Register	0D9H	00H
	DAPR	D/A Converter Program Register	0DAH	00H
Interrupt System	EN0	Interrupt Enable Register 0	**0A8H** 1)	00H
	IEN1	Interrupt Enable Register 1	**0B8H** 1)	00H
	IP0	Interrupt Priority Register 0	0A9H	00H
	IP1	Interrupt Priority Register 1	0B9H	X000 0000B 2)
	IRCON	Interrupt Request Control Register	**0C0H** 1)	XX00 0000B 3)
	TCON 2)	Timer Control Register	**88H** 1)	00H
	T2CON 2)	Timer 2 Control Register	**0C8H** 1)	00H
				00H
Compare/ Capture-Unit (CCU)	CCEN	Comp./Capture Enable Reg.	0C1H	00H
	CCH1	Comp./Capture Reg. 1, High Byte	0C3H	00H
	CCH2	Comp./Capture Reg. 2, High Byte	0C5H	00H
	CCH3	Comp./Capture Reg. 3, High Byte	0C7H	00H
	CCL1	Comp./Capture Reg. 1, Low Byte	0C2H	00H
	CCL2	Comp./Capture Reg. 2, Low Byte	0C4H	00H
	CCL3	Comp./Capture Reg. 3, Low Byte	0C6H	00H
	CRCH	Com./Rel./Capt. Reg. High Byte	0CBH	00H
	CRCL	Com./Rel./Capt. Reg. Low Byte	0CAH	00H
	TH2	Timer 2, High Byte	0CDH	00H
	TL2	Timer 2, Low Byte	0CCH	00H
	T2CON	Timer 2 Control Register	**0C8H** 1)	00H

1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

3) X means that the value is indeterminate and the location is reserved

Table 2: Special Function Registers- Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Ports	P0	Port 0	**80H** 1)	0FFH
	P1	Port 1	**90H** 1)	0FFH
	P2	Port 2	**0A0H** 1)	0FFH
	P3	Port 3	**0B0H** 1)	0FFH
	P4	Port 4	**0E8H** 1)	0FFH
	P5	Port 5	**0F8H** 1)	0FFH
	P6	Port 6, Analog/Digital Input	0DBH	
Pow.Sav.Modes	PCON	Power Control Register	87H	000X 0000B 2)
Serial Channels	ADCON 2)	A/D Converter Control Reg.	**0D8H** 1)	00X0 0000B 2)
	PCON 2)	Power Control Register	87H	000X 0000B 2)
	SBUF	Serial Channel Buffer Reg.	99H	0XXH 3)
	SCON	Serial Channel Control Reg.	**98H** 1)	00H
Timer 0/ Timer 1	TCON	Timer Control Register	**88H** 1)	00H
	TH0	Timer 0, High Byte	8CH	00H
	TH1	Timer 1, High Byte	8DH	00H
	TL0	Timer 0, Low Byte	8AH	00H
	TL1	Timer 1, Low Byte	8BH	00H
	TMOD	Timer Mode Register	89H	00H
Watchdog	IEN0 2)	Interrupt Enable Register 0	**0A8H** 1)	00H
	IEN1 2)	Interrupt Enable Register 1	**0B8H** 1)	00H
	IP0 2)	Interrupt Priority Register 0	0A9H	X000 0000B 2)
	IP1 2)	Interrupt Priority Register 1	0B9H	XX00 0000B 3)

1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

3) X means that the value is indeterminate and the location is reserved

I/O Ports

The SAB 80C515 has six 8-bit I/O ports and one 8-bit input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pullup resistors. That means, when configured as inputs, ports 1 to 5 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET. Ports 1 and 3 are provided for several alternate functions, as listed below:

Port	Symbol	Function
P1.0	$\overline{\text{INT3}}$/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	INT6/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	$\overline{\text{INT2}}$	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external count or gate input
P3.0	R×D	Serial port's receiver data input (asynchronous) or data input/output (synchronous)
P3.1	T×D	Serial port's transmitter data output (asynchronous) or clock output (synchronous)
P3.2	$\overline{\text{INT0}}$	External interrupt 0 input, timer 0 gate control
P3.3	$\overline{\text{INT1}}$	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	T1	Timer 1 external counter input
P3.6	$\overline{\text{WR}}$	External data memory write strobe
P3.7	$\overline{\text{RD}}$	External data memory read strobe

The SAB 80C515 has dual-purpose input port. As the ANx lines in the SAB 80515 (NMOS version), the eight port lines at port 6 can be used as analog inputs. But if the input voltages at port 6 meet the specified digital input levels (V_{IL} and V_{IH}), the port can also be used as digital input port. Reading the special function register P6 allows the user to input the digital values currently applied to the port pins. It is not necessary to select these modes by software; the voltages applied at port 6 pins can be converted to digital values using the A/D converter and at the same time the pins can be read via SFR P6.
It must be noted, however, that the results in port P6 bits will be indeterminate if the levels at the corresponding pins are not within their respective V_{IL}/ V_{IH} specifications. Furthermore, it is not possible to use port P6 as output lines. Special function register P6 is located at address 0DBH.

Timer/Counters

The SAB 80C515 contains three 16-bit timers/counters which are useful in many applications for timing and counting. The input clock for each timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

– Timer/Counter 0 and 1

These timers/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto-reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; Timer/counter 1 in this mode holds its count.

External inputs $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

– Timer/Counter 2

Timer/counter 2 of the SAB 80C515 is a 16-bit timer/counter with several additional features. It offers a 2:1 prescaler, a selectable gate function, and compare, capture and reload functions. Corresponding to the 16-bit timer register there are four 16-bit capture/compare registers, one of them can be used to perform a 16-bit reload on a timer overflow or external event. Each of these registers corresponds to a pin of port 1 for capture input/compare output.
Figure 3 shows a block diagram of timer/counter 2.

Reload

A 16-bit reload can be performed with the 16-bit CRC register consisting of CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer 2 overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

Capture

This feature permits saving the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value in timer 2 registers TL2 and TH2 into a dedicated capture register:

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 registers. If the count value in the timer 2 registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to a low level when timer 2 overflows.

Mode 1: The transition of the output signal can be determined by software. A timer 2 overflow causes no output change

.

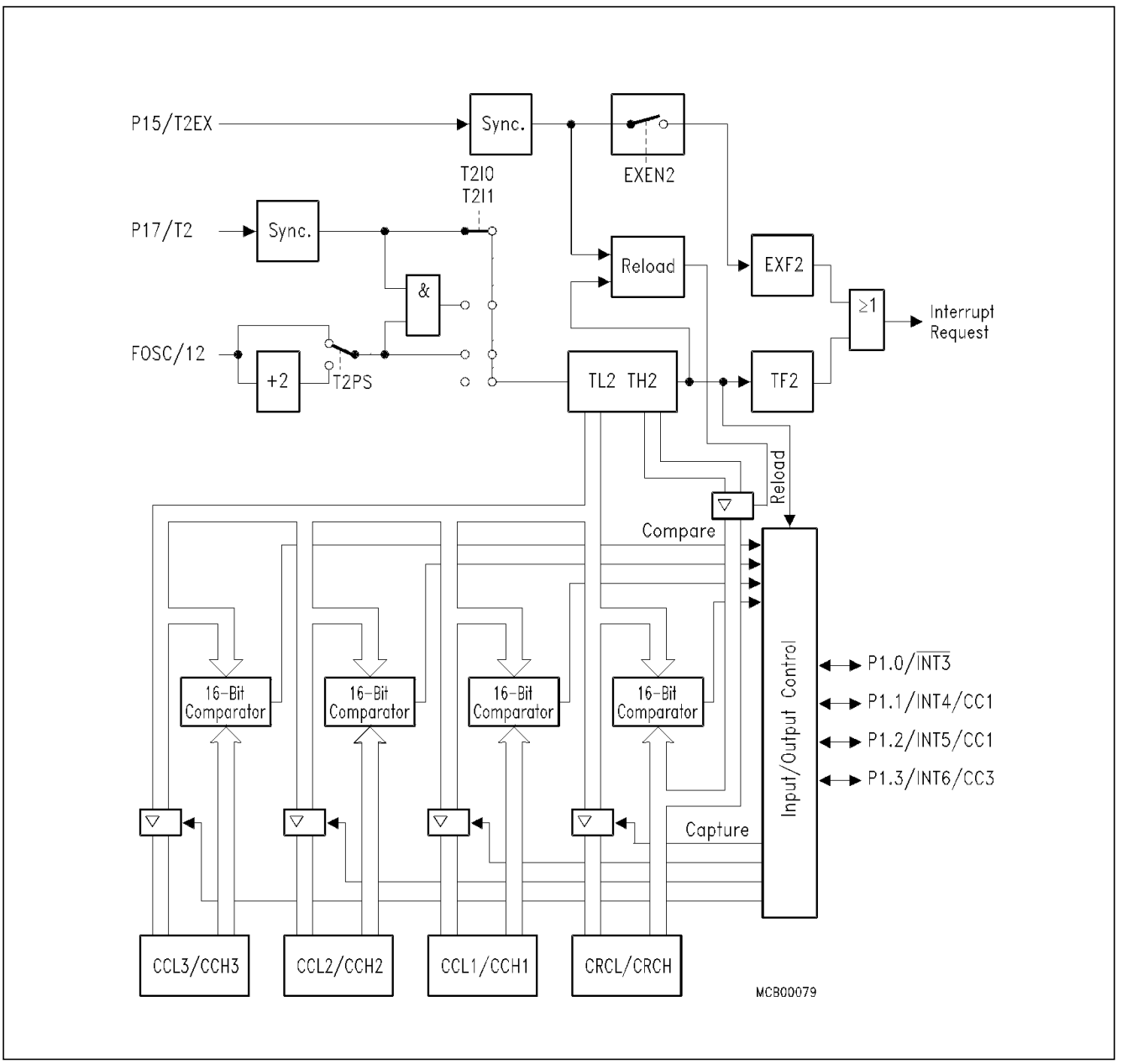


Figure 3
Block Diagram of Timer/Counter 2

Serial Port

The serial port of the SAB 80C515 enables full duplex communication between microcontrollers or between microcontroller and peripheral devices.
The serial port can operate in 4 modes:

Mode 0: Shift register mode. Serial data enters and exits through R×D. T×D outputs the shift clock. 8-bits are transmitted/received: 8 data bits (LSB first).
The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 10-bits are transmitted (through R×D) or received (through T×D): a start bit (0), 8 data bits (LSB first), and a stop bit (1). The baud rate is variable.

Mode 2: 11-bits are transmitted (through R×D) or received (through T×D): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1).
The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 11-bits are transmitted (through T×D) or received (through R×D): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is identical to mode 2 except for the baud rate. The baud rate in mode 3 is variable.

The variable baud rates in modes 1 and 3 can be generated by timer 1 or an internal baud rate generator.

A/D Converter

The 8-bit A/D converter of the SAB 80C515 has eight multiplexed analog inputs (Port 6) and uses the successive approximation method.
There are three characteristic time frames in a conversion cycle (see A/D converter characteristics): the conversion time t_C, which is the time required for one conversion; the sample time t_S which is included in the conversion time and is measured from the start of the conversion; the load time t_L, which in turn is part of the sample time and also is measured from the conversion start.
Within the load time t_L, the analog input capacitance C_I must be loaded to the analog inpult voltage level. For the rest of the sample time t_S, after the load time has passed, the selected analog input must be held constant. During the rest of the conversion time t_C the conversion itself is actually performed. Conversion can be programmed to be single or continuous; at the end of a conversion an interrupt can be generated.

A unique feature is the capability of internal reference voltage programming. The internal reference voltages $V_{IntAREF}$ and $V_{IntAGND}$ for the A/D converter both are programmable to one of 16 steps with respect to the external reference voltages. This feature permits a conversion with a smaller internal reference voltage range to gain a higher resolution.
In addition, the internal reference voltages can easily be adapted by software to the desired analog input voltage range.

Figure 4 shows a block diagram of the A/D converter.

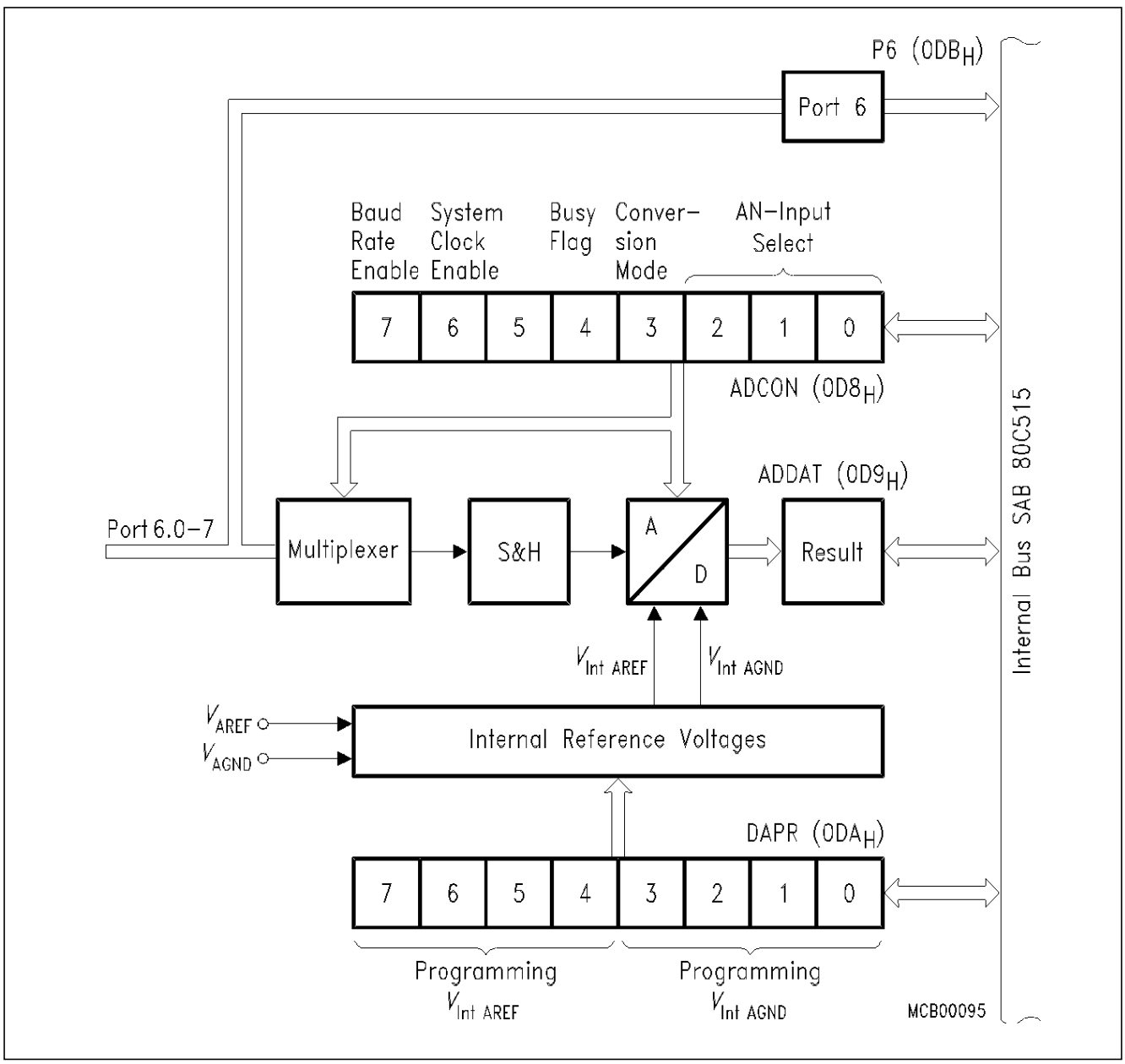


Figure 4
Block Diagram of the A/D Converter

Interrupt Structure

The SAB 80C515 has 12 interrupt vectors with the following vector addresses and request flags:

Table 3
Interrupt Sources and Vectors

Source (Request Flags)	Vector Address	Vector
IE0	0003H	External interrupt 0
TF0	000BH	Timer 0 interrupt
IE1	0013H	External interrupt 1
TF1	001BH	Timer 1 interrupt
RI + TI	0023H	Serial port interrupt
TF2 + EXF2	002BH	Timer 2 interrupt
IADC	0043H	A/D converter interrupt
IEX2	004BH	External interrupt 2
IEX3	0053H	External interrupt 3
IEX4	005BH	External interrupt 4
IEX5	0063H	External interrupt 5
IEX6	006BH	External interrupt 6

Each interrupt vector can be individually enabled/disabled. The minimum response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

Figure 5 shows the interrupt request sources.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 3 or 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs. Each pair can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1.

Figure 6 shows the priority level structure.

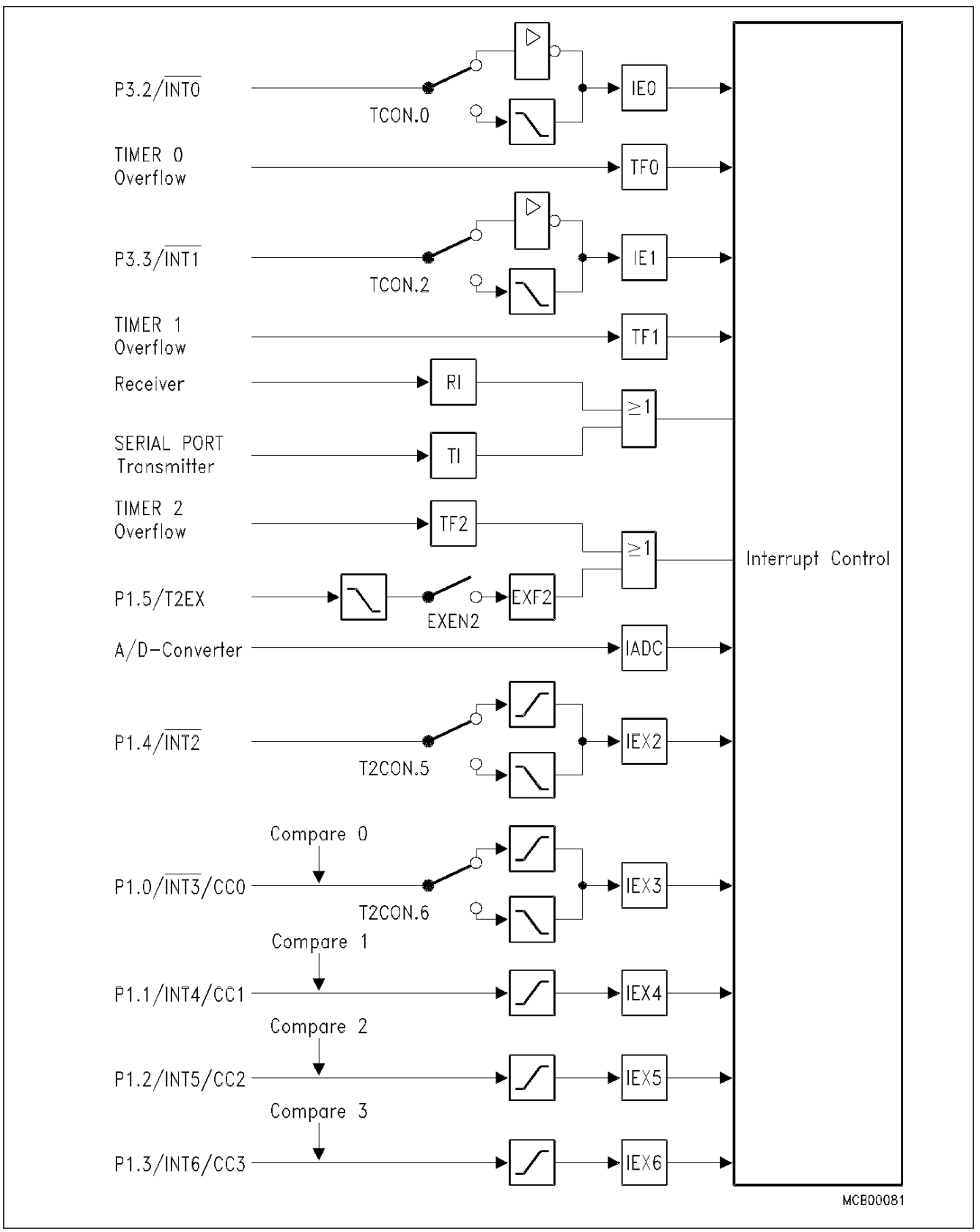


Figure 5
Interrupt Request Sources

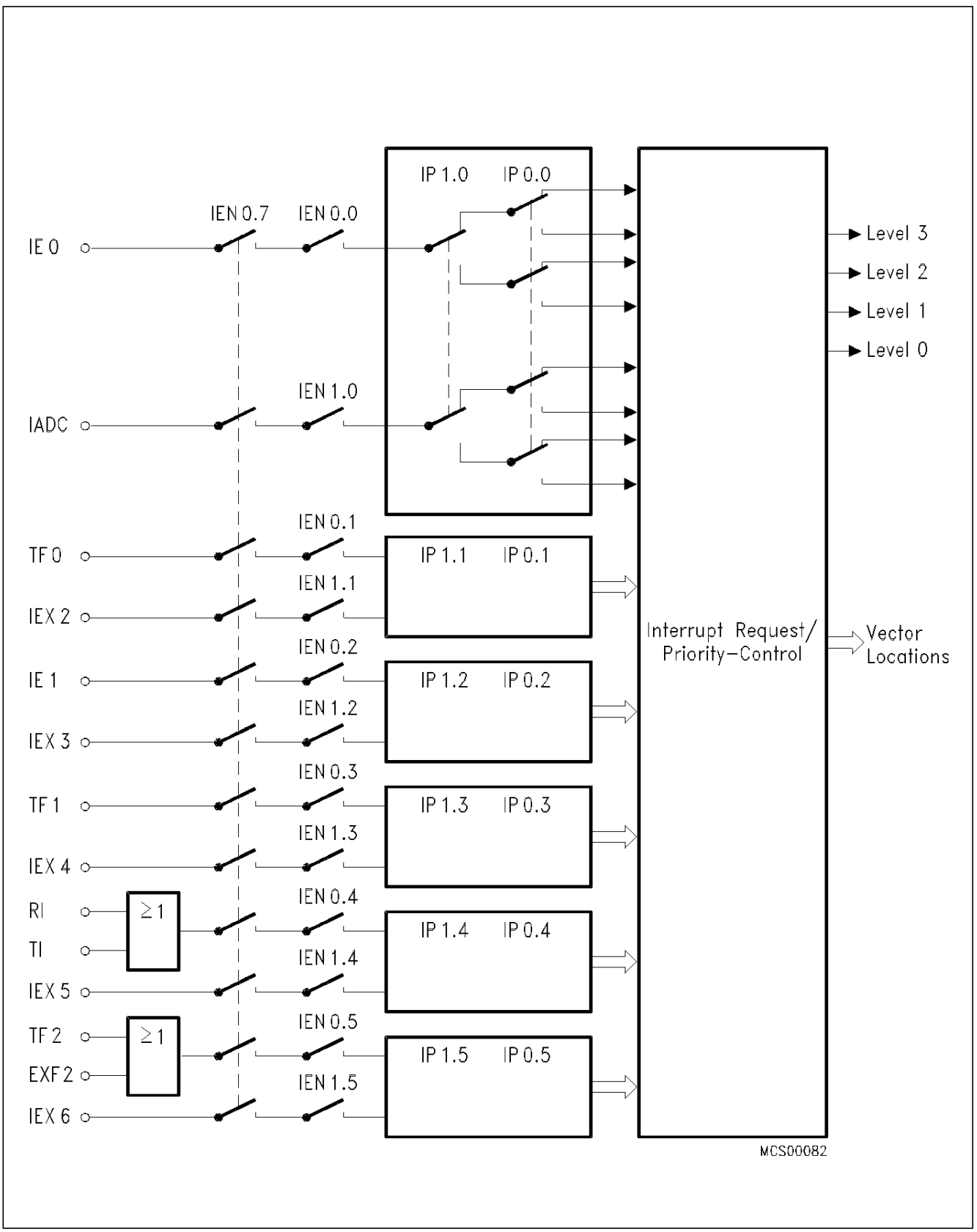


Figure 6
Interrupt Priority Level Structure

Watchdog Timer

This feature is provided as a means of graceful recovery from a software upset. After an external reset, the watchdog timer is cleared and stopped. It can be started and cleared by software, but it cannot be stopped during active mode of the device. If the software fails to clear the watchdog timer at least every 65532 machine cycles (about 65 ms if a 12 MHz oscillator frequency is used), an internal reset will be initiated. The reset cause (external reset or reset caused by the watchdog) can be examined by software. To clear the watchdog, two bits in two different special function registers must be set by two consecutive instructions (bits IEN0.6 and IEN1.6). This is done to prevent the watchdog from being cleared by unexpected opcodes.

It must be noted, however, that the watchdog timer is halted during the idle mode and power-down mode of the processor (see section "Power Saving Modes" below).
Therefore, it is possible to use the idle mode in combination with the watchdog timer function. But even the watchdog timer cannot reset the device when one of the power saving modes has been is entered accidentally.
For these reasons several precautions are taken against unintentional entering of the power-down or idle mode (see below).

Power Saving Modes

The ACMOS technology of the SAB 80C515 allows two new power saving modes of the device: The idle mode and the power-down mode. These modes replace the power-down supply mode via pin V_{PD} of the SAB 80515 (NMOS). The SAB 80C515 is supplied via pins V_{CC} also during idle and power-down operation.
However, there are applications where unintentional entering of these power saving modes must be absolutely avoided. Such critical applications often use the watchdog timer to prevent the system from program upsets. Then accidental entering of the power saving modes would even stop the watchdog timer and would circumvent the watchdog timer's task of system protection.

Thus, the SAB 80C515 has an extra pin that allows it to disable both of the power saving modes. When pin $\overline{PE}$ is held high, idle mode and power-down mode are completely disabled and the instruction sequences that are used for entering these modes (see below) will NOT affect the normal operations of the device. When $\overline{PE}$ is held low, the use of the idle mode and power-down mode is possible as described in the following sections.

Pin $\overline{PE}$ has a weak internal pullup resistor. Thus, when left open, the power saving modes are disabled.

The Special Function Register PCON

In the NMOS version SAB 80515 the SFR PCON (address 87H) contains only bit SMOD; in the CMOS version SAB 80C515 there are more bits used (see table 4).
The bits PDE, PDS and IDLE, IDLS select the power-down mode or the idle mode, respectively, when the use of the power saving modes is enabled by pin $\overline{PE}$ (see next page).

If the power-down mode and the idle mode are set at the same time, power-down takes precedence.
Furthermore, register PCON contains two general purpose flags. For example, the flag bits GF0 and GF1 can be used to give an indication if an interrupt occurred during normal operation or during an idle. Then an instruction that activates Idle can also set one or both flag bits. When idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.
The reset value of PCON is 000X0000B.

Table 4
SFR PCON (87H)

SMOD	PDS	IDLS	–	GF1	GF0	PDE	IDLE	87H
7	6	5	4	3	2	1	0	

Symbol	Position	Function
SMOD	PCON.7	When set, the baud rate of the serial channel in mode 1, 2, 3 is doubled.
PDS	PCON.6	Power-down start bit. The instruction that sets the PDS flag bit is the last instruction before entering the power-down mode.
IDLS	PCON.5	Idle start bit. The instruction that sets the IDLS flag bit is the last instruction before entering the idle mode.
–	PCON.4	Reserved
GF1	PCON.3	General purpose flag
GF0	PCON.2	General purpose flag
PDE	PCON.1	Power-down enable bit. When set, starting of the power-down mode is enabled.
IDLE	PCON.0	Idle mode enable bit. When set, starting of the idle mode is enabled.

Idle Mode

In the idle mode the oscillator of the SAB 80C515 continues to run, but the CPU is gated off from the clock signal. However, the interrupt system, the serial port, the A/D converter, and all timers with the exception of the watchdog timer are further provided with the clock. The CPU status is preserved in its entirety: the stack pointer, program counter, program status word, accumulator, and all other registers maintain their data during idle mode.

The reduction of power consumption, which can be achieved by this feature depends on the number of peripherals running.

If all timers are stopped and the A/D converter and the serial interface are not running, the maximum power reduction can be achieved. This state is also the test condition for the idle mode I_{CC} (see DC characteristics, note 5).

So the user has to take care which peripheral should continue to run and which has to be stopped during idle mode. Also the state of all port pins – either the pins controlled by their latches or controlled by their secondary functions – depends on the status of the controller when entering idle mode.

Normally the port pins hold the logical state they had at the time idle mode was activated. If some pins are programmed to serve their alternate functions they still continue to output during idle mode if the assigned function is on. This applies to the compare outputs as well as to the clock output signal or to the serial interface in case it cannot finish reception or transmission during normal operation. The control signals ALE and $\overline{\text{PSEN}}$ hold at logic high levels (see table 5).

Table 5
Status of External Pins During Idle and Power-Down Mode

	Last instruction executed from internal code memory		**Last instruction executed from external code memory**	
Outputs	**Idle**	**Power-down**	**Idle**	**Power-down**
ALE	High	Low	High	Low
PSEN	High	Low	High	Low
PORT 0	Data	Data	Float	Float
PORT 1	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output
PORT 2	Data	Data	Address	Data
PORT 3	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output
PORT 4	Data	Data	Data	Data
PORT 5	Data	Data	Data	Data

As in normal operation mode, the ports can be used as inputs during idle mode. Thus a capture or reload operation can be triggered, the timers can be used to count external events, and external interrupts will be detected.

The idle mode is a useful feature which makes it possible to "freeze" the processor's status – either for a predefined time, or until an external event reverts the controller to normal operation, as discussed below. The watchdog timer is the only peripheral which is automatically stopped during idle mode. If it were not disabled on entering idle mode, the watchdog timer would reset the controller, thus abandoning the idle mode.

When idle mode is used, pin $\overline{PE}$ must be held on low level. The idle mode is then entered by two consecutive instructions. The first instruction sets the flag bit IDLE (PCON.0) and must not set bit IDLS (PCON.5), the following instruction sets the start bit IDLS (PCON.5) and must not set bit IDLE (PCON.0). The hardware ensures that a concurrent setting of both bits, IDLE and IDLS, does not initiate the idle mode. Bits IDLE and IDLS will automatically be cleared after being set. If one of these register bits is read the value that appears is 0 (see table 4). This double instruction is implemented to minimize the chance of an unintentional entering of the idle mode which would leave the watchdog timer's task of system protection without effect.

Note that PCON is not a bit-addressable register, so the above mentioned sequence for entering the idle mode is obtained by byte-handling instructions, as shown in the following example:

```
ORL     PCON,#00000001B     ;Set bit IDLE, bit IDLS must not be set
ORL     PCON,#00100000B     ;Set bit IDLS, bit IDLE must not be set
```

The instruction that sets bit IDLS is the last instruction executed before going into idle mode.

There are two ways to terminate the idle mode:

– The idle mode can be terminated by activating any enable interrupt. This interrupt will be serviced and normally the instruction to be executed following the RETI instruction will be the one following the instruction that sets the bit IDLS.

– The other way to terminate the idle mode, is a hardware reset. Since the oscillator is still running, the hardware reset must be held active only for two machine cycles for a complete reset.

Power-Down Mode

In the power-down mode, the on-chip oscillator is stopped. Therefore all functions are stopped; only the contents of the on-chip RAM and the SFR's are maintained.The port pins controlled by their port latches output the values that are held by their SFR's.
The port pins which serve the alternate output functions show the values they had at the end of the last cycle of the instruction which initiated the power-down mode; when the clockout signal (CLKOUT, P1.6) is enabled, it will stop at low level. ALE and $\overline{PSEN}$ hold at logic low level (see table 5).

To enter the power-down mode the pin $\overline{PE}$ must be on low level. The power-down mode then is entered by two consecutive instructions. The first instruction has to set the flag bit PDE (PCON.1) and must not set bit PDS (PCON.6), the following instruction has to set the start bit PDS (PCON.6) and must not set bit PDE (PCON.1). The hardware ensures that a concurrent setting of both bits, PDE and PDS, does not initiate the power-down mode. Bits PDE and PDS will automatically be cleared after having been set and the value shown by reading one of these bits is always 0 (see table 4). This double instruction is implemented to minimize the chance of unintentionally entering the power-down mode which could possibly "freeze" the chip's activity in an undesired status.

Note that PCON is not a bit-addressable register, so the above mentioned sequence for entering the power-down mode is obtained by byte-handling instructions, as shown in the following example:

```
ORL     PCON,#00000010B   ;Set bit PDE, bit PDS must not be set
ORL     PCON,#01000000B   ;Set bit PDS, bit PDE must not be set
```

The instruction that sets bit PDS is the last instruction executed before going into power-down mode.

The only exit from power-down mode is a hardware reset. Reset will redefine all SFR's, but will not change the contents of the internal RAM.

In the power-down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the power- down mode is invoked, and that V_{CC} is restored to its normal operating level, before the power-down mode is terminated. The reset signal that terminates the power-down mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (similar to power-on reset).

Differences in Pin Assignments of the SAB 80C515 and SAB 80515

Since the SAB 80C515 is designed in CMOS technology, this device requires no V_{BB} pin, because the die's substrate is internally connected to V_{CC}.

Furthermore, the RAM backup power supply via pin V_{PD} is replaced by the software- controlled power-down mode and power supply via V_{CC}.

Therefore, pins V_{BB} and V_{PD} of the NMOS version SAB 80515 are used for other functions in the SAB 80C515.

Pin 4 (the former pin V_{PD}) is the new $\overline{PE}$ pin which enables the use of the power saving modes.

Pin 37 (the former pin V_{BB}) becomes an additional V_{CC} pin. Thus, it is possible to insert a decoupling capacitor between pin 37 (V_{CC}) and pin 38 (V_{SS}) very close to the device, thereby avoiding long wiring and reducing the voltage distortion resulting from high dynamic current peaks.

There is a difference between the NMOS and CMOS version concerning the clock circuitry. When the device is driven from an external source, pin XTAL2 must be driven by the clock signal; pin XTAL1, however, must be left open in the SAB 80C515 (must be tied low in the NMOS version). When using the oscillator with a crystal there is no difference in the circuitry.

Thus, due to its pin compatibility the SAB 80C515 normally substitutes any SAB 80515 without redesign of the user's printed circuit board, but the user has to take care that the two V_{CC} pins are hardwired on-chip. In any case, it is recommended that power is supplied on both V_{CC} pins of the SAB 80C515 to improve the power supply to the chip.
If the power saving modes are to be used, pin $\overline{PE}$ must be tied low, otherwise these modes are disabled.

Instruction Set

The SAB 80C515 / 83C535 has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function Registers, Interrupt Vectors and Assembler Directives.

Literature Information

Title	Ordering No.
Microcontroller Family SAB 8051 Pocket Guide	B158-H6579-X-X-7600

Absolute Maximum Ratings

Ambient temperature under bias	
SAB 80C515	0 to 70 °C
SAB 80C515-T3	– 40 to 85 °C
Storage temperature	– 65 to 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS})	– 0.5 to 6.5 V
Voltage on any pin with respect to ground (V_{SS})	– 0.5 to V_{CC} + 0.5 V
Input current on any pin during overload condition	– 10 mA to + 10 mA
Absolute sum of all input currents during overload condition	|100 mA|
Power disipation	2 W

Note *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exeed the values defined by the absolute maximum ratings.*

DC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB 80C515/80C535
T_A = – 40 to 85 °C for the SAB 80C515/80C535-T3

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input low voltage (except $\overline{EA}$)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input high voltage (except $\overline{RESET}$ and XTAL[2)]	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL2	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage to $\overline{RESET}$	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage, ports 1, 2, 3, 4, 5	V_{OL}	–	– 0.45	V	I_{OL} = 1.6 mA [1)]

Notes see page 36.

DC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Output low voltage, port 0, ALE, $\overline{PSEN}$	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA 1)
Output high voltage, ports 1, 2, 3, 4, 5	V_{OH}	2.4 0.9 V_{CC}	– –	V V	I_{OH} = – 80 µA I_{OH} = – 10 µA
Output high voltage (port 0 in external bus mode, ALE, PSEN)	V_{OH1}	2.4 0.9 V_{CC}	– –	V V	I_{OH} = – 400 µA I_{OH} = – 40 µA 2)
Logic 0 input current, ports 1, 2, 3, 4, 5	I_{IL}	– 10	– 70	µA	V_{IN} = 0.45 V
Input low current to $\overline{RESET}$ for reset	I_{IL2}	– 10	– 100	µA	V_{IN} = 0.45 V
Input low current ($\overline{XTAL2}$)	I_{IL3}	–	– 15	µA	V_{IN} = 0.45 V
Input low current ($\overline{PE}$)	I_{IL4}	–	– 20	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current, ports 1, 2, 3, 4, 5	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, port 6, AN0-7, $\overline{EA}$)	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	–	10	pF	f_C = 1 MHz, T_A = 25 °C
Power-supply current: Active mode, 12 MHz 6) Idle mode, 12 MHz 6) Active mode, 16 MHz 6) Idle mode, 16 MHz 6) Power-down mode	 – I_{CC} – I_{CC} – I_{CC} – I_{CC} – I_{PD}	 – – – – –	 35 13 46 17 50	 mA mA mA mA µA	 V_{CC} = 5 V 4) V_{CC} = 5 V 5) V_{CC} = 5 V 4) V_{CC} = 5 V 5) V_{CC} = 2 V to 5.5 V 3)

Notes see page 36.

Notes for page 34 and 35:

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1, 3, 4 and 5. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation.
   In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V.
   Then, it may be desirable to qualify ALE with a Schmitttrigger, or use an address latch with a Schmitttrigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the VOH on ALE and PSEN to momentarily fall below the 0.9 V_{CC} specification when the address bits are stabilizing.

3) Power-down I_{CC} is measured with: $\overline{EA}$ = Port 0 = Port 6 = V_{CC};
   XTAL1 = N.C.; XTAL2 = V_{SS}; $\overline{RESET}$ = V_{CC}; V_{AGND} = V_{SS}; all other pins are disconnected.

4) I_{CC}(active mode) is measured with: XTAL2 driven with the clock signal according to the figure below; XTAL1 = N.C.; EA = Port 0 = Port 6 = V_{CC}; RESET = V_{SS}; all other pins are disconnected. I_{CC} might be slightly higher if a crystal oscillator is used.

5) I_{CC} (idle mode) is measured with: XTAL2 driven with the clock signal according to the figure below; XTAL1 = N.C.; $\overline{EA}$ = V_{SS}; Port 0 = Port 6 V_{CC}; RESET = V_{CC}; all other pins are disconnected; all on-chip peripherals are disabled.

6) I_{CC} at other frequencies is given by:
   Active mode: $I_{CC\,max}$ (mA) = 2.67 × f_{OSC} (MHz) + 3.00
   Idle mode: $I_{CC\,max}$ (mA) = 0.88 × f_{OSC} (MHz) + 2.50
   where f_{OSC} is the oscillator frequency in MHz.
   $I_{CC\,max}$ is given in mA and measured at V_{CC} = 5 V (see also notes 4 and 5)

A/D Converter Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V; V_{AREF} = V_{CC} ± 5 %; V_{AGND} = V_{SS} ± 0.2 V;
$V_{IntAREF} - V_{IntAGND} \geq 1$ V; T_A = 0 to 70 °C for SAB 80C515/80C535
T_A = – 40 to 85 °C for SAB 80C515/80C535-T40/85

Parameter	Symbol	Limit values			Unit	Test condition
		min.	typ.	max.		
Analog input voltage	V_{AINPUT}	V_{AGND} – 0.2	–	V_{AREF} + 0.2	V	9)
Analog input capacitance	C_I	–	25	45	pF	7)
Load time	t_L	–	–	2 t_{CY}	µs	–
Sample time (incl. load time)	t_S	–	–	7 t_{CY}	µs	–
Conversion time (incl. sample time)	t_C	–	–	13 t_{CY}	µs	–
Total unadjusted error	TUE	–	± 1	± 2	LSB	$V_{IntAREF}$ = V_{AREF} = V_{CC} $V_{IntAGND}$ = V_{AGND} = V_{SS} 7)
V_{AREF} supply current	I_{REF}	–	–	5	mA	8)
Internal reference error	$V_{Int\ REFERR}$	–		± 30	mV	8)

7) The output impedance of the analog source must be low enough to assure full loading of the sample capacitance (C_I) during load time (t_L). After charging of the internal capacitance (C_I) in the load time (t_L) the analog input must be held constant for the rest of the sample time (t_S)

8) The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

9) Exceeding these limit values at one or more input channels will cause additional current which is sinked / sourced at these channels. This may also affect the accuracy of other channels which are operated within these specifications.

AC Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V (C_L for Port 0, ALE and $\overline{PSEN}$ outputs = 100 pF;
C_L for all outputs = 80 pF); T_A = 0 to 70 °C for SAB 80C515/80C535
T_A = – 40 to 85 °C for SAB 80C515/80C535-T40/85

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
ALE pulse width	t_{LHLL}	127	–	$2\,t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	53	–	$t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX}	48	–	$t_{CLCL} - 35$	–	ns
ALE to valid instruction in	t_{LLIV}	–	233	–	$4\,t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	58	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	215		$3\,t_{CLCL} - 35$		ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	–	150	–	$3\,t_{CLCL} - 100$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} [1]	–	63	–	$t_{CLCL} - 20$	ns
Address valid after $\overline{PSEN}$	t_{PXAV} [1]	75		$t_{CLCL} - 8$		ns
Address to valid instruction in	t_{AVIV}	–	302	–	$5\,t_{CLCL} - 115$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

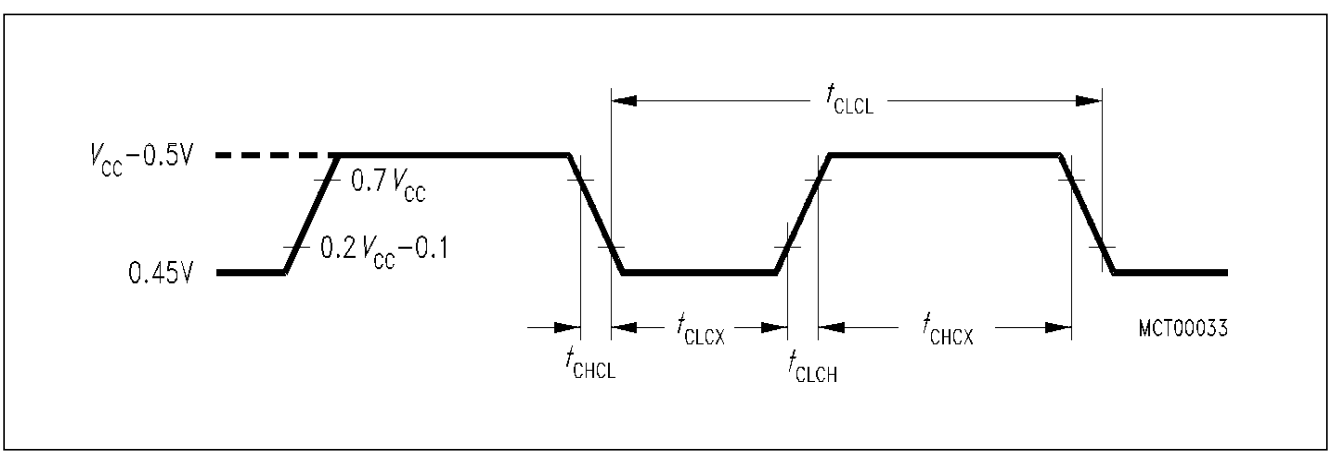
[1] Interfacing the SAB 80C515 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	400	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	132	–	2 t_{CLCL} – 35	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	5 t_{CLCL} – 165	ns
DATA hold after $\overline{RD}$	t_{RHDX}	0	–	0		ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	2 t_{CLCL} – 70	ns
ALE to valid data in	t_{LLDV}	–	517	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	585	–	9 t_{CLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	t_{CLCL} – 40	t_{CLCL} + 40	ns
Address valid to $\overline{WR}$	t_{AVWL}	203	–	4 t_{CLCL} – 130	–	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	t_{CLCL} – 50	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	288	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	13	–	t_{CLCL} – 50	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

AC Characteristics (cont'd)

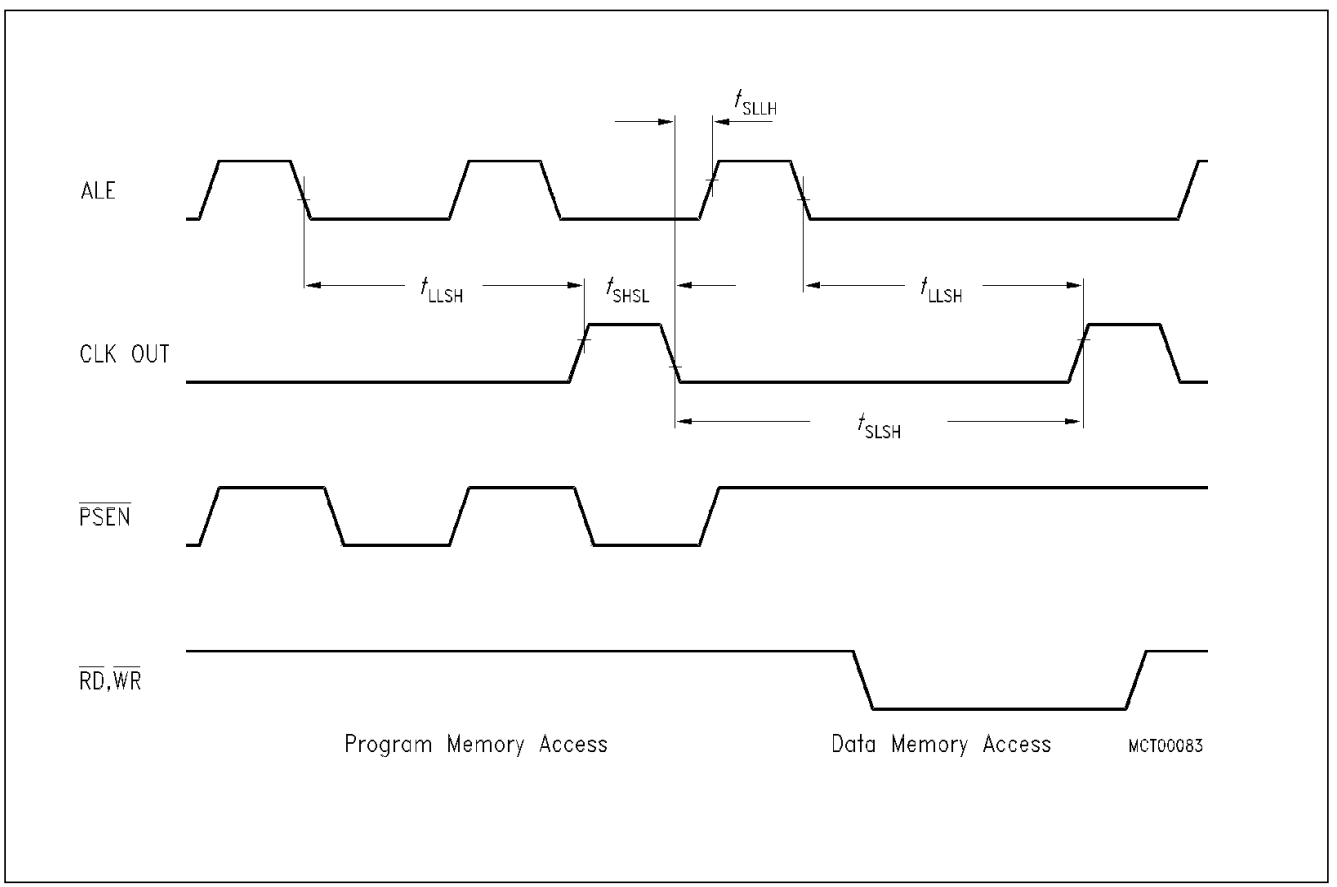
Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 3.5 MHz to 12 MHz		
		min.	max.	
External Clock Drive				
Oscillator period	t_{CLCL}	83.3	285	ns
Oscillator frequency	$1/t_{CLCL}$	0.5	12	MHz
High time	t_{CHCX}	20	–	ns
Low time	t_{CLCX}	20	–	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns



External Clock Cycle

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
System Clock Timing						
ALE to CLKOUT	t_{LLSH}	543	–	7 t_{CLCL} – 40	–	ns
CLKOUT high time	t_{SHSL}	127	–	2 t_{CLCL} – 40	–	ns
CLKOUT low time	t_{SLSH}	793	–	10 t_{CLCL} – 40	–	ns
CLKOUT low to ALE high	t_{SLLH}	43	123	t_{CLCL} – 40	t_{CLCL} + 40	ns



System Clock Timing

AC Characteristics for SAB 80C515-16/80C535-16

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V (C_L for Port 0, ALE and $\overline{PSEN}$ outputs = 100 pF;
C_L for all outputs = 80 pF) T_A = 0 to 70 °C for SAB 80C515-16/80C535-16
T_A = – 40 to 85 °C for SAB 80C515-16/80C535-16-T40/85

Parameter	Symbol	Limit values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 16 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
ALE pulse width	t_{LHLL}	85	–	$2\,t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	33	–	$t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX}	28	–	$t_{CLCL} - 35$	–	ns
ALE to valid instruction in	t_{LLIV}	–	150	–	$4\,t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	38	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	153		$3\,t_{CLCL} - 35$		ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	–	88	–	$3\,t_{CLCL} - 100$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} [1)]	–	43	–	$t_{CLCL} - 20$	ns
Address valid after $\overline{PSEN}$	t_{PXAV} [1)]	55		$t_{CLCL} - 8$		ns
Address to valid instruction in	t_{AVIV}	–	198	–	$5\,t_{CLCL} - 115$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

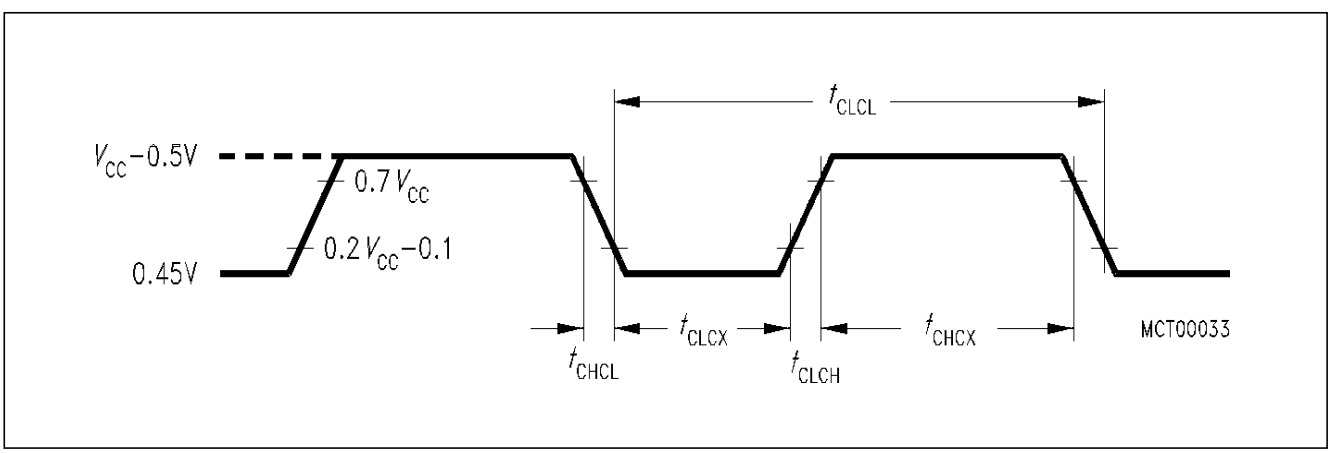
1) Interfacing the SAB 80C515-16 to devices with float times up to 55 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 16 MHz		
		min.	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	275	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	275	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	90	–	2 t_{CLCL} – 35	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	148	–	5 t_{CLCL} – 165	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	55	–	2 t_{CLCL} – 70	ns
ALE to valid data in	t_{LLDV}	–	350	–	8t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	398	–	9 t_{CLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	138	238	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	23	103	t_{CLCL} – 40	t_{CLCL} + 40	ns
Address valid to $\overline{WR}$	t_{AVWL}	120	–	4 t_{CLCL} – 130	–	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	13	–	t_{CLCL} – 50	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	288	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	13	–	t_{CLCL} – 50	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

AC Characteristics (cont'd)

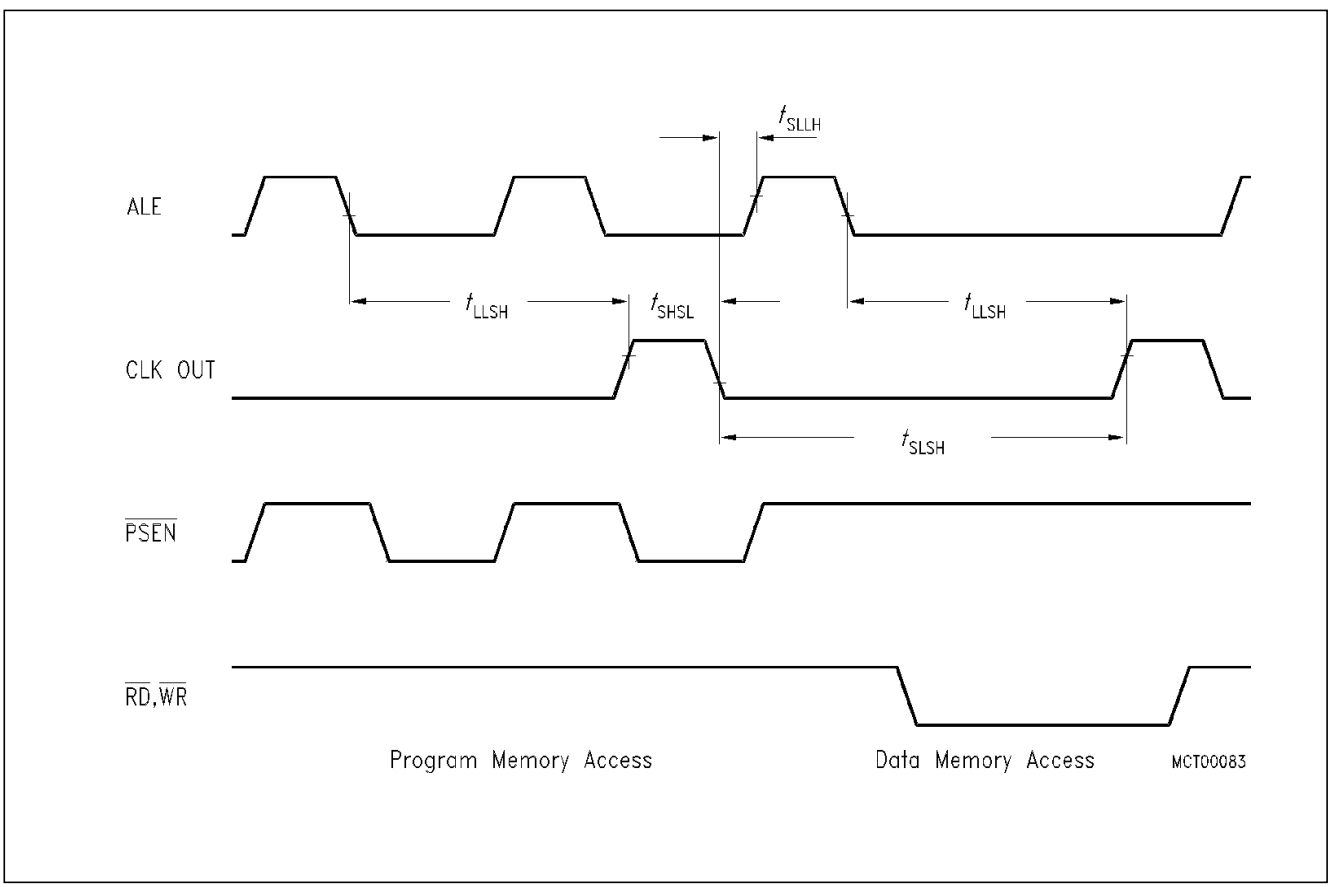
Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 3.5 MHz to 16 MHz		
		min.	max.	
External Clock Drive				
Oscillator period	t_{CLCL}	62.5	285	ns
Oscillator frequency	$1/t_{CLCL}$	0.5	16	MHz
High time	t_{CHCX}	15	–	ns
Low time	t_{CLCX}	15	–	ns
Rise time	t_{CLCH}	–	15	ns
Fall time	t_{CHCL}	–	15	ns



External Clock Cycle

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 16 MHz		
		min.	max.	min.	max.	
System Clock Timing						
ALE to CLK OUT	t_{LLSH}	398	–	7 t_{CLCL} – 40	–	ns
CLK OUT high time	t_{SHSL}	85	–	2 t_{CLCL} – 40	–	ns
CLK OUT low time	t_{SLSH}	585	–	10 t_{CLCL} – 40	–	ns
CLK OUT low to ALE high	t_{SLLH}	23	103	t_{CLCL} – 40	t_{CLCL} + 40	ns



System Clock Timing

AC Characteristics for SAB 80C515-20 / 80C535-20

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V T_A = 0 °C to + 70 °C
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Parameter	Symbol	Limit values				Unit
		20 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 20 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
ALE pulse width	t_{LHLL}	60	–	2 t_{CLCL} – 40	–	ns
Address setup to ALE	t_{AVLL}	20	–	t_{CLCL} – 30	–	ns
Address hold after ALE	t_{LLAX}	20	–	t_{CLCL} – 30	–	ns
ALE low to valid instr in	t_{LLIV}	–	100	–	4 t_{CLCL} – 100	ns
ALE to $\overline{PSEN}$	t_{LLPL}	25	–	t_{CLCL} – 25	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	115	–	3 t_{CLCL} – 35	–	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	–	75	–	3 t_{CLCL} – 75	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	–	40	–	t_{CLCL} – 10	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	47	–	t_{CLCL} – 3	–	ns
Address to valid instr in	t_{AVIV}	–	190	–	5 t_{CLCL} – 60	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

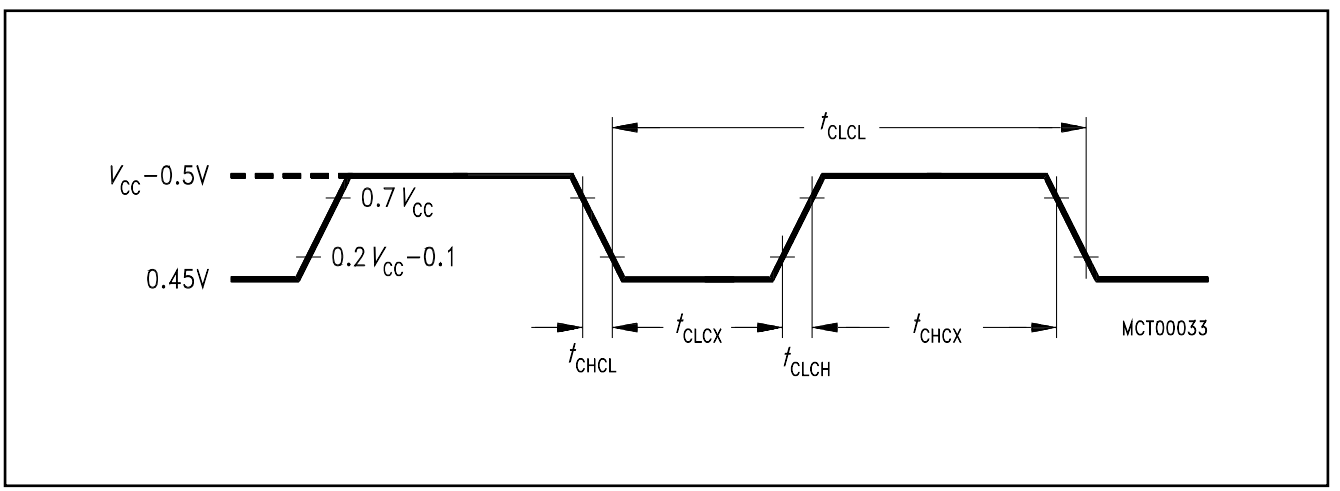
*) Interfacing the SAB 80C515 / 80C535 microcontrollers to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		20 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 20 MHz		
		min.	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	200	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	200	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	65	–	2 t_{CLCL} – 35	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	155	–	5 t_{CLCL} – 95	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	40	–	2 t_{CLCL} – 60	ns
ALE to valid data in	t_{LLDV}	–	250	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	285	–	9 t_{CLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	100	200	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	70	–	4 t_{CLCL} – 130	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	20	80	t_{CLCL} – 30	t_{CLCL} + 30	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	t_{CLCL} – 45	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	200	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	10	–	t_{CLCL} – 40	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

AC Characteristics (cont'd)

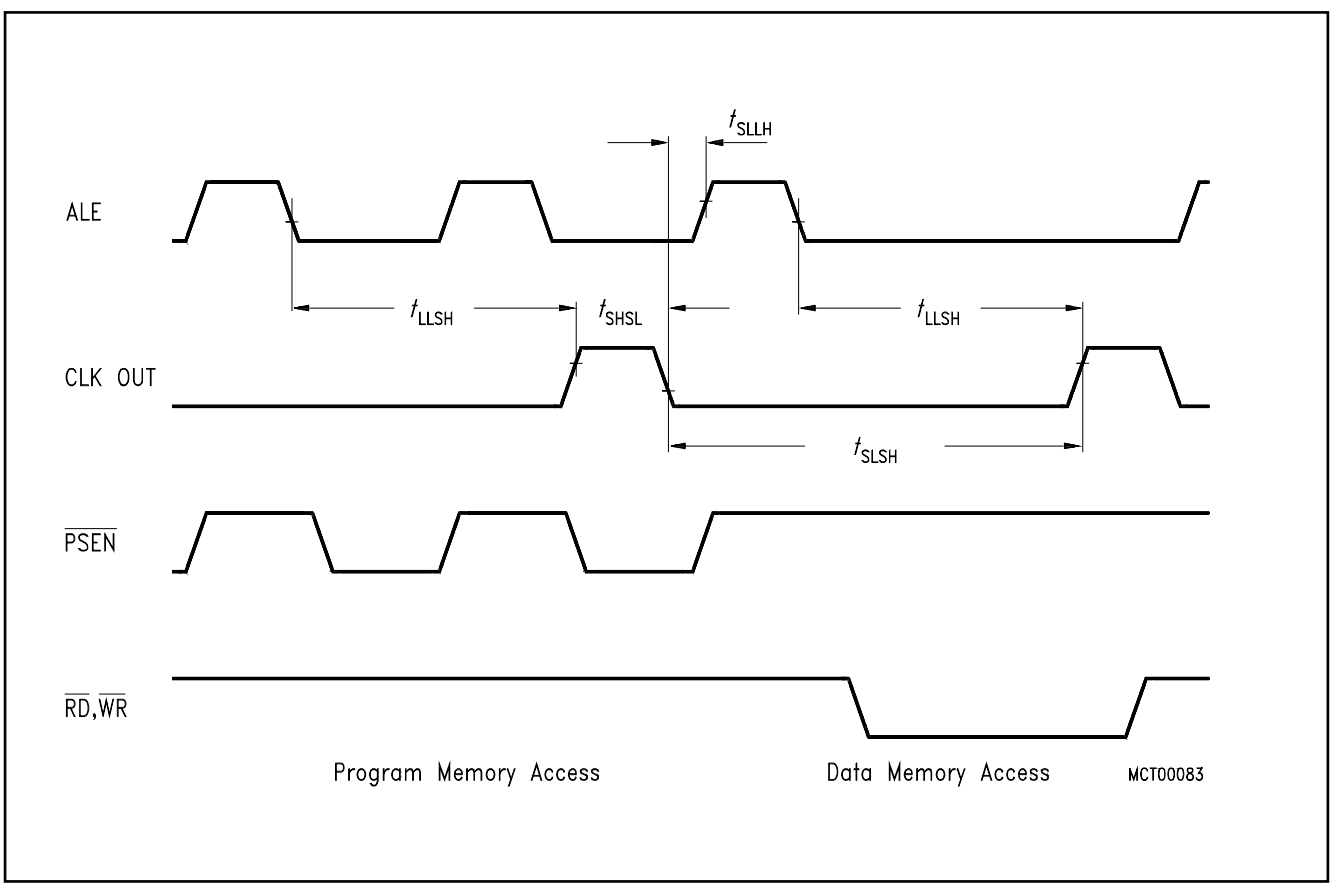
Parameter	Symbol	Limit Values		Unit
		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 20 MHz		
		min.	max.	
External Clock Drive				
Oscillator period	t_{CLCL}	50	285	ns
High time	t_{CHCX}	12	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	12	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	12	ns
Fall time	t_{CHCL}	–	12	ns



External Clock Cycle

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		20 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 20 MHz		
		min.	max.	min.	max.	
System Clock Timing						
ALE to CLKOUT	t_{LLSH}	310	–	7 t_{CLCL} – 40	–	ns
CLKOUT high time	t_{SHSL}	60	–	2 t_{CLCL} – 40	–	ns
CLKOUT low time	t_{SLSH}	460	–	10 t_{CLCL} – 40	–	ns
CLKOUT low to ALE high	t_{SLLH}	10	90	t_{CLCL} – 40	t_{CLCL} + 40	ns

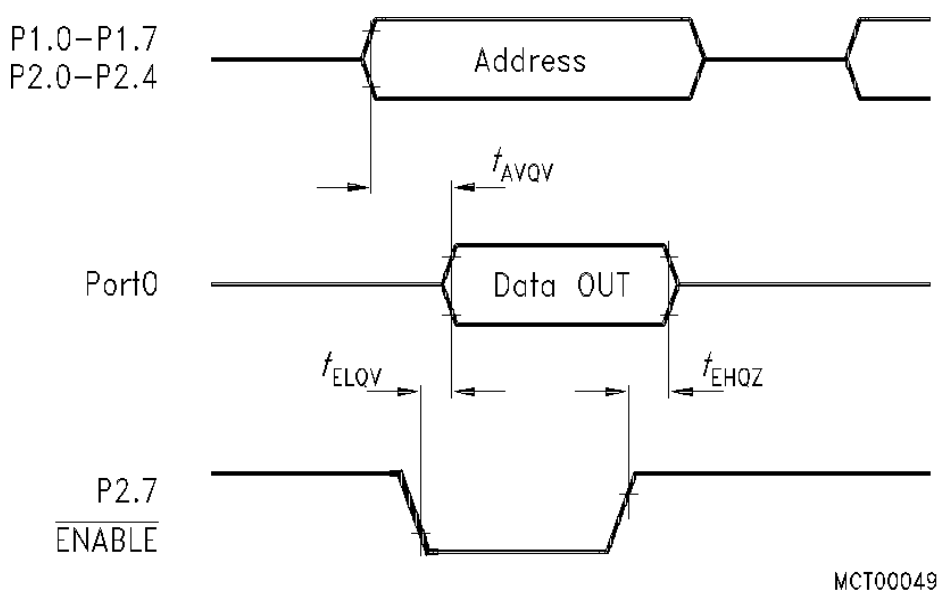


External Clock Cycle

ROM Verification Characteristics

T_A = 25 °C ± 5 °C; V_{CC} = 5 V ± 10 %; V_{SS} = 0 V

Parameter	Symbol	Limit values		Unit
		min.	max.	
ROM Verification				
Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns
ENABLE to valid data	t_{ELQV}	–	48 t_{CLCL}	ns
Data float after ENABLE	t_{EHOZ}	0	48 t_{CLCL}	ns
Oscillator frequency	$1/t_{CLCL1}$	4	6	MHz
Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns

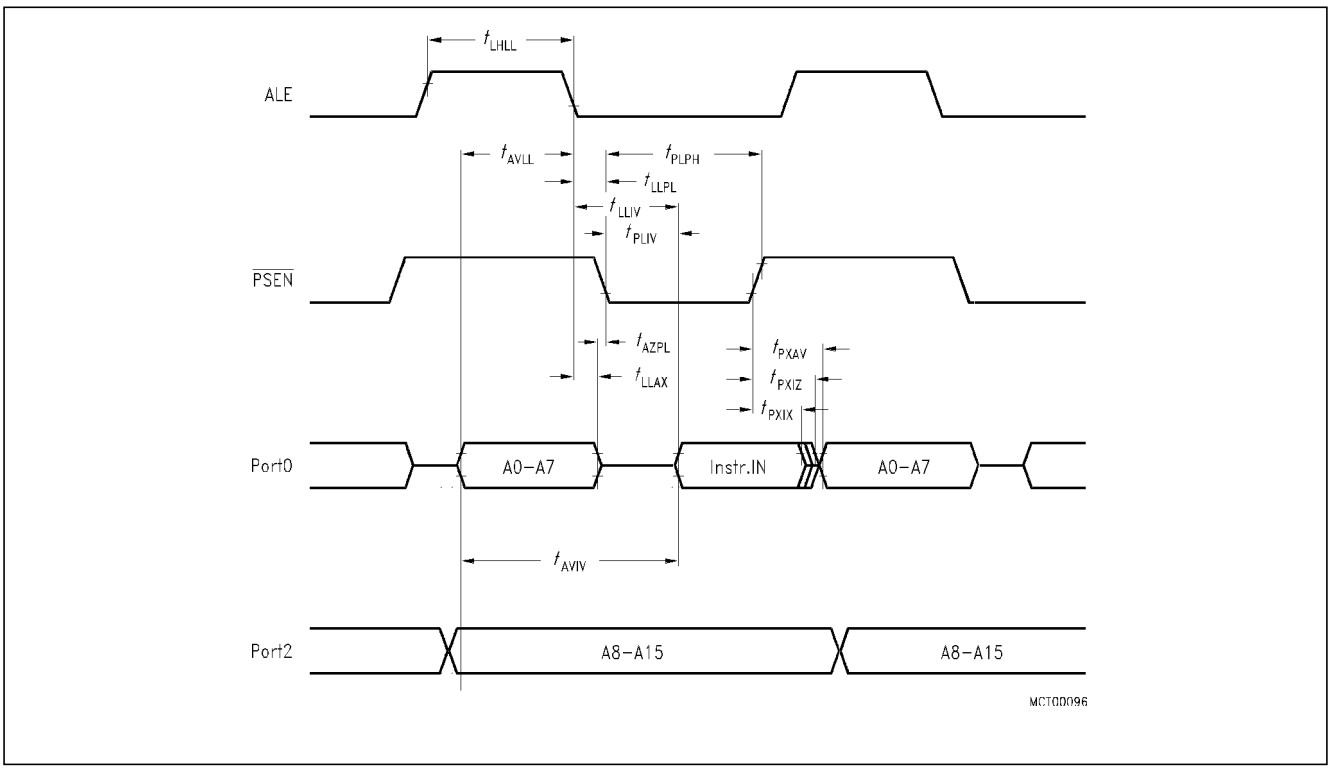


Address: P1.0–P1.7=A0–A7
P2.0–P2.4=A8–A12
Data: P0.0–P0.7=D0–D7

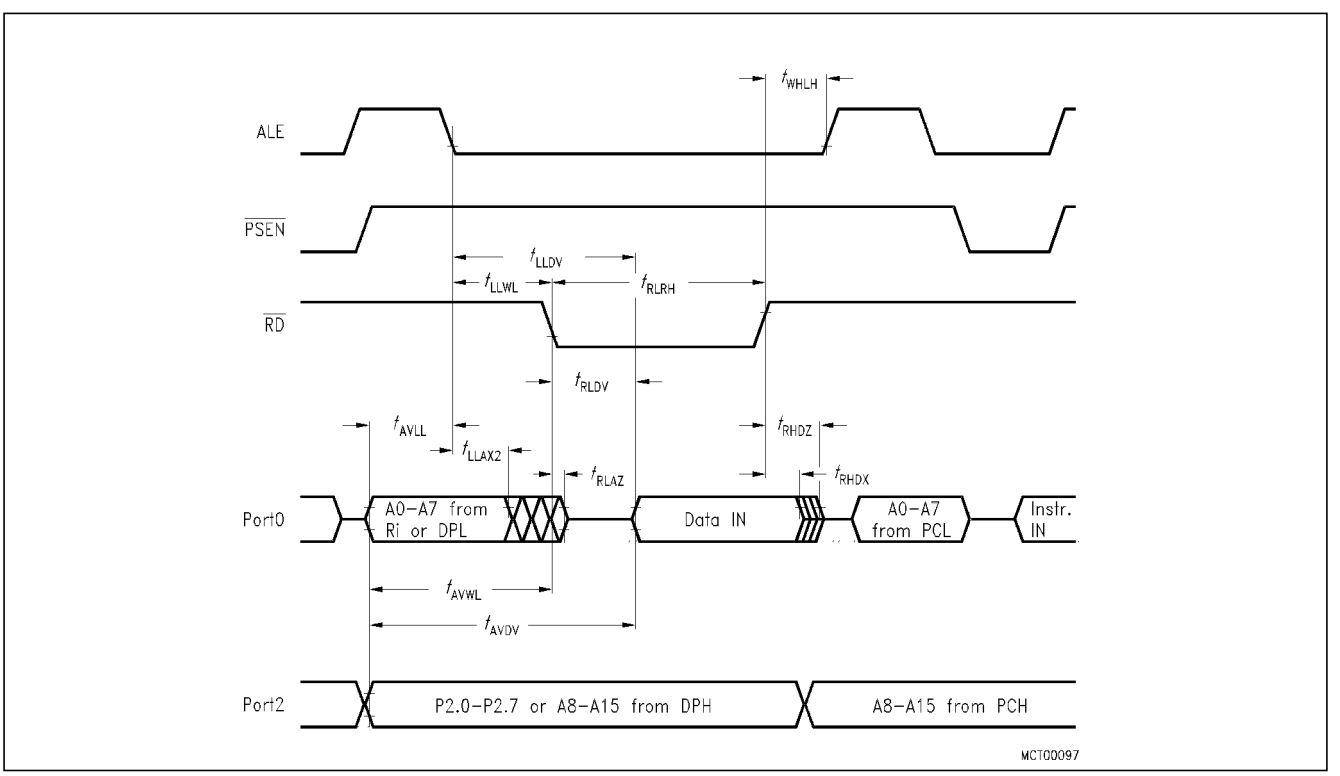
Inputs: P2.5–P2.6, $\overline{PSEN}$=V_{SS}
ALE, $\overline{EA}$= V_{IH}
$\overline{RESET}$ = V_{SS}

ROM Verification

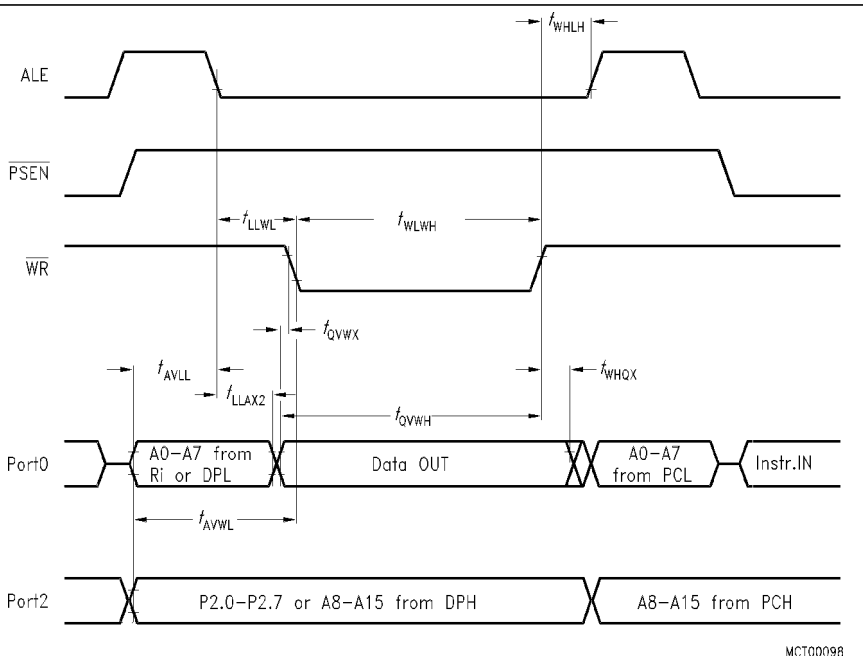
Waveforms



Program Memory Read Cycle

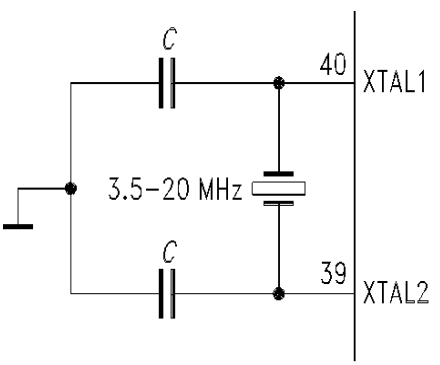


Data Memory Read Cycle



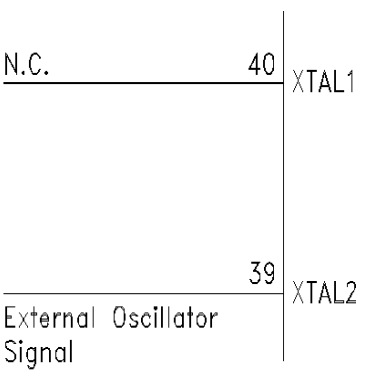
AC inputs during testing are driven at V_{CC} – 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at $V_{IH\,min}$ for a logic '1' and $V_{IL\,max}$ for a logic '0'.

Data Memory Write Cycle



C = 30pF ± 10pF
(incl. stray capacitance)

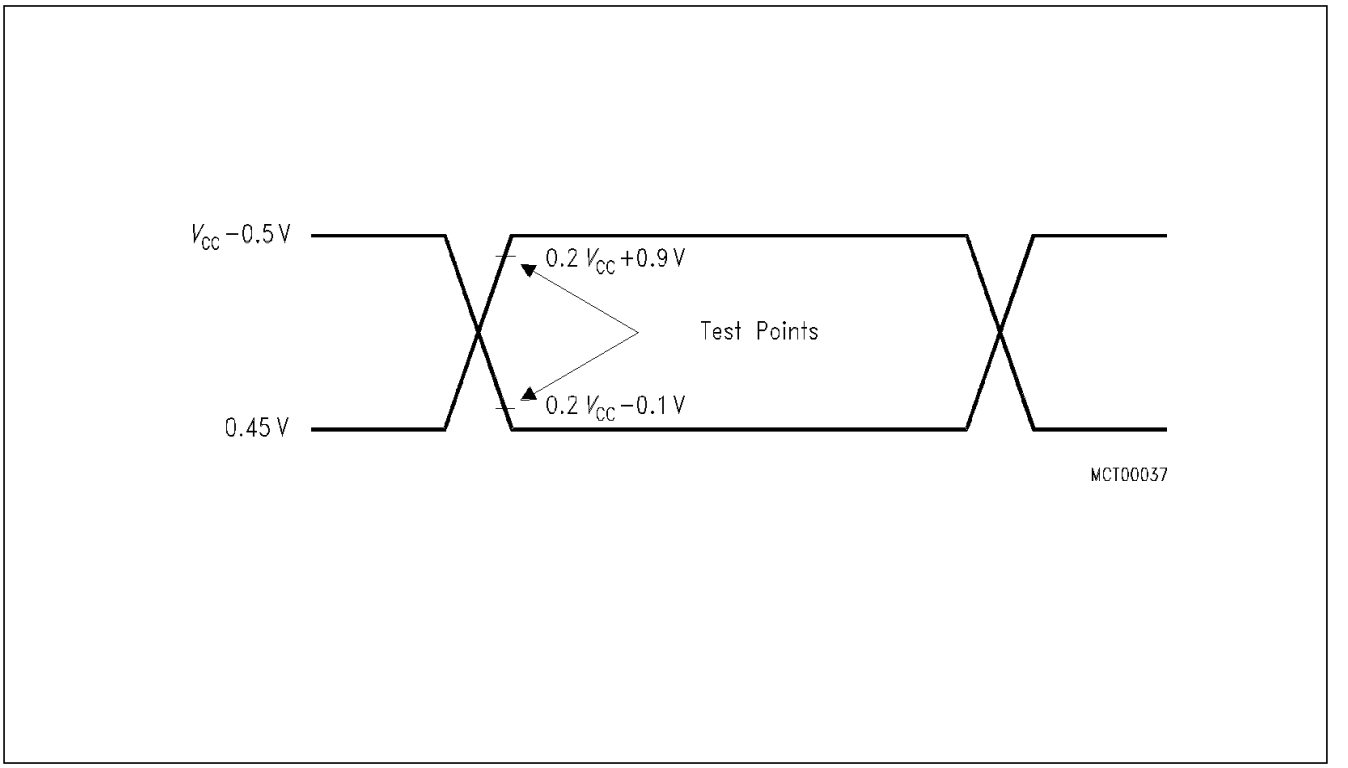
Crystal Oscillator Mode



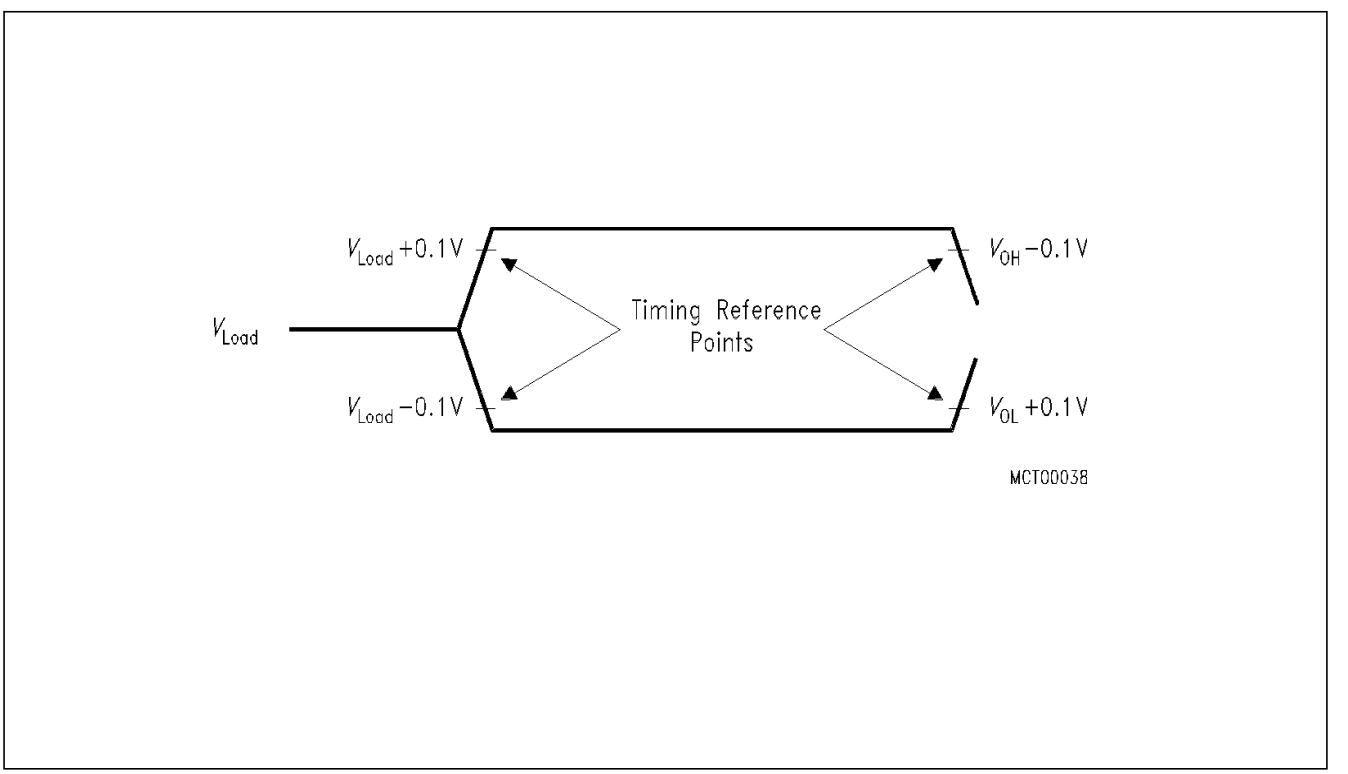
Driving from External Source

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV deviation from the load voltage V_{OH}/V_{OL} occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

Recommended Oscillator Circuits



AC Testing: Input, Output Waveforms

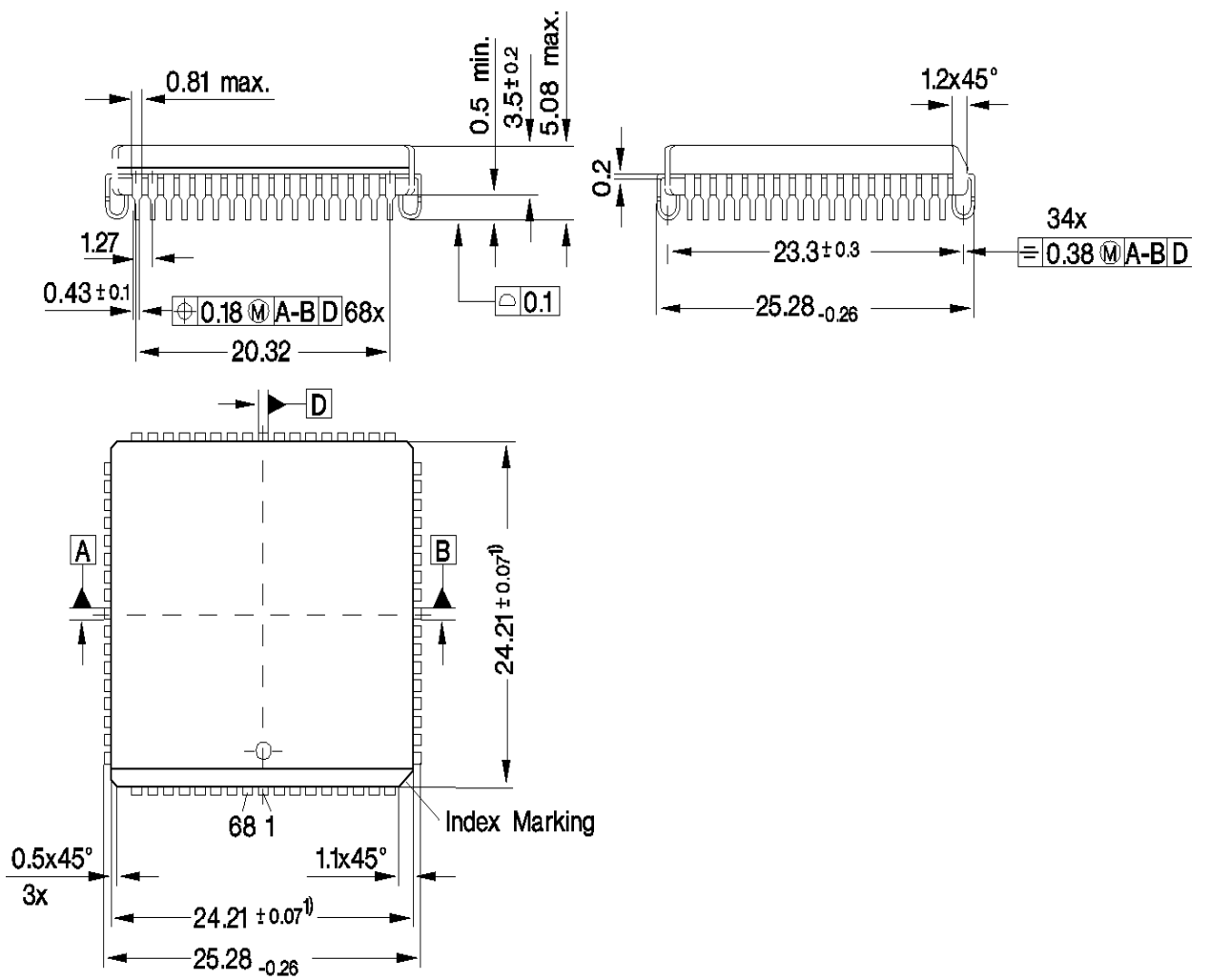


AC Testing: Float Waveforms

SMD = Surface Mounted Device

Package Outlines

Plastic Package, P-LCC-68 – SMD
(Plastic Leaded Chip-Carrier)



1) Does not include plastic or metal protrusion of 0.15 max. per side

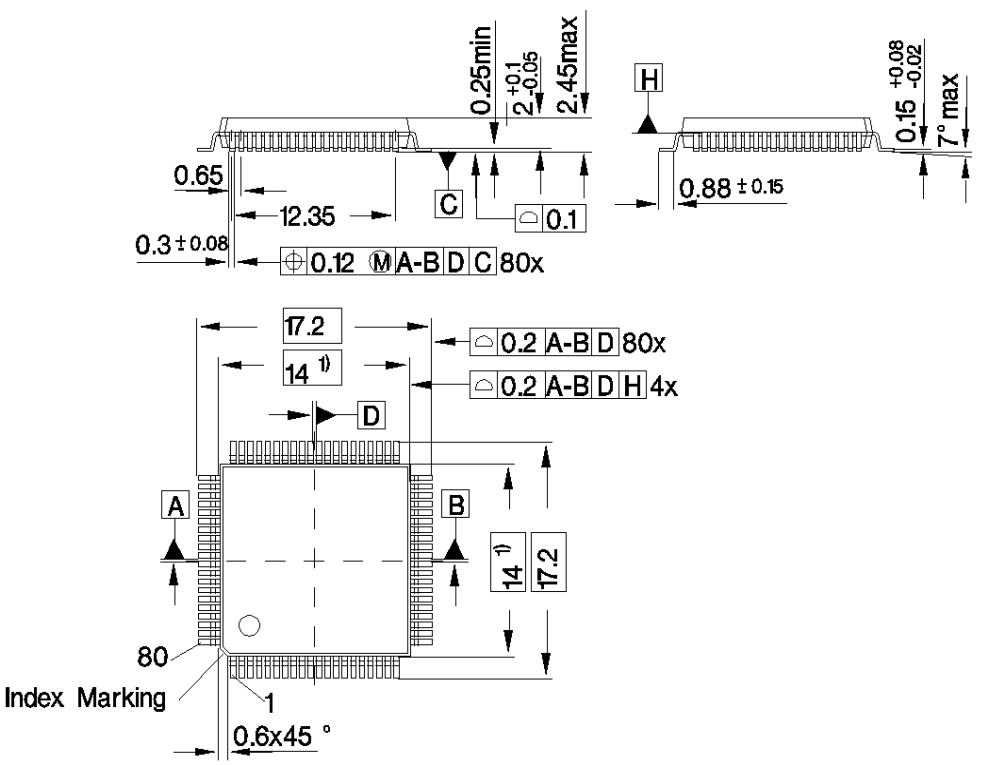
Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

Package Outlines

Plastic Package, P-MQFP-80 – SMD
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

SIEMENS

High-Performance SAB 80C515A / 83C515A-5
8-Bit CMOS Single-Chip Microcontroller

Preliminary

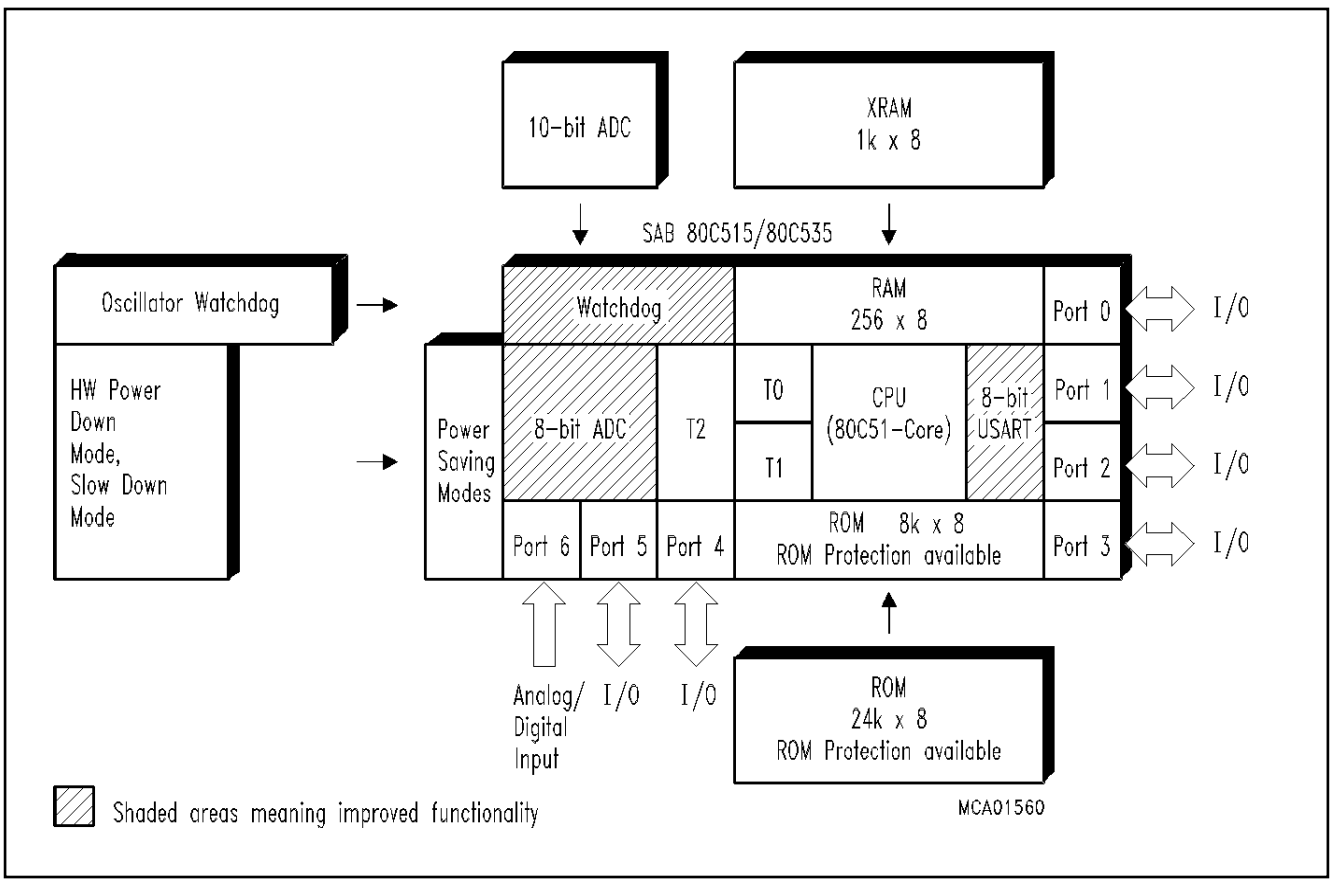
SAB 83C515A-5	Microcontroller with factory mask-programmable ROM
SAB 80C515A	Microcontroller for external ROM

- SAB 80C515A / 83C515A-5, up to 18 MHz operation frequency
- 32 K × 8 ROM (SAB 83C515A-5 only, ROM-Protection available)
- 256 × 8 on-chip RAM
- Additional 1 K × 8 on-chip RAM (XRAM)
- Superset of SAB 80C51 architecture:
  1 µs instruction cycle time at 12 MHz
  666 ns instruction cycle time at 18 MHz
  256 directly addressable bits
  Boolean processor
  64 Kbyte external data and program memory addressing
- Three 16-bit timer/counters
- Versatile "fail-safe" provisions
- Twelve interrupt vectors, four priority levels selectable
- Genuine 10-bit A/D converter with 8 multiplexed inputs
- Full duplex serial interface with programmable Baudrate-Generator
- Functionally compatible with SAB 80C515
- Extended power saving mode
- Fast Power-On Reset
- Seven ports: 48 I/O lines, 8 input lines
- Two temperature ranges available:
  0 to 70 °C (T1)
  – 40 to 85 °C (T3)
- Plastic packages: P-LCC-68 and P-MQFP-80

The SAB 80C515A/83C515A-5 is a high-end member of the Siemens SAB 8051 microcontroller family. It is designed in Siemens ACMOS technology and based on the SAB 8051 architecture. ACMOS is a technology which combines high-speed and density characteristics with low-power consumption or dissipation.

While maintaining all the SAB 80C515 features and operating characteristics the SAB 80C515A/83C515A-5 contains more on-chip RAM/ROM. Furthermore a new 10-bit A/D-Converter is implemented as well as extended security mechanisms. The SAB 80C515A is identical with the SAB 83C515A-5 except that it lacks the on-chip program memory. The SAB 80C515A / 83C515A-5 is supplied in a 68-pin plastic leaded chip carrier package (P-LCC- 68) and in a 80-pin plastic metric quad flat package (P-MQFP-80).

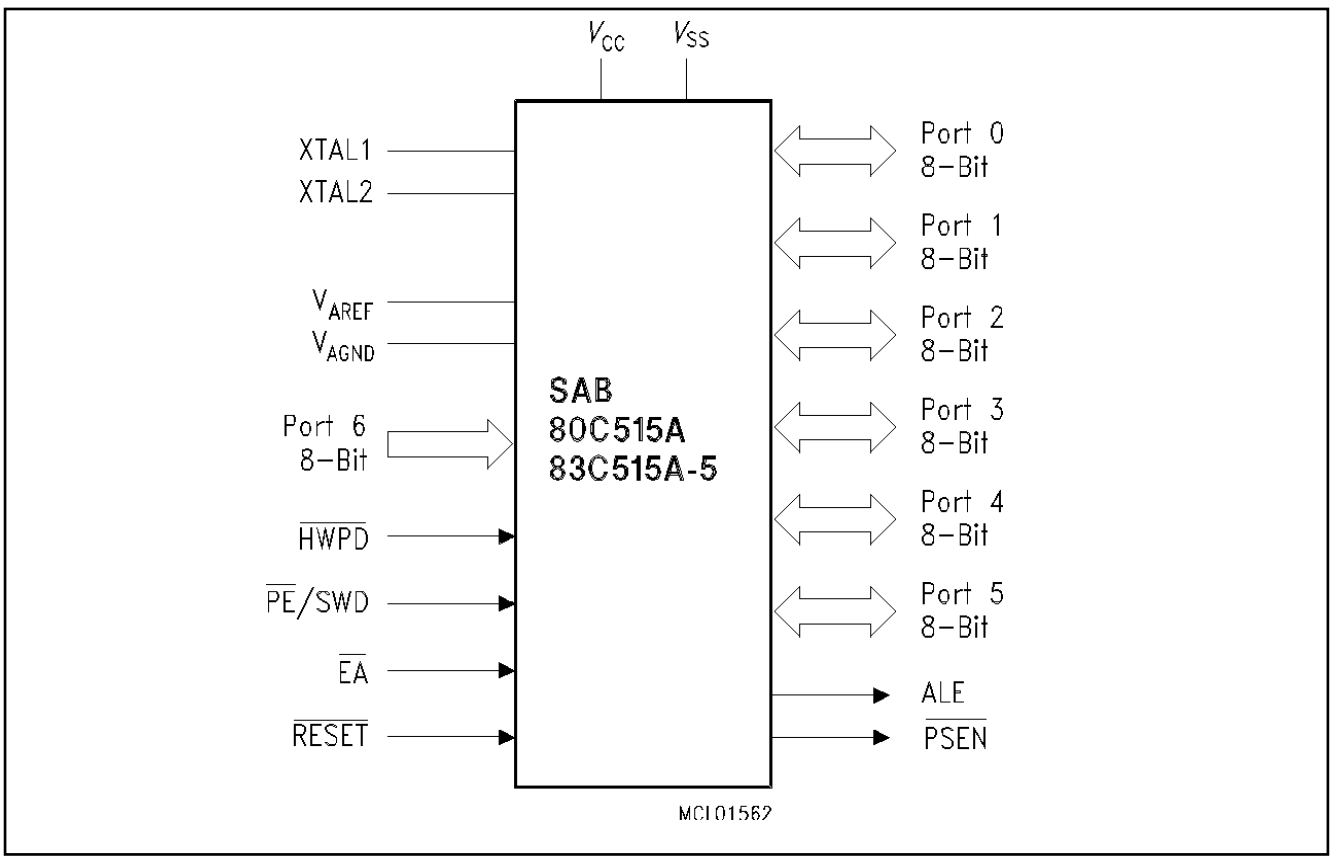
Versions for extended temperature range – 40 to + 110 °C are available on request.



Ordering Information

Type	Ordering Code	Package	Description 8-Bit CMOS microcontroller
SAB 80C515A-N18	Q67120-C0581	P-LCC-68	for external memory, 18 MHz
SAB 83C515A-5N18	Q67120-DXXXX	P-LCC-68	with mask-programmable ROM, 18 MHz
SAB 80C515A-N18-T3	Q67120-C0784	P-LCC-68	for external memory, 18 MHz ext. temperature – 40 to + 85 °C
SAB 83C515A-5N18-T3	Q67120-DXXXX	P-LCC-68	with mask-programmable ROM, 18 MHz ext. temperature – 40 to + 85 °C
SAB 80C515A-M18-T3	Q67120-C0851	P-MQFP-80	for external memory, 18 MHz ext. temperature – 40 to + 85 °C
SAB 83C515A-5M18-T3	Q67120-DXXXX	P-MQFP-80	with mask-programmable ROM, 18 MHz ext. temperature – 40 to + 85 °C

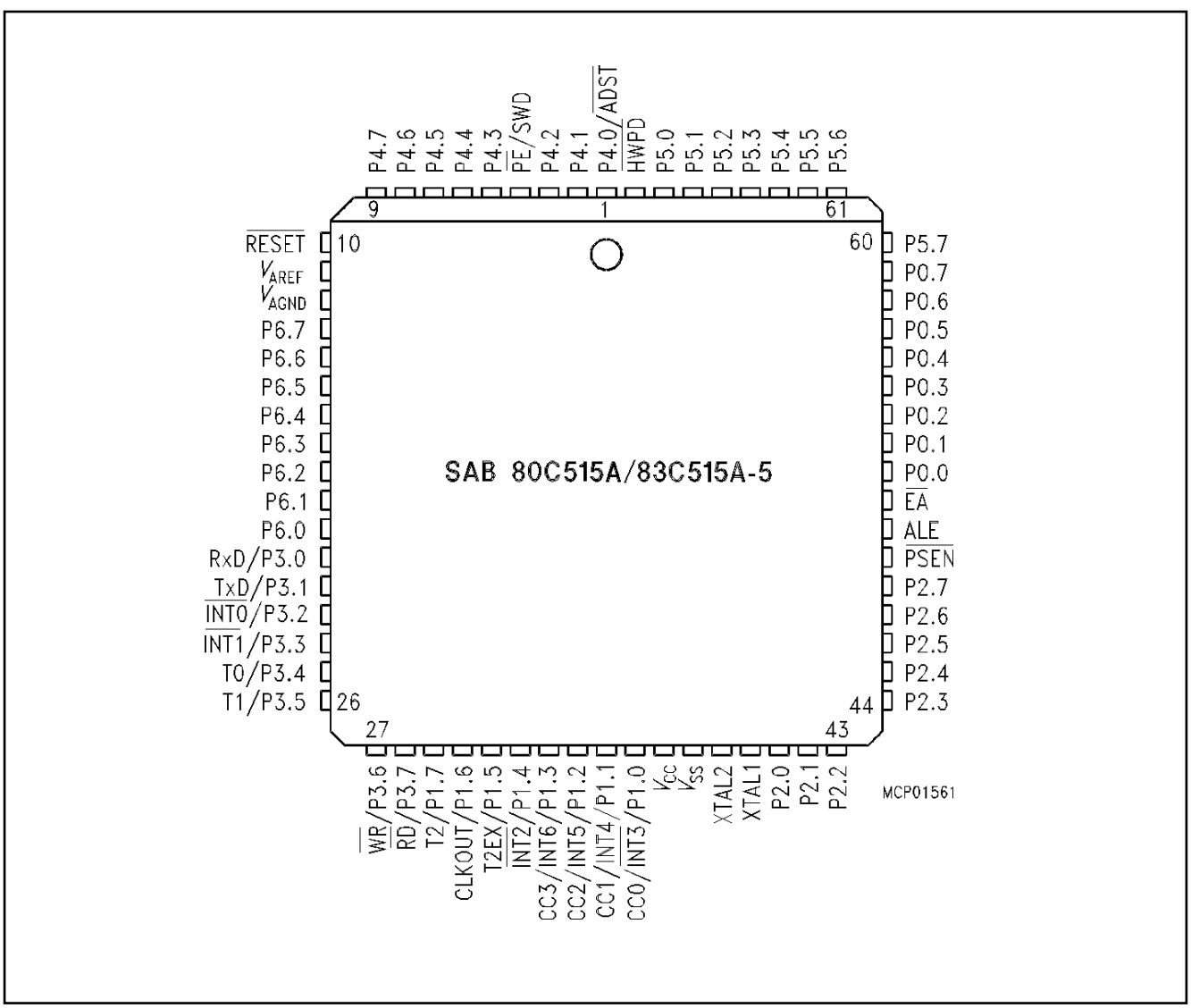
Notes: Versions for extended temperature range – 40 to + 110 °C on request.
The ordering number of ROM types (DXXXX extension) is defined after program release (verification) of the customer.



Logic Symbol

The pin functions of the SAB 80C515A are identical with those of the SAB 80C515 with following exception:

Pin	SAB 80C515A	SAB 80C515
68	$\overline{\text{HWPD}}$	V_{CC}
1	P0.4/$\overline{\text{ADST}}$	P4.0
4	$\overline{\text{PE}}$/SWD	$\overline{\text{PE}}$



Pin Configuration
(P-LCC-68)

N.C. pins must not be connected.

Pin Configuration
(P-MQFP-80)

Pin Definitions and Functions

Symbol	Pin P-LCC-68	Pin P-MQFP-80	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	72-74, 76-80	I/O	**Port 4** is an 8-bit bidirectional I/O port with internal pull-up resistors. Port 4 pins that have 1's written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. P4 also contains the external A/D converter control pin. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary function assigned to port 6: – $\overline{ADST}$(P4.0): external A/D converter start pin
$\overline{PE}$/SWD	4	75	I	**Power saving mode $\overline{enable}$/Start Watchdog Timer** A low level on this pin allows the software to enter the power down, idle and slow down mode. In case the low level is also seen during reset, the watchdog timer function is off on default. Use of the software controlled power saving modes is blocked, when this pin is held on high level. A high level during reset performs an automatic start of the watchdog timer immediately after reset. When left unconnected this pin is pulled high by a weak internal pull-up resistor.
$\overline{RESET}$	10	1	I	**$\overline{Reset}$ pin** A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80C515A. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}
V_{AREF1}	11	3		**Reference voltage** for the A/D converter
V_{AGND}	12	4		**Reference ground** for the A/D converter

Pin Definitions and Functions (cont'd)

Symbol	Pin P-LCC-68	Pin P-MQFP-80	Input (I) Output (O)	Function
P6.7-P6.0	13-20	5-12	I	**Port 6** is an 8-bit unidirectional input port to the A/D converter. Port pins can be used for digital input, if voltage levels simultaneously meet the specifications high/low input voltages, and for the eight multiplexed analog inputs.
P3.0-P3.7	21-28	15-22	I/O	**Port 3** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 3 pins that have1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – R × D (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – T × D (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{INT0}$(P3.2): interrupt 0 input/timer 0 gate control input – $\overline{INT1}$(P3.3): interrupt 1 input/timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{WR}$(P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{RD}$(P3.7): the read control signal enables the external data memory to port 0

Pin Definitions and Functions (cont'd)

Symbol	Pin P-LCC-68	Pin P-MQFP-80	Input (I) Output (O)	Function
P1.7 - P1.0	29-36	24-31	I/O	**Port 1** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL} in the DC characteristics) because of the internal pullup resistors. The port is used for the low-order address byte during program verification. Port 1 also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows: – $\overline{INT3}$/CC0 (P1.0): interrupt 3 input / compare 0 output / capture 0 input – INT4/CC1 (P1.1): interrupt 4 input / compare 1 output / capture 1 input – INT5/CC2 (P1.2): interrupt 5 input / compare 2 output / capture 2 input – INT6/CC3 (P1.3): interrupt 6 input / compare 3 output / capture 3 input – $\overline{INT2}$(P1.4): interrupt 2 input – T2EX (P1.5): timer 2 external reloadtrigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input
XTAL2	39	36	–	**XTAL2** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.

Pin Definitions and Functions (cont'd)

Symbol	Pin P-LCC-68	Pin P-MQFP-80	Input (I) Output (O)	Function
XTAL1	40	37	-	**XTAL1** Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clokking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times and rise/fall times specified in the AC characteristics must be taken into account.
P2.0-P2.7	41-48	38-45	I/O	**Port 2** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current ($I_{IL,}$ in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application it uses strong internal pullup resistors when issuing 1's. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	49	47	O	The **$\overline{\text{Program Store Enable}}$** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. The signal remains high during internal program execution.
ALE	50	48	O	The **Address Latch enable** output is used for latching the address into external memory during normal operation. It is activated every six oscillator periods, except during an external data memory access.

Pin Definitions and Functions (cont'd)

Symbol	Pin P-LCC-68	Pin P-MQFP-80	Input (I) Output (O)	Function
$\overline{EA}$	51	49	I	**External Access Enable** When held high, the SAB 80C515A executes instructions from the internal ROM as long as the PC is less than 32768. When held low, the SAB 80C515A fetches all instructions from external program memory. For the SAB 80C515A this pin must be tied low.
P0.0-P0.7	52-59	52-59	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1's. Port 0 also outputs the code bytes during program verification in the SAB 80C515A. External pullup resistors are required during program verification.
P5.7-P5.0	60-67	60-67	I/O	**Port 5** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 5 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL} in the DC characteristics) because of the internal pullup resistors.
$\overline{HWPD}$	68	69	I	**Hardware Power Down** A low level on this pin for the duration of one machine cycle while the oscillator is running resets the SAB 80C515A. A low level for a longer period will force the part to Power Down Mode with the pins floating. (**see table 5**)
V_{CC}	37	32, 33	–	**Supply voltage** during normal, idle, and power-down operation.
V_{SS}	38	34, 35	–	**Ground** (0 V)
N.C.	–	2, 13, 14, 23, 46, 50, 51, 68, 70, 71	–	Not connected These pins of the P-MQFP-80 package must not be connected.

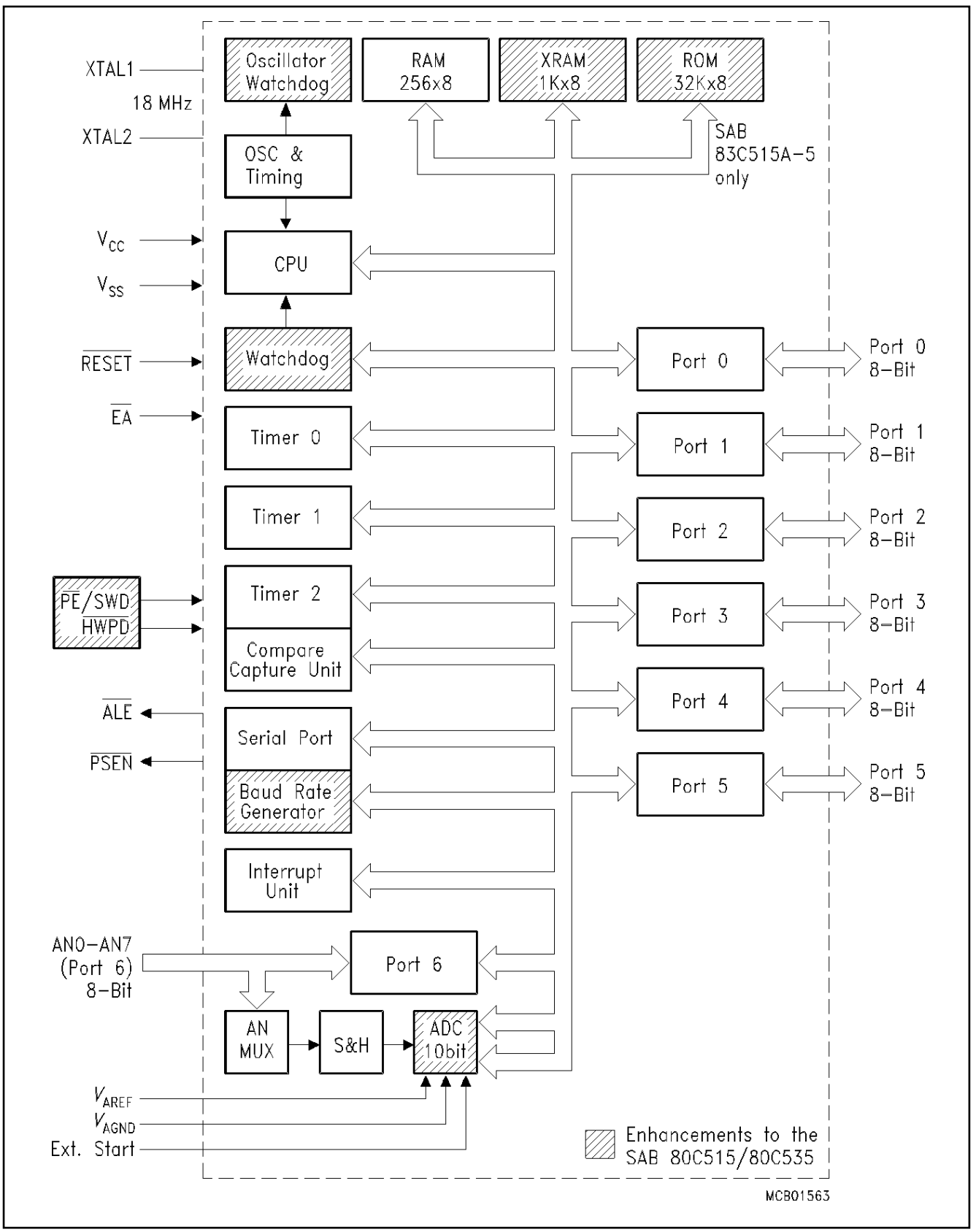


Figure 1
Block Diagram

Functional Description

The SAB 80C515A is based on 8051 architecture. It is a fully compatible member of the Siemens SAB 8051/80C51 microcontroller family being an significantly enhanced SAB 80C515. The SAB 80C515A is therefore code compatible with the SAB 80C515.

Having an 8-bit CPU with extensive facilities for bit-handling and binary BCD arithmetics the SAB 80C515A is optimized for control applications. With a 18 MHz crystal, 58 % of the instructions are executed in 666.67 ns.

While maintaining all architectural and operational characteristics of the SAB 80C515 the SAB 80C515A incorporates more on-chip RAM. A new 10-bit A/D-Converter is implemented as well as an oscillator watchdog unit. Also the maximum operating frequency of 18 MHz is higher than at the SAB 80C515.

With exception of the ROM sizes both parts are identical. Therefore the therm SAB 80C515A refers to both versions within this specification unless otherwise noted.

Memory Organisation

According to the SAB 8051 architecture, the SAB 80C515A has separate address spaces for program and data memory. Figure 2 illustrates the mapping of address spaces.

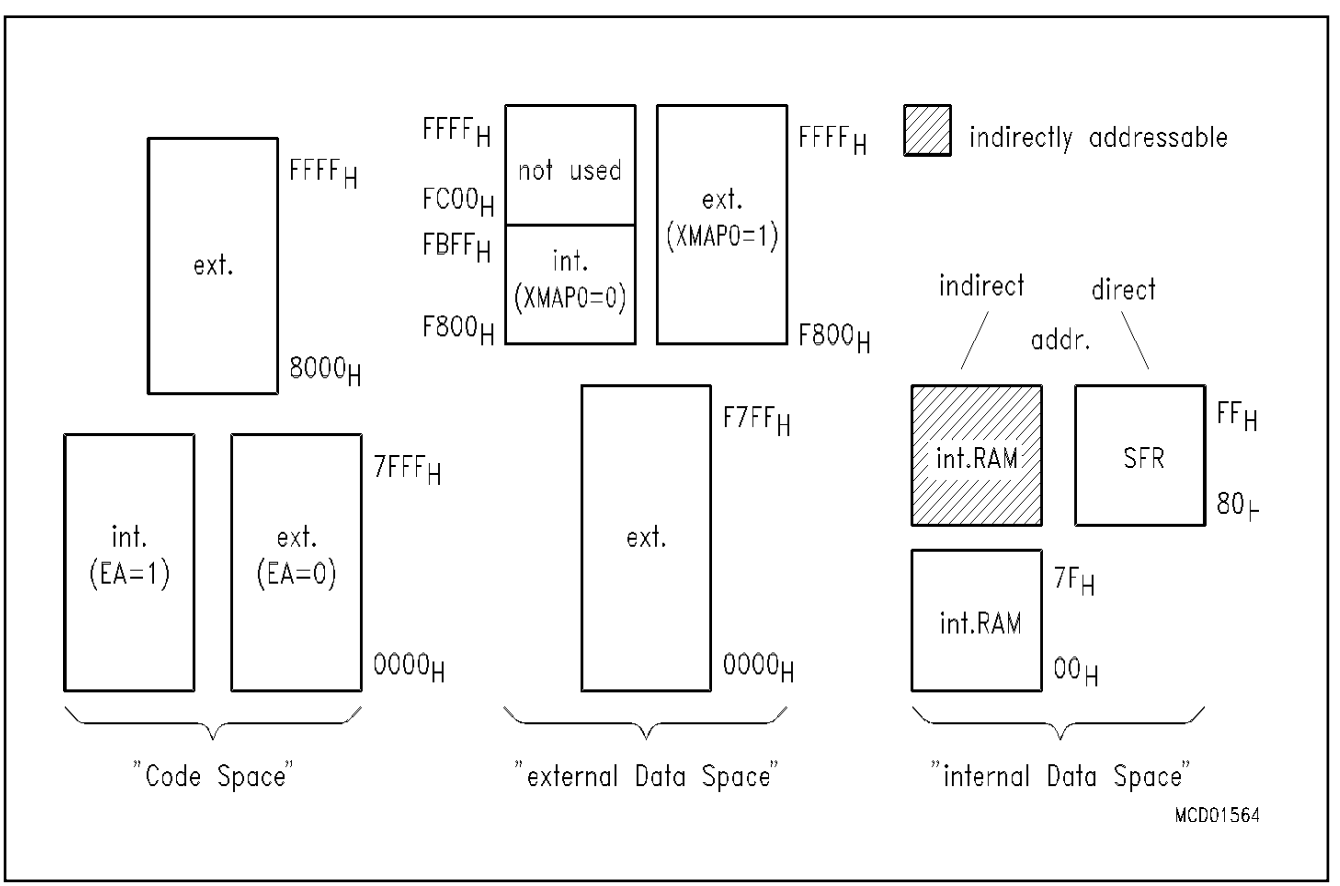


Figure 2
Memory Map

Program Memory ('Code Space')

The SAB 83C515A-5 has 32 Kbyte of on-chip ROM, while the SAB 80C515A has no internal ROM. The program memory can externally be expanded up to 64 Kbyte. Pin $\overline{EA}$ determines whether program fetches below address 8000_H are done from internal or external memory.

As a new feature the SAB 83C515A-5 offers the possibility of protecting the internal ROM against unauthorized access. This protection is implemented in the ROM-Mask. Therefore, the decision ROM-Protection 'yes' or 'no' has to be made when delivering the ROM-Code. Once enabled, there is no way of disabling the ROM-Protection.

Effect: The access to internal ROM done by an externally fetched MOVC instruction is disabled. Nevertheless, an access from internal ROM to external ROM is possible.

To verify the read protected ROM-Code a special ROM-Verify-Mode is implemented. This mode also can be used to verify unprotected internal ROM.

ROM -Protection	ROM-Verification Mode (see 'AC Characteristics')	Restrictions
no	ROM-Verification Mode 1 (standard 8051 Verification Mode) ROM-Verification Mode 2	–
yes	ROM-Verification Mode 2	– standard 8051 Verification Mode is disabled – externally applied MOVC accessing internal ROM is disabled

Data Memory ('Data Space')

The data memory space consists of an internal and an external memory space.The SAB 80C515A contains another 1 Kbyte on On-Chip RAM additional to the 256-bytes internal RAM of the base type SAB 80C515. This RAM is called XRAM ('extended RAM') in this document.

External Data Memory

Up to 64 Kbyte external data memory can be addressed by instructions that use 8-bit or 16-bit indirect addressing. For 8-bit addressing MOVX instructions in combination with registers R0 and R1 can be used. A 16-bit external memory addressing is supported by a 16-bit datapointer. Registers XPAGE and SYSCON are controlling whether data fetches at addresses $F800_H$ to $FBFF_H$ are done from internal XRAM or from external data memory.

Internal Data Memory

The internal data memory is divided into four physically distinct blocks:

– the lower 128 bytes of RAM including four register banks containing eight registers each

– the upper 128 byte of RAM

– the 128 byte special function register area.

– a 1 K $\times$ 8 area which is accessed like external RAM (MOVX-instructions), implemented on chip at the address range from $F800_H$ to $FBFF_H$. Special Function Register SYSCON controls whether data is read from or written to XRAM or external RAM.

A map of the internal data memory is shown in figure 2. The overlapping address spaces of the standard internal data memory (256 byte) are accessed by different addressing modes (see User's Manual SAB 80C515). The stack can be located anywhere in the internal data memory.

Architecture of the XRAM

The contents of the XRAM is not affected by a reset or HW Power Down. After power-up the contents is undefined, while it remains unchanged during and after a reset or HW Power Down if the power supply is not turned off.

The additional On-Chip RAM is logically located in the "external data memory" range at the upper end of the 64 Kbyte address range ($F800_H$-$FBFF_H$). Nevertheless when XRAM is enabled the address range $F800_H$ to $FFFF_H$ is occupied. This is done to assure software compatibility to SAB 80C517A. It is possible to enable and disable (only by reset) the XRAM. If it is disabled the device shows the same behaviour as the parts without XRAM, i.e. all MOVX accesses use the external bus to physically external data memory.

Accesses to XRAM

Because the XRAM is used in the same way as external data memory the same instruction types must be used for accessing the XRAM.

Note: *If a reset occurs during a write operation to XRAM, the effect on XRAM depends on the cycle which the reset is detected at (MOVX is a 2-cycle instruction):*

Reset detection at cycle 1: *The new value will not be written to XRAM. The old value is not affected.*

Reset detection at cycle 2: *The old value in XRAM is overwritten by the new value.*

Accesses to XRAM using the DPTR

There are a Read and a Write instruction from and to XRAM which use one of the 16-bit DPTR for indirect addressing. The instructions are:

MOVX A, @DPTR (Read)

MOVX @DPTR, A (Write)

Normally the use of these instructions would use a physically external memory. However, in the SAB 80C515A the XRAM is accessed if it is enabled and if the DPTR points to the XRAM address space (DPTR $\geq F800_H$).

Accesses to XRAM using the Registers R0/R1

The 8051 architecture provides also instructions for accesses to external data memory range which use only an 8-bit address (indirect addressing with registers R0 or R1). The instructions are:

MOVX A, @Ri (Read)

MOVX @Ri, A (Write)

In application systems, either a real 8-bit bus (with 8-bit address) is used or Port 2 serves as page register which selects pages of 256-byte. However, the distinction, whether Port 2 is used as general purpose I/O or as "page address" is made by the external system design. From the device's point of view it cannot be decided whether the Port 2 data is used externally as address or as I/O data!

Hence, a special page register is implemented into the SAB 80C515A to provide the possibility of accessing the XRAM also with the MOVX @Ri instructions, i.e. XPAGE serves the same function for the XRAM as Port 2 for external data memory.

Special Function Register XPAGE

Addr. 91_H									XPAGE

The reset value of XPAGE is 00_H.
XPAGE can be set and read by software.

The register XPAGE provides the upper address byte for accesses to XRAM with MOVX @Ri instructions. If the address formed from XPAGE and Ri is less than the XRAM address range, then an external access is performed. For the SAB 80C515A the contents of XPAGE must be greater or equal than $F8_H$ in order to use the XRAM. Of course, the XRAM must be enabled if it shall be used with MOVX @Ri instructions.

Thus, the register XPAGE is used for addressing of the XRAM; additionally its contents are used for generating the internal XRAM select. If the contents of XPAGE is less than the XRAM address range then an external bus access is performed where the upper address byte is provided by P2 and not by XPAGE!

Therefore, the software has to distinguish two cases, if the MOVX @Ri instructions with paging shall be used:

a) Access to XRAM:	The upper address byte must be written to XPAGE or P2; both writes selects the XRAM address range.
b) Access to external memory:	The upper address byte must be written to P2; XPAGE will be loaded with the same address in order to deselect the XRAM.

Control of XRAM in the SAB 80C515A

There are two control bits in register SYSCON which control the use and the bus operation during accesses to the additional On-Chip RAM (XRAM).

Special Function Register SYSCON

Addr. $0B1_H$							XMAP1	XMAP0	SYSCON

Bit	Function
XMAP0	Global enable/disable bit for XRAM memory. XMAP0 =0: The access to XRAM (= On-Chip XDATA memory) is enabled. XMAP0 = 1: The access to XRAM is disabled. All MOVX accesses are performed by the external bus (reset state).
XMAP1	Control bit for / $\overline{RD/WR}$signals during accesses to XRAM; this bit has no effect if XRAM is disabled (XMAP0 = 1) or if addresses exceeding the XRAM address range are used for MOVX accesses. XMAP1 = 0: The signals $\overline{RD}$ and $\overline{WR}$ are not activated during accesses to XRAM. XMAP1 = 1: The signals $\overline{RD}$ and $\overline{WR}$ are activated during accesses to XRAM.

Reset value of SYSCON is XXXX XX01B.

The control bit XMAP0 is a global enable/disable bit for the additional On-Chip RAM (XRAM). If this bit is set, the XRAM is disabled, all MOVX accesses use external memory via the external bus. In this case the SAB 80C515A does not use the additional On-Chip RAM and is compatible with the types without XRAM.

XMAP0 is hardware protected by an unsymmetric latch. An unintentional disabling of XRAM could be dangerous since indeterminate values would be read from external bus. To avoid this the XMAP-bit is forced to '1' only by reset. Additionally, during reset an internal capacitor is loaded. So after reset state XRAM is disabled. Because of the load time of the capacitor XMAP0-bit once written to '0' (that is, discharging capacitor) cannot be set to '1' again by software. On the other hand any distortion (software hang up, noise, ...) is not able to load this capacitor, too. That is, the stable status is XRAM enabled. The only way to disable XRAM after it was enabled is a reset.

The clear instruction for XMAP0 should be integrated in the program initialization routine before XRAM is used. In extremely noisy systems the user may have redundant clear instructions.

The control bit XMAP1 is relevant only if the XRAM is accessed. In this case the external $\overline{RD}$ and $\overline{WR}$ signals at P3.6 and P3.7 are not activated during the access, if XMAP1 is cleared. For debug purposes it might be useful to have these signals and the addresses at Ports 0.2 available. This is performed if XMAP1 is set.

The behaviour of Port 0 and P2 during a MOVX access depends on the control bits in register SYSCON and on the state of pin $\overline{EA}$. The table 1 lists the various operating conditions. It shows the following characteristics:

a) Use of P0 and P2 pins during the MOVX access.

   Bus: The pins work as external address/data bus. If (internal) XRAM is accessed, the data written to the XRAM can be seen on the bus in debug mode.

   I/0: The pins work as Input/Output lines under control of their latch.

b) Activation of the $\overline{RD}$ and $\overline{WR}$ pin during the access.

c) Use of internal or external XDATA memory.

The shaded areas describe the standard operation as each 80C51 device without on-chip XRAM behaves.

Table 1:
Behaviour of P0/P2 and $\overline{RD}/\overline{WR}$ during MOVX accesses

		$\overline{EA}$ = 0			$\overline{EA}$ = 1	
		XMAP1, XMAP0			XMAP1, XMAP0	
		00	10	X1	00	10
MOVX @DPTR	DPTR < XRAM address range	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used
	DPTR ≥ XRAM address range	a) P0/P2→BUS ($\overline{WR}$ -Data only) b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→BUS ($\overline{WR}$ -Data only) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→I/0 b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→BUS ($\overline{WR}$ -Data only) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used
MOVX @Ri	XPAGE < XRAM addr. page range	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used
	XPAGE ≥ XRAM addr. page range	a) P0/P2→BUS ($\overline{WR}$ -Data only) P2→I/0 b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→BUS ($\overline{WR}$ -Data only) P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→I/0 b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0→BUS ($\overline{WR}$ -Data only) P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) XRAM is used

modes compatible to 8051 - family

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function registers include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripherals. There are also 128 directly addressable bits within the SFR area. All special function registers are listed in table 2 and table 3.

In table 2 they are organized in numeric order of their addresses. In table 3 they are organized in groups which refer to the functional blocks of the SAB 80C515A.

Table 2
Special Function Register

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80_H	**P0** [1]	**$0FF_H$**	**98_H**	**S0CON** [1]	**00_H**
81_H	SP	07_H	99_H	SBUF	XX_H [2]
82_H	DPL	00_H	$9A_H$	reserved	XX_H [2]
83_H	DPH	00_H	$9B_H$	reserved	XX_H [2]
84_H	(WDTL)		$9C_H$	reserved	XX_H [2]
85_H	(WDTH)		$9D_H$	reserved	XX_H [2]
86_H	WDTREL	00_H	$9E_H$	reserved	XX_H [2]
87_H	PCON	00_H	$9F_H$	reserved	XX_H [2]
88_H	**TCON** [1]	**00_H**	**$A0_H$**	**P2** [1]	**$0FF_H$**
89_H	TMOD	00_H	$A1_H$	reserved	XX_H [2]
$8A_H$	TL0	00_H	$A2_H$	reserved	XX_H [2]
$8B_H$	TL1	00_H	$A3_H$	reserved	XX_H [2]
$8C_H$	TH0	00_H	$A4_H$	reserved	XX_H [2]
$8D_H$	TH1	00_H	$A5_H$	reserved	XX_H [2]
$8E_H$	reserved	XX_H [2]	$A6_H$	reserved	XX_H [2]
$8F_H$	reserved	XX_H [2]	$A7_H$	reserved	XX_H [2]
90_H	**P1** [1]	**$0FF_H$**	**$A8_H$**	**IEN0** [1]	**00_H**
91_H	XPAGE	XX_H [2]	$A9_H$	IP0	00_H
92_H	reserved	XX_H [2]	AA_H	SRELL	$0D9_H$
93_H	reserved	XX_H [2]	AB_H	reserved	XX_H [2]
94_H	reserved	XX_H [2]	AC_H	reserved	XX_H [2]
95_H	reserved	XX_H [2]	AD_H	reserved	XX_H [2]
96_H	reserved	XX_H [2]	AE_H	reserved	XX_H [2]
97_H	reserved	XX_H [2]	AF_H	reserved	XX_H [2]

[1] Bit-addressable special function registers

[2] X means that the value is indeterminate and the location is reserved

Table 2: Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
$B0_H$	**P3** [1]	**$0FF_H$**	**$D0_H$**	**PSW** [1]	**00_H**
$B1_H$	SYSCON	$XXXX\ XX01_B$ [2]	$D1_H$	reserved	XX_H [2]
$B2_H$	reserved	XX_H [2]	$D2_H$	reserved	XX_H [2]
$B3_H$	reserved	XX_H [2]	$D3_H$	reserved	XX_H [2]
$B4_H$	reserved	XX_H [2]	$D4_H$	reserved	XX_H [2]
$B5_H$	reserved	XX_H [2]	$D5_H$	reserved	XX_H [2]
$B6_H$	reserved	XX_H [2]	$D6_H$	reserved	XX_H [2]
$B7_H$	reserved	XX_H [2]	$D7_H$	reserved	XX_H [2]
$B8_H$	**EN1** [1]	**00_H**	**$D8_H$**	**ADCON0**[1]	**00_H**
$B9_H$	IP1	$XX00\ 0000_B$ [2]	$D9_H$	ADDATH	00_H
BA_H	SRELH	$XXXX\ XX11_B$ [2]	DA_H	ADDATL	00_H
BB_H	reserved	XX_H [2]	DB_H	P6	XX_H[2]
BC_H	reserved	XX_H [2]	DV_H	ADCVON1	$XXXX\ 0000_B$ [2]
BD_H	reserved	XX_H [2]	DD_H	reserved	XX_H[2]
BE_H	reserved	XX_H [2]	DE_H	reserved	XX_H[2]
BF_H	reserved	XX_H [2]	DF_H	reserved	XX_H[2]
$C0_H$	**IRCON** [1]	**00_H**	**$E0_H$**	**ACC** [1]	**00_H**
$C1_H$	CCEN	00_H	$E1_H$	reserved	XX_H [2]
$C2_H$	CCL1	00_H	$E2_H$	reserved	XX_H [2]
$C3_H$	CCH1	00_H	$E3_H$	reserved	XX_H [2]
$C4_H$	CCL2	00_H	$E4_H$	reserved	XX_H [2]
$C5_H$	CCH2	00_H	$E5_H$	reserved	XX_H [2]
$C6_H$	CCL3	00_H	$E6_H$	reserved	XX_H [2]
$C7_H$	CCH3	00_H	$E7_H$	reserved	XX_H [2]
$C8_H$	**T2CON** [1]	**00_H**	**$E8_H$**	**P4** [1]	**$0FF_H$**
$C9_H$	reserved	XX_H [2]	$E9_H$	reserved	XX_H [2]
CA_H	CRCL	00_H	EA_H	reserved	XX_H [2]
CB_H	CRCH	00_H	EB_H	reserved	XX_H [2]
CC_H	TL2	00_H	EC_H	reserved	XX_H [2]
CD_H	TH2	00_H	ED_H	reserved	XX_H [2]
CE_H	reserved	XX_H [2]	EE_H	reserved	XX_H [2]
CF_H	reserved	XX_H [2]	EF_H	reserved	XX_H [2]

[1] Bit-addressable special function registers

[2] X means that the value is indeterminate and the location is reserved

Table 2: Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
$F0_H$	**B** [1]	**00_H**	**$F8_H$**	P5 [1]	**$00F_H$**
$F1_H$	reserved	XX_H [2]	$F9_H$	reserved	XX_H [2]
$F2_H$	reserved	XX_H [2]	FA_H	reserved	XX_H [2]
$F3_H$	reserved	XX_H [2]	FB_H		
$F4_H$	reserved	XX_H [2]	FC_H		
$F5_H$	reserved	XX_H [2]	FD_H		
$F6_H$	reserved	XX_H [2]	FE_H		
$F7_H$	reserved	XX_H [2]	FF_H		

[1] Bit-addressable special function registers

[2] X means that the value is indeterminate and the location is reserved

Table 3
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$0E0_H$** [1]	00_H
	B	B-Register	**$0F0_H$** [1]	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	PSW	Program Status Word Register	**$0D0_H$** [1]	00_H
	SP	Stack Pointer	81_H	07_H
A/D-Converter	ADCON0	A/D Converter Control Register 0	**$0D8_H$** [1]	00_H
	ADCON1	A/D Converter Control Register 1	$0DC_H$	$0XXX\ 0000_B$ [3]
	ADDATH	A/D Converter Data Reg. High Byte	$0D9_H$	00_H
	ADDATL	A/D Converter Data Reg. Low Byte	$0DA_H$	00_H
Interrupt System	EN0	Interrupt Enable Register 0	**$0A8_H$** [1]	00_H
	IEN1	Interrupt Enable Register 1	**$0B8_H$** [1]	00_H
	IP0	Interrupt Priority Register 0	$0A9_H$	00_H
	IP1	Interrupt Priority Register 1	$0B9_H$	$XX00\ 0000_B$
	IRCON0	Interrupt Request Control Register	**$0C0_H$** [1]	00_H
	TCON [2]	Timer Control Register	**88_H** [1]	00_H
	T2CON [2]	Timer 2 Control Register	**$0C8_H$**	00_H
Compare/ Capture-Unit (CCU)	CCEN	Comp./Capture Enable Reg.	$0C1_H$	00_H
	CCH1	Comp./Capture Reg. 1, High Byte	$0C3_H$	00_H
	CCH2	Comp./Capture Reg. 2, High Byte	$0C5_H$	00_H
	CCH3	Comp./Capture Reg. 3, High Byte	$0C7_H$	00_H
	CCL1	Comp./Capture Reg. 1, Low Byte	$0C2_H$	00_H
	CCL2	Comp./Capture Reg. 2, Low Byte	$0C4_H$	00_H
	CCL3	Comp./Capture Reg. 3, Low Byte	$0C6_H$	00_H
	CRCH	Com./Rel./Capt. Reg. High Byte	$0CB_H$	00_H
	CRCL	Com./Rel./Capt. Reg. Low Byte	$0CA_H$	00_H
	TH2	Timer 2, High Byte	$0CD_H$	00_H
	TL2	Timer 2, Low Byte	$0CC_H$	00_H
	T2CON	Timer 2 Control Register	**$0C8_H$** [1]	00_H
XRAM	XPAGE	Page Address Register for Extended On Chip RAM	91_H	00_H
	SYSCON	XRAM Control Register	$0B1_H$	$XXXX\ XX01_B$ [3]

[1] Bit-addressable special function registers

[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

[3] X means that the value is indeterminate and the location is reserved

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Ports	P0	Port 0	**80_H** 1)	$0FF_H$
	P1	Port 1	**90_H** 1)	$0FF_H$
	P2	Port 2	**$0A0_H$** 1)	$0FF_H$
	P3	Port 3	**$0B0_H$** 1)	$0FF_H$
	P4	Port 4	**$0E8_H$** 1)	$0FF_H$
	P5	Port 5	**$0F8_H$** 1)	$0FF_H$
	P6	Port 6, Analog/Digital Input	$0DB_H$	
Pow.Sav.Mode	PCON	Power Control Register	87_H	00_H
Serial Channels	ADCON0 2)	A/D Converter Control Reg.	**$0D8_H$** 1)	00_H
	PCON 2)	Power Control Register	87_H	00_H
	SBUF	Serial Channel Buffer Reg.	99_H	$0XX_H$ 3)
	SCON	Serial Channel Control Reg.	**98_H** 1)	00_H
	SRELL	Serial Channel Reload Reg., low byte	AA_H	$D9_H$
	SRELH	Serial Channel Reload Reg., high byte	BA_H	XXXX $XX11_B$ 3)
Timer 0/ Timer 1	TCON	Timer Control Register	**88_H** 1)	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Watchdog	IEN0 2)	Interrupt Enable Register 0	**$0A8_H$** 1)	00_H
	IEN1 2)	Interrupt Enable Register 1	**$0B8_H$** 1)	00_H
	IP0 2)	Interrupt Priority Register 0	$0A9_H$	00_H
	IP1 2)	Interrupt Priority Register 1	$0B9_H$	XX00 0000_B
	WDTREL	Watchdog Timer Reload Reg.	86_H	00_H

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) X means that the value is indeterminate and the location is reserved

A/D Converter

In the SAB 80C515A a new high performance / high-speed 8-channel 10-bit A/D-Converter (ADC) is implemented. Its successive approximation technique provides 7 µs conversion time (f_{OSC} = 16 MHz). The conversion principle is upward compatible to the one used in the SAB 80C515. The main functional blocks are shown in figure 3.

The comparator is a fully differential comparator for a high power supply rejection ratio and very low offset voltages. The capacitor network is binary weighted providing genuine10-bit resolution.

The table below shows the sample time T_S and the conversion time T_C, which are dependend on f_{OSC} and a new prescaler.

f_{OSC} [MHz]	Prescaler	f_{ADC} [MHz]	Sample Time T_S [µs]	Conversion Time (incl. sample time) T_C [µs]
12	÷ 8	1.5	2.67	9.3
	÷ 16	0.75	5.33	18.66
16	÷ 8	2.0	2.0	7.0
	÷ 16	1.0	1.0	14.0
18	÷ 8	–	–	–
	÷ 16	1.125	3.55	12.4

The ADC is clocked (f_{ADC}) with f_{OSC}/8. Because of the ADC's maximum clock frequency of 2 MHz the prescaler (divide-by-2) has to be enabled (set Bit ADCL in SFR ADCON 1) when the oscillator frequency (f_{OSC}) is higher than 16 MHz.

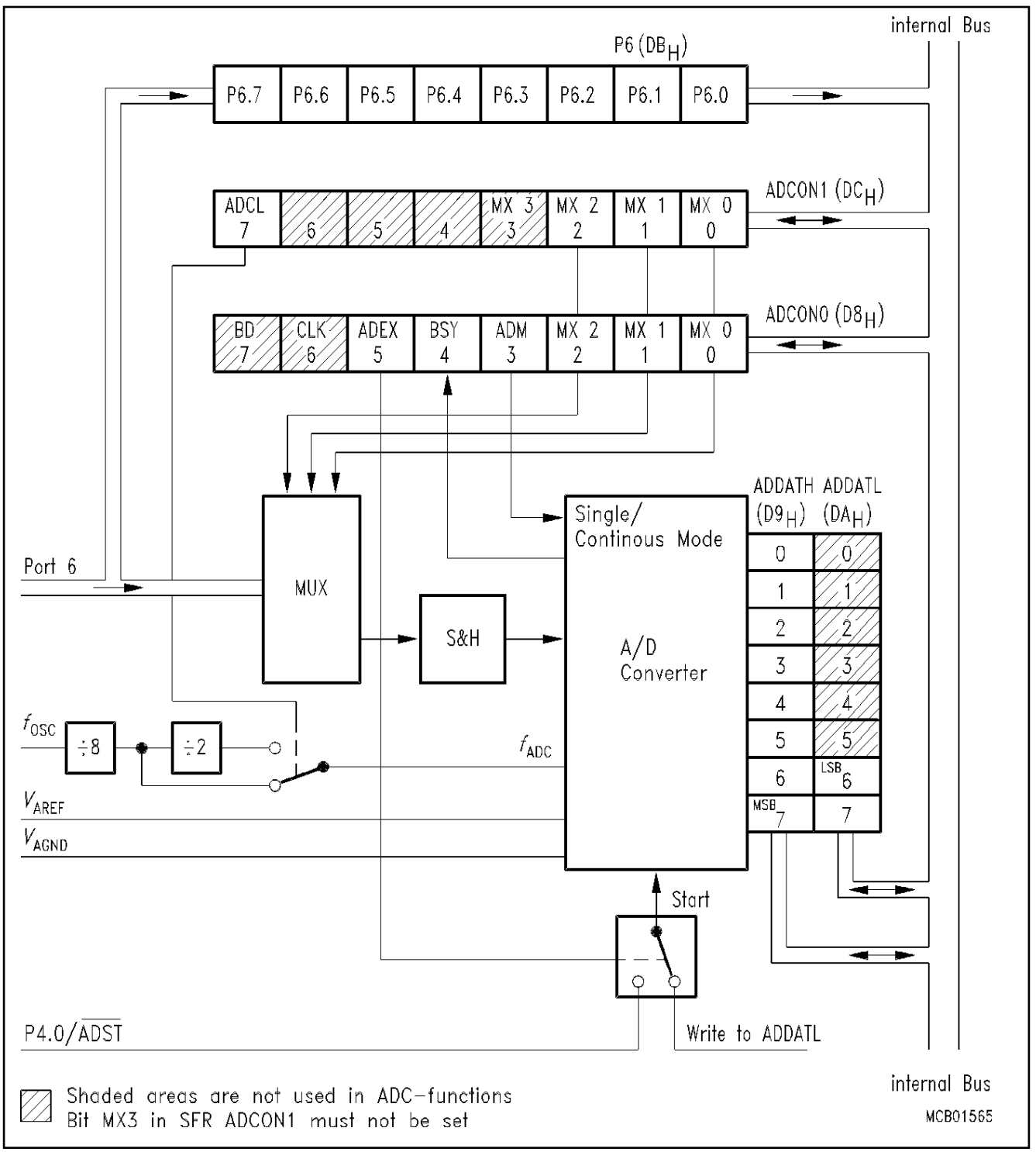


Figure 3
Block Diagram A/D Converter

Timers /Counters

The SAB 80C515A contains three 16-bit timers/counters wich are useful in many applications for timing and counting. the input clock for wach timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

– Timer/Counter 0 and 1

These timers/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto-reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; Timer/counter 1 in this mode holds its count.

External inputs $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

– Timer/Counter 2

Timer/counter 2 of the SAB 80C515A is a 16-bit timer/counter with several additional features. It offers a 2:1 prescaler, a selectable gate function, and compare, capture and reload functions. Corresponding to the 16-bit timer register there are four 16-bit capture/compare registers, one of them can be used to perform a 16-bit reload on a timer overflow or external event. Each of these registers corresponds to a pin of port 1 for capture input/compare output.

Figure 4 shows a block diagram of timer/counter 2.

Reload

A 16-bit reload can be performed with the 16-bit CRC register consisting of CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer 2 overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

Capture

This feature permits saving of the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value of timer 2 registers TL2 and TH2 into a dedicated capture register.

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

Compare

In compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 registers. If the count value in the timer 2 registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to low level when timer 2 overflows.

Mode 1: The transition of the output signal can be determined by software. A timer 2 overflow causes no output change.

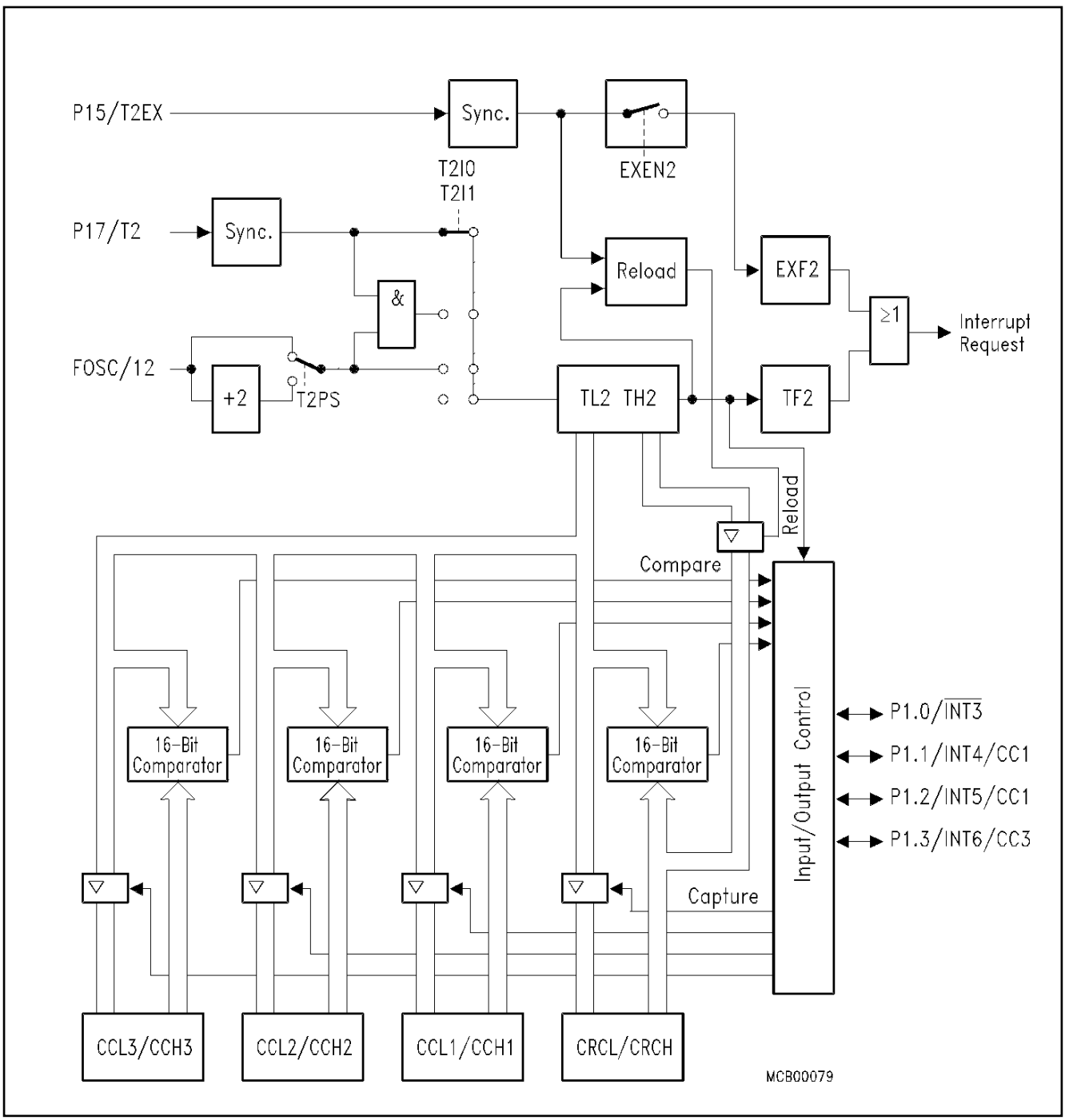


Figure 4
Block Diagram of Timer/Counter 2

Interrupt Structure

The SAB 80C515A has 12 interrupt vectors with the following vector addresses and request flags.

Table 4
Interrupt Sources and Vectors

Source (Request Flags)	Vector Address	Vector
IE0	0003_H	External interrupt 0
TF0	$000B_H$	Timer 0 interrupt
IE1	0013_H	External interrupt 1
TF1	$001B_H$	Timer 1 interrupt
RI + TI	0023_H	Serial port interrupt
TF2 + EXF2	$002B_H$	Timer 2 interrupt
IADC	0043_H	A/D converter interrupt
IEX2	$004B_H$	External interrupt 2
IEX3	0053_H	External interrupt 3
IEX4	$005B_H$	External interrupt 4
IEX5	0063_H	External interrupt 5
IEX6	$006B_H$	External interrupt 6

Each interrupt vector can be individually enabled/disabled. The minimum response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles, if no other interrrupt of the same or a higher priority level is in process.

Figure 5 shows the interrupt request sources.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 3 or 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs. Each pair can be programmed individually to one of four priority levels by setting or clearing one bit in special function register IP0 and one in IP1.

Figure 6 shows the priority level structure.

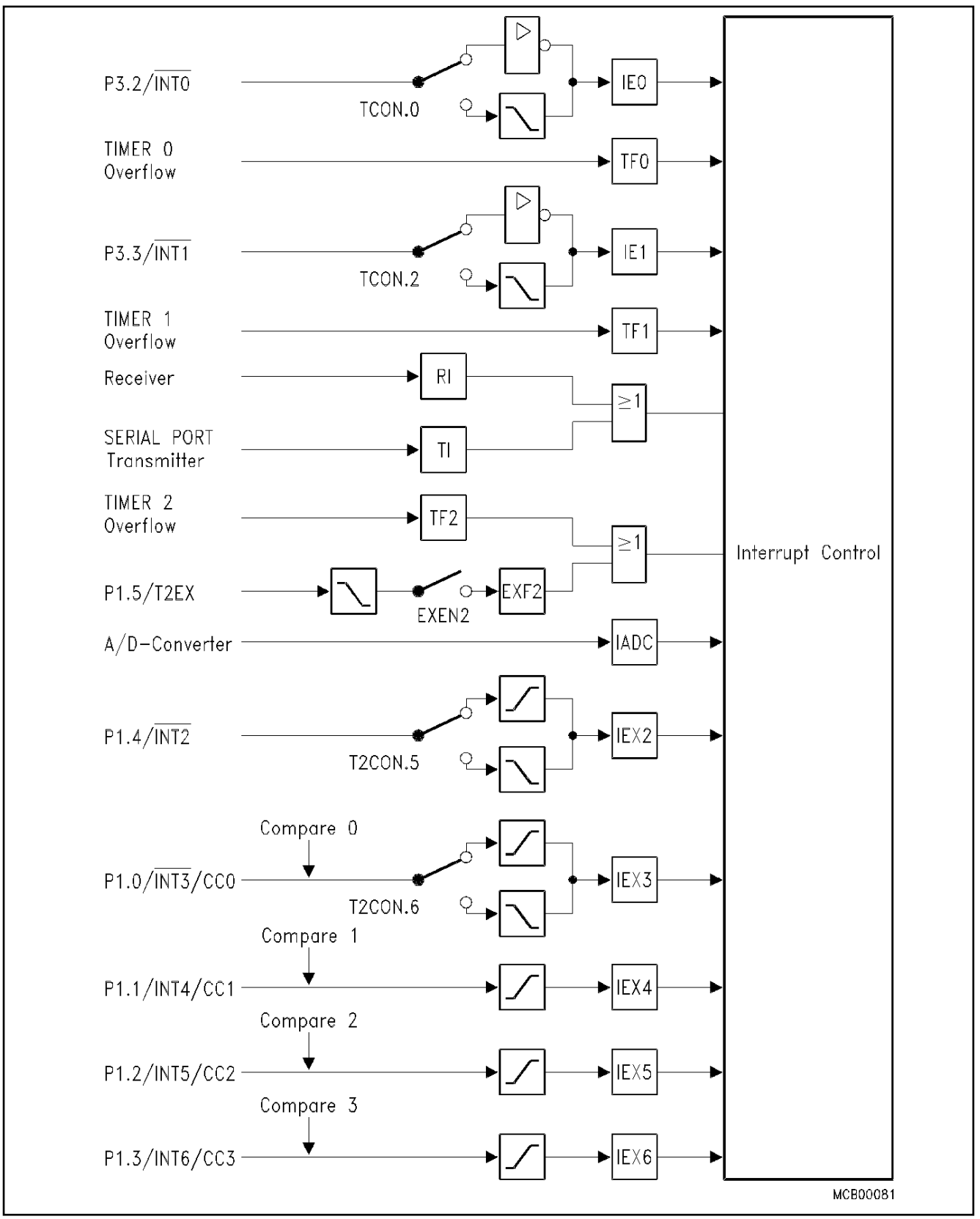


Figure 5
Interrupt Request Sources

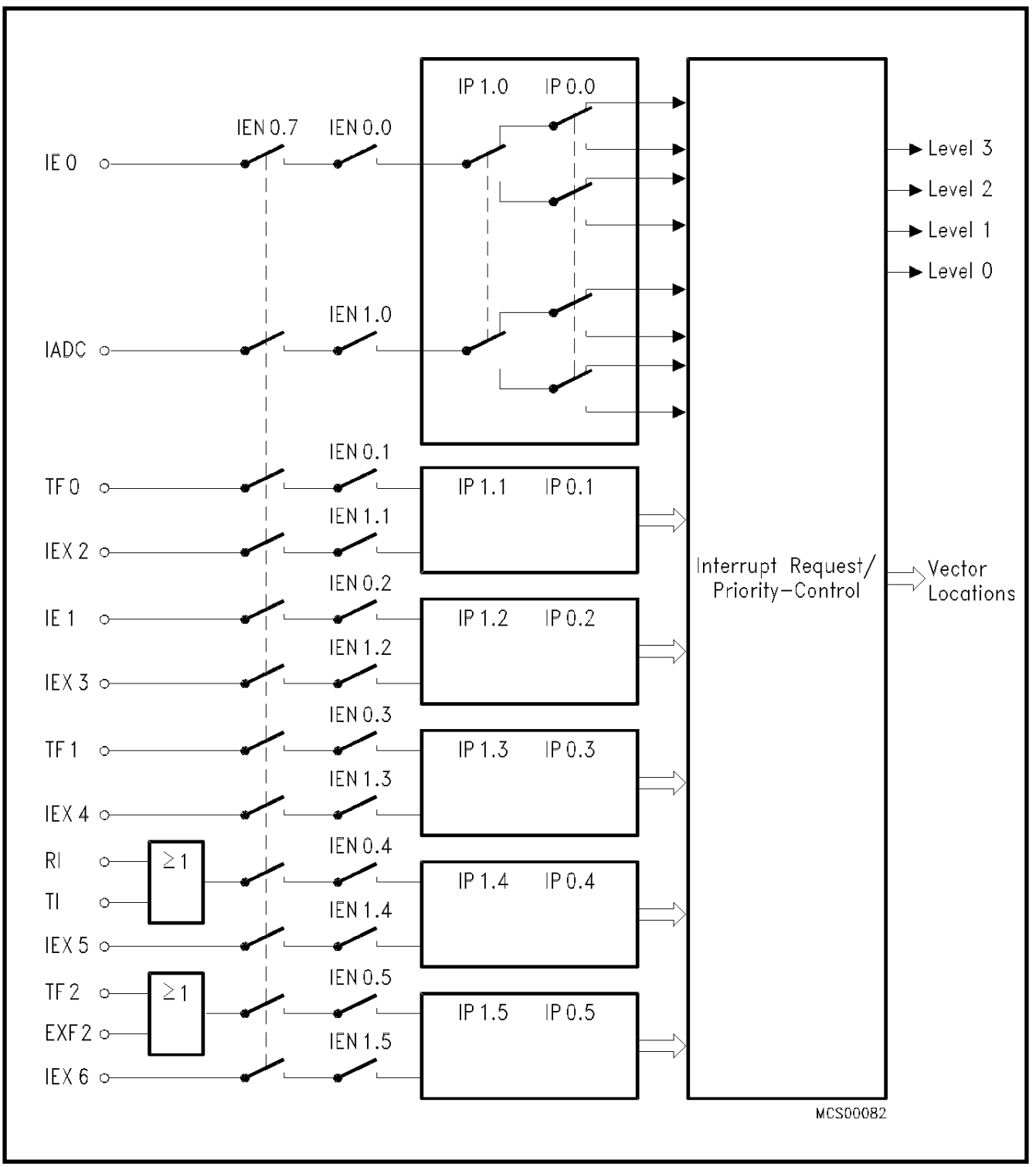


Figure 6
Interrupt Priority Level Structure

I/O Ports

The SAB 80C515A has six 8-bit I/O ports and one input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pull-up resistors. That means, when configured as inputs, ports 1 to 5 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pull-up FET. Ports 1, 3 and 4 are provided for several alternate functions, as listed below:

Port	Symbol	Function
P1.0	$\overline{\text{INT3}}$/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	INT6/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	$\overline{\text{INT2}}$	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external count or gate input
P3.0	RxD	Serial port's receiver data input (asynchronous) or data input /output (synchronous)
P3.1	TxD	Serial port's transmitter data output (asynchronous) or clock output (synchronous)
P3.2	INT0	External interrupt 0 input, timer 0 gate control
P3.3	INT1	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	T1	Timer 1 external counter input
P3.6	WR	External data memory write strobe
P3.7	RD	External data memory read strobe
P4.0	$\overline{\text{ADST}}$	A/D Converter, external start of conversion

The SAB 80C515A has one dual-purpose input port. The ANx lines of port 6 in the SAB 80C515 can individually be used as analog or digital inputs. Reading the special function register P6 allows the user to input the digital values currently applied to the port pins. It is not necessary to select these modes by software; the voltages applied at port 6 pins can be converted to digital values using the A/D converter and at the same time the pins can be read via SFR P6. It must be noted, however, that the results in port P6 bits will be indeterminate if the levels at the corresponding pins are not within their V_{IL}/V_{IH} specifications. Furthermore, it is not possible to use port P6 as an output port. Special function register P6 is located at address $0DB_H$.

In Hardware Power Down Mode the port pins and several control lines enter a floating state. For more details see the section about Hardware Power Down Mode.

Power Saving Modes

The SAB 80C515A provides – due to Siemens ACMOS technology – four modes in which power consumption can be significantly reduced.

- The **Slow Down Mode**
  The controller keeps up the full operating functionality, but is driven with one eight of its normal operating frequency. Slowing down the frequency remarkable reduces power consumption.
- The **Idle Mode**
  The CPU is gated off from the oscillator, but all peripherals are still supplied with the clock and continue working.
- The **Software Power Down Mode**
  Operation of the SAB 80C515A is stopped, the on-chip oscillator and the RC-oscillator are turned off. This mode is used to save the contents of the internal RAM with a very low standby current and is fully compatible to the Power Down Mode of the SAB 80C515.
- The **Hardware Power Down Mode**
  Operation of the SAB 80C515A is stopped, the on-chip oscillator and the RC-oscillator are turned off. The pin $\overline{\text{HWPD}}$ controls this mode. Port pins and several control lines enter a floating state. The Hardware Power Down Mode is new in the SAB 80C515A and is independent of the state of pin $\overline{\text{PE}}$/SWD (which enables only the software initiated power reduction modes).

Hardware Enable for Software controlled Power Saving Modes

A dedicated pin $\overline{\text{PE}}$/SWD of the SAB 80C515A allows to block the Software controlled power saving modes. Since this pin is mostly used in noise-critical application it is combined with an automatic start of the Watchdog Timer.

$\overline{\text{PE}}$/SWD = V_{IH} (logic high level):	Using of the power saving modes is not possible. The watchdog timer starts immediately after reset. The instruction sequences used for entering of power saving modes will not affect the normal operation of the device.
$\overline{\text{PE}}$/SWD = V_{IL} (logic low level):	All power saving moes can be activated by software. The watchdog timer can be started by software at any time.

When left unconnected, pin $\overline{\text{PE}}$/SWD is pulled high by a weak internall pull-up. This is done to provide system protection on default.

The logic-level applied to pin $\overline{\text{PE}}$/SWD can be changed during program execution to allow or to block the use of the power saving modes without any effect on the on-chip watchdog circuitry.

Requirements for Hardware Power Down Mode

There is no dedicated pin to enable the Hardware Power Down Mode. The control pin $\overline{PE}$/SWD has no control function in this mode. It enables and disables only the use of software controlled power saving modes.

Software Controlled Power Saving Modes

All of these modes are entered by software. Special function register PCON (power control register, address is 87_H) is used to select one of these modes.

Slow Down Mode

During slow down operation all signal frequencies that are derived from the oscillator clock, are divided by eight, also the clockout signal and and the watchdog timer count.

The slow down mode is enabled by setting bit SD. The controller actually enters the slow down mode after a short synchronisation period (max. 2 machine cycles).

The slow down mode is disabled by clearing bit SD.

Idle Mode

During idle mode all peripherals of the SAB 80C515A (except for the watchdog timer) are still supplied by the oscillator clock. Thus the user has to take care which peripheral should continue to run and which has to be stopped during Idle.

The procedure to enter the Idle mode is similar to the one entering the power down mode. The two bits IDLE and IDLS must be set by two consecutive instructions to minimize the chance of unintentional activating of the idle mode.

There are two ways to terminate the idle mode:

– The idle mode can be terminated by activating any enabled interrupt. This interrupt will be serviced and the instruction to be executed following the RETI instruction will be the one following the instruction that set the bit IDLS.

– The other way to terminate the idle mode, is a hardware reset. Since the oscillator is still running, the hardware reset must be held active only for two machine cycles for a complete reset.

Normally the port pins hold the logical state they had at the time idle mode was activated. If some pins are programmed to serve their alternate functions they still continue to output during idle mode if the assigned function is on. The control signals ALE and $\overline{PSEN}$ hold at logic high levels (see table 5).

Software Power Down Mode

The power down mode is entered by two consecutive instructions directly following each other. The first instruction has to set the flag PDE (power down enable) and must not set PDS (power down set). The following instruction has to set the start bit PDS. Bits PDE and PDS will automatically be cleared after having been set.

The instruction that sets bit PDS is the last instruction executed before going into power down mode. The only exit from power down mode is a hardware reset.

The status of all output lines of the controller can be looked up in table 5.

Hardware Controlled Power Down Mode

The pin $\overline{\text{HWPD}}$ controls this mode. If it is on logic high level (inactive) the part is running in the normal operating modes. If pin $\overline{\text{HWPD}}$ gets active (low level) the part enters the Hardware Power Down Mode; this is independent of the state of pin $\overline{\text{PE}}$/SWD.

$\overline{\text{HWPD}}$ is sampled once per machine cycle. If it is found active, the device starts a complete internal reset sequence. The watchdog timer is stopped and its status flag WDTS is cleared exactly the same effects as a hardware reset. In this phase the power consumption is not yet reduced. After completion of the internal reset both oscillators of the chip are disabled. At the same time the port pins and several control lines enter a floating state as shown in table 5. In this state the power consumption is reduced to the power down current IPD. Also the supply voltage can be reduced. Table 5 also lists the voltages which may be applied at the pins during Hardware Power Down Mode without affecting the low power consumption.

Termination of HWPD Mode:

This power down state is maintained while pin $\overline{\text{HWPD}}$ is held active. If HWPD goes to high level (inactive state) an automatic start up procedure is performed:

- First the pins leave their floating condition and enter their default reset state (as they had immediately before going to float state).
- Both oscillators are enabled. The oscillator watchdog's RC oscillator starts up very fast (typ. less than 2 ms).
- Because the oscillator watchdog is active it detects a failure condition if the on-chip oscillator hasn't yet started. Hence, the watchdog keeps the part in reset and supplies the internal clock from the RC oscillator.
- Finally, when the on-chip oscillator has started, the oscillator watchdog releases the part from reset with oscillator watchdog status flag set.
  When automatic start of the watchdog was enabled ($\overline{\text{PE}}$/SWD connected to V_{CC}), the Watchdog Timer will start, too (with its default reload value for time-out period).
- The $\overline{\text{Reset}}$ pin overrides the Hardware Power Down function, i.e. if reset gets active during Hardware Power Down it is terminated and the device performs the normal resetfunction.(Thus, pin $\overline{\text{Reset}}$ has to be inactive during Hardware Power Down Mode). function.(Thus, pin $\overline{\text{Reset}}$ has to be inactive during Hardware Power Down Mode).

Table 5
Status of all pins during Idle Mode, Power Down Mode and Hardware Power Down Mode

Pins	Idle Mode Last instruction executed from		Power Down Mode Last instruction executed from		Hardware Power Down
	internal ROM	external ROM	internal ROM	external ROM	Status
P0	Data	float	Data	float [1]	floating [1]
P1	Data alt outputs	Dat alt outputsa	Data last outputs	Data last outputs	
P2	Data	Address	Data	Data	
P3	Data alt outputs	Data alt outputs	Data last output	Data last output	outputs
P4	Data alt outputs	Data alt outputs	Data last outputs	Data last output	disabled
P5	Data alt output	Data alt output	Data last output	Data last output	input
P6	[1]	[1]	[1]	[1]	function
$\overline{EA}$					active input [2]
$\overline{PE}$/SWD					active input pull-up disabled [2]
XTAL1					active output
XTAL2					disabled input function [1]
$\overline{PSEN}$	high	high	low	low	floating output
ALE	high	high	low	low	
V_{AREF} V_{AGND}					active supply pins [3]
$\overline{RESET}$					active input must be high

[1] Applied voltage range at pin $V_{SS} \leq V_{IN} \leq V_{CC}$
[2] $V_{IN} = V_{SS}$ or $V_{IN} = V_{CC}$
[3] $V_{SS} \leq V_{IN} \leq V_{CC}$; $V_{AREF} \geq V_{AGND}$

Serial Interface

The SAB 80C515A has a full duplex and receive buffered serial interface. It is functionally identical with the serial interface of the SAB 8051.

Table 6 shows possible configurations and the according baud rates.

Table 6
Baud Rate Generation

	Mode		Mode 0		
8-Bit synchronous channel	Baud-rate	f_{OSC} =12 MHz	1 MHz		
		f_{OSC} =16 MHz	1.33 MHz		
		f_{OSC} =18 MHz	1.5 MHz		
	derived from		f_{OSC}		
	Mode		**Mode 1**		
8-Bit UART	Baud-rate	f_{OSC} =12 MHz	1 Baud – 62.5 kBaud		183 Baud – 375 kBaud
		f_{OSC} =16 MHz	1 Baud – 83 kBaud		244 Baud – 500 kBaud
		f_{OSC} =18 MHz	1 Baud – 93.7 kBaud		2375 Baud – 562.5 kBaud
	derived from		Timer 1		10-Bit Baudrate Generator
	Mode		**Mode 2**	**Mode 3**	
9-Bit UART	Baud-rate	f_{OSC} =12 MHz	187.5 kBaud/ 375 kBaud	1 Baud – 62.5 kBaud	183 Baud –75 kBaud
		f_{OSC}=16 MHz	250 Baud/ 500 kBaud	1 Baud – 83.3 kBaud	244 Baud – 500 kBaud
		f_{OSC} =18 MHz	281.2 kBaud/ 562.5 kBaud	1 Baud – 93.7 kBaud	275 Baud – 562.5 kBaud
	derived from		$f_{OSC}/2$	Timer 1	10-Bit Baudrate Generator

The Serial Interface can operate in 4 modes:

Mode 0: Shift register mode:
Serial data enters and exits through R × D. T × D outputs the shift clock 8 data bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 8-bit UART, variable baud rate:
10-bit are transmitted (through T × D) or received (through R × D): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On reception, the stop bit goes into RB80 in special function register SCON. The baud rate is variable.

Mode 2: 9-bit UART, fixed baud rate:
11-bit are transmitted (through T × D) or received (through R × D): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). On transmission, the 9th data bit (TB80 in SCON) can be assigned to the value of 0 or 1. For example, the parity bit (P in the PSW) could be moved into TB80 or a second stop bit by setting TB80 to 1. On reception the 9th data bit goes into RB80 in special function register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 9-bit UART, variable baud rate:
11-bit are transmitted (through T × D) or received (through R × D): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). In fact, mode 3 is the same as mode 2 in all respects except the baud rate. The baud rate in mode 3 is variable.

Variable Baud Rates for Serial Interface

Variable baud rates for modes 1 and 3 of serial interface can be derived from either timer 1 or a new dedicated Baudrate Generator.

The baud rate is generated by a free running 10-bit timer with programmable reload register.

$$\text{Mode 1.3 baud rate} = \frac{2^{\text{SMOD}} * f_{\text{OSC}}}{64 * (2^{10} - \text{SREL})}$$

The default value after reset in the reload registers SRELL and SRELH provides a baud rate of 4.8 kBaud (SMOD = 0) or 9.6 kBaud (SMOD = 1) at 12 MHz oscillator frequency. This guarantees full compatibility to the SAB 80C515.

Fail Safe Units

The SAB 80C515A offers enhanced fail safe mechanisms, which allow an automatic recovery from software upset or hardware failure:

– a programmable watchdog timer (WDT), with variable time-out period from 512 µs up to appr. 1.1 s @12 MHz. Upward compatible to SAB 80C515 watchdog timer.

– an oscillator watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into reset state, in case the on-chip oscillator fails; it also controls the restart from the Hardware Power Down Mode and provides the clock for a fast internal reset after power-on.

Programmable Watchdog Timer

The WDT can be activated by hardware or software.

Hardware initialization is done when pin $\overline{PE}$/SWD (Pin 4) is held high during RESET. The SAB 80C515A then starts program execution with the WDT running. Since pin $\overline{PE}$/SWD is only sampled during Reset, the WDT cannot be started externally during normal operation.

Software initialization is done by setting bit SWDT in SFR IEN1.

A refresh of the watchdog timer is done by setting bits WDT (SFR IEN0) and SWDT consecutively. This double instruction sequence has been implemented to increase system security.

When a watchdog timer reset occurs, the watchdog timer keeps on running, but a status flag WDTS (SFR IP0) is set. This flag can also be cleared by software.

Figure 7 shows the block diagram of the programmable Watchdog Timer.

Oscillator Watchdog

The unit serves three functions:

– Monitoring of the on-chip oscillator’s function.
The watchdog monitors the on-chip oscillator’s frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is forced into reset; if the failure condition disappears (i.e. the on-chip oscillator has again a higher frequency than the RC oscillator), the part executes a final reset phase of appr. 0.25 ms in order to allow the oscillator to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.

– Restart from the Hardware Power Down Mode.
If the Hardware Power Down Mode is terminated the oscillator watchdog has to control the correct start-up of the on-chip oscillator and to restart the program. The oscillator watchdog function is only part of the complete Hardware Power Down sequence; however, the watchdog works identically to the monitoring function.

– Fast internal reset after power-on.
In this function the oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. In this case the oscillator watchdog unit also works identically to the monitoring function.

Figure 8 shows the block diagram of the oscillator watchdog unit. It consists of an internal RC oscillator which provides the reference frequency for the frequency comparator.

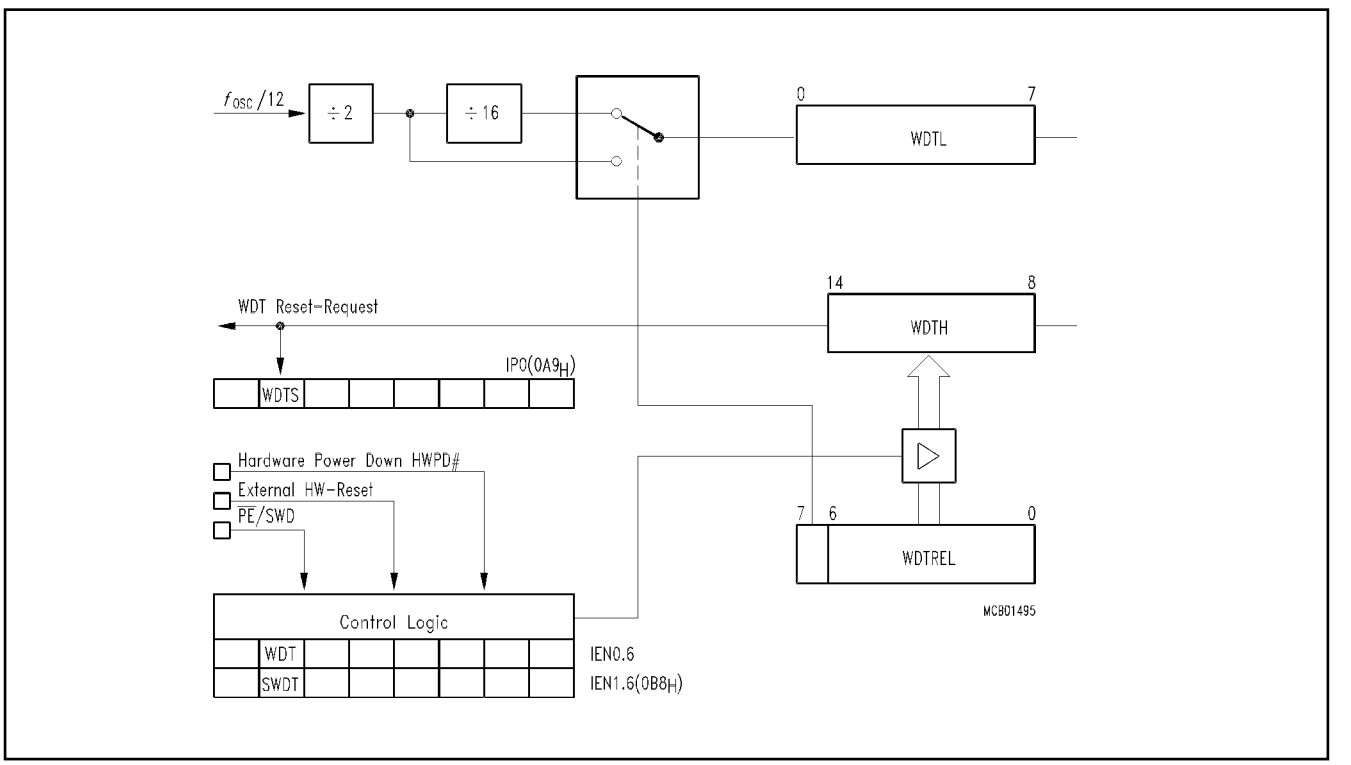


Figure 7
Block Diagram of the Programmable Watchdog Timer

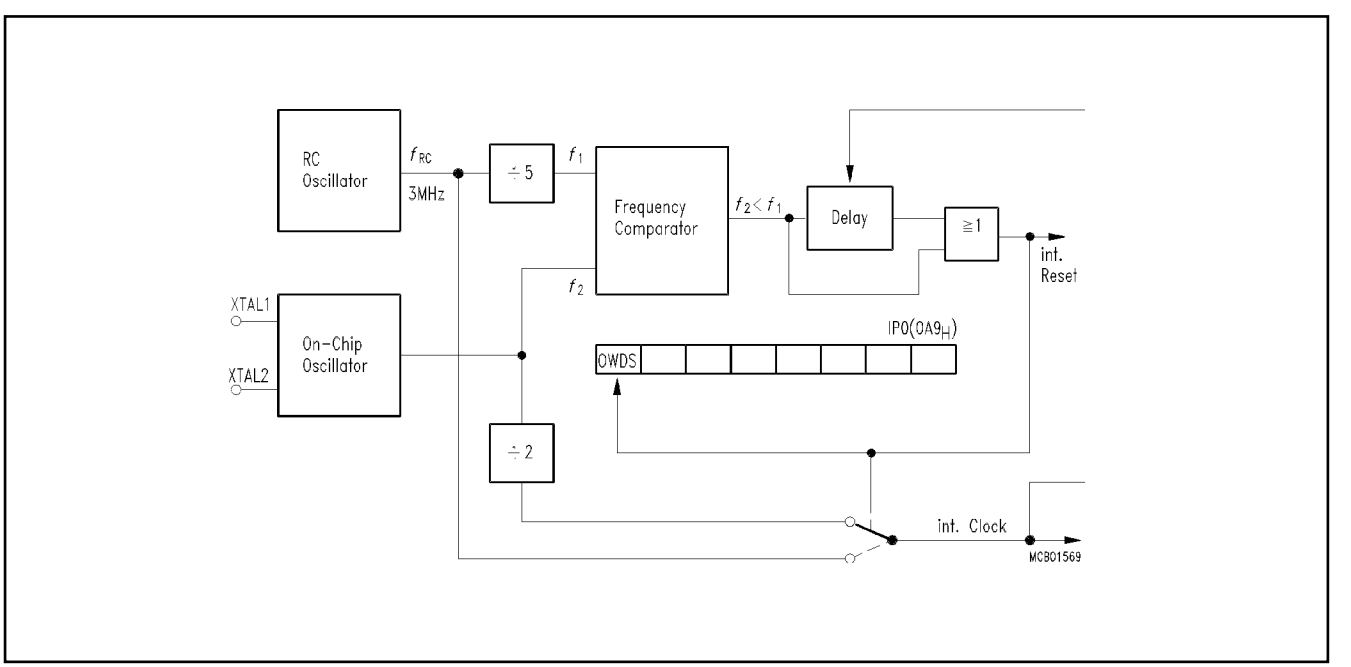


Figure 8
Functional Block Diagram of the Oscillator Watchdog

Fast internal reset after power-on

The SAB 80C515A can use the oscillator watchdog unit for a fast internal reset procedure after power-on.

Normally members of the 8051 family (like the SAB 80C515) enter their default reset state not before the on-chip oscillator starts. The reason is that the external reset signal must be internally synchronized and processed in order to bring the device into the correct reset state. Especially if a crystal is used the start up time of the oscillator is relatively long (typ. 1 ms). During this time period the pins have an undefined state which could have severe effects e.g. to actuators connected to port pins.

In the SAB 80C515A the oscillator watchdog unit avoids this situation. After power-on the oscillator watchdog's RC oscillator starts working within a very short start-up time (typ. less than 2 ms). In the following the watchdog circuitry detects a failure condition for the on-chip oscillator because this has not yet started (a failure is always recognized if the watchdog's RC oscillator runs faster than the on-chip oscillator). As long as this condition is valid the watchdog uses the RC oscillator output as clock source for the chip rather than the on-chip oscillator's output. This allows correct resetting of the part and brings also all ports to the defined state.

Delay time between power-on and correct reset state:

Typ.: 18 µs
Max.: 34 µs

Instruction Set

The SAB 80C515A / 83C515A-5 has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function Registers, Interrupt Vectors and Assembler Directives.

Literature Information

Title	Ordering No.
Microcontroller Family SAB 8051 Pocket Guide	B158-H6497-X-X-7600

Absolute Maximum Ratings

Ambient temperature under bias	– 40 to 85 °C
Storage temperature	– 65 to 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS})	– 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS})	– 0.5 to V_{CC} + 0.5 V
Input current on any pin during overload condition	– 10mA to + 10 mA
Absolute sum of all input currents during overload condition	|100 mA|
Power dissipation	1 W

Note *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) theVoltage on V_{CC} pins with respect to ground (V_{SS}) must not exeed the values definded by the absolute maximum ratings.*

DC Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V
T_A = 0 to 70 °C for the SAB 80C515A
T_A = – 40 to 85 °C for the SAB 80C515A-T3

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Input low voltage (exept $\overline{EA}$,$\overline{RESET}$, $\overline{HWPD}$)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage $\overline{EA}$	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage ($\overline{HWPD}$, $\overline{RESET}$)	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (exept $\overline{RESET}$, XTAL2 and $\overline{HWPD}$)	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL2	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage to $\overline{RESET}$ and $\overline{HWPD}$	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Output low voltage (ports 1, 2, 3, 4, 5)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Output low voltage (ports 0, ALE, $\overline{\text{RESET}}$)	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage, (ports1, 2, 3, 4, 5)	V_{OH}	2.4 0.9 V_{CC}	– –	V V	I_{OH} = – 80 µA I_{OH} = – 10 µA
Output high voltage (port 0 in external bus mode,- ALE, $\overline{\text{PSEN}}$)	V_{OH1}	2.4 0.9 V_{CC}	– –	V V	I_{OH} = – 800 µA I_{OH} = – 80 µA [2]
Logic 0 input current (ports 1, 2, 3, 4, 5)	I_{IL}	– 10	– 70	µA	V_{IN} = 2 V
Logical 1-to-0 transition current, ports 1, 2, 3, 4, 5	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{\text{EA}}$, P6, $\overline{\text{HWPD}}$)	I_{LI}	– –	± 100 ± 150	nA nA	0.45 < V_{IN} < V_{CC} 0.45 < V_{IN} < V_{CC} T_A > 100 °C
Input low current to $\overline{\text{RESET}}$ for reset	I_{IL2}	– 10	– 100	µA	V_{IN} = 0.45 V
Input low current ($\overline{\text{XTAL2}}$)	I_{IL3}	–	– 15	µA	V_{IN} = 0.45 V
Input low current ($\overline{\text{PE}}$/SWD)	I_{IL4}	–	– 20	µA	V_{IN} = 0.45 V
Pin capacitance	C_{IO}	–	10	pF	f_C = 1 MHz, T_A = 25 °C
Power-supply current: Active mode, 12 MHz [7] Active mode, 18 MHz [7] Idle mode, 12 MHz [7] Idle mode, 18 MHz [7] Slow down mode, 12 MHz Slow down mode, 18 MHz Power Down Mode	 $-I_{CC}$ $-I_{CC}$ $-I_{CC}$ $-I_{CC}$ $-I_{CC}$ $-I_{CC}$ $-I_{PD}$	 – – – – – – –	 26 35 11.8 14.2 9 10 50	 mA mA mA mA mA mA µA	 V_{CC} = 5 V [4] V_{CC} = 5 V [4] V_{CC} = 5 V [5] V_{CC} = 5 V [5] V_{CC} = 5 V [6] V_{CC} = 5 V [6] V_{CC} = 2 ... 5.5 V [3]

Notes see page 43.

Notes for page 42:

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1, 3, 4 and 5. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (Software Power Down Mode) is measured under following conditions:
$\overline{EA}$ = $\overline{RESET}$ = V_{CC}; Port0 = Port6 = V_{CC}; XTAL1 = N.C.; XTAL2 = V_{SS};
$\overline{PE}$/SWD = V_{SS}; $\overline{HWPD}$ = V_{CC}; V_{AGND} = V_{SS}; V_{ARef} = V_{CC}; all other pins are disconnected.
I_{PD} (Hardware Power Down Mode): independent of any particular pin connection.

4) I_{CC} (active mode) is measured with:
XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL1 = N.C.;
$\overline{EA}$ = $\overline{PE}$/SWD = V_{CC}; Port0 = Port6 = V_{CC}; $\overline{HWPD}$ = V_{CC}; $\overline{RESET}$ = V_{SS};
all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL1 = N.C.; $\overline{RESET}$ = V_{CC}; $\overline{HWPD}$ = V_{CC}; Port0 = Port6 = V_{CC}; $\overline{EA}$ = $\overline{PE}$/SWD = $V_{SS;}$ all other pins are disconnected;

6) I_{CC} (slow down mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL1 = N.C.; $\overline{RESET}$ = V_{CC}; $\overline{HWPD}$ = V_{CC}; Port6 = V_{CC}; $\overline{EA}$ = $\overline{PE}$/SWD = V_{SS}; all other pins are disconnected;

7) I_{CC} Max at other frequencies is given by:
active mode: I_{CC} (max) = 1.5 * f_{OSC} + 8
idle mode: I_{CC} (max)= 0.4 * f_{OSC} + 7
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

A/D Converter Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V
V_{AREF} = V_{CC} ± 5 %; V_{AGND} = V_{SS} ± 0.2 V;
T_A = 0 to 70 °C for the SAB 80C515A/83C515A-5
T_A = – 40 to 85 °C for the SAB 80C515A-T3/83C515A-5-T3

Parameter	Symbol	Limit values			Unit	Test condition
		min.	typ.	max.		
Analog input capacitance	C_I		25	70	pF	
Sample time (inc. load time)	T_S			4 t_{CY} [1]	µs	[2]
Conversion time (inc. sample time)	T_C			14 t_{CY} [1]	µs	[3]
Total unadjusted error	TUE			± 2	LSB	V_{AREF} = V_{CC} V_{AGND} = V_{SS}
V_{AREF} supply current	I_{REF}		± 20		µA	

1) t_{CY} = (8*2^{ADCL}) /f_{OSC}; (t_{CY} = 1/f_{ADC}; f_{ADC} = f_{OSC}/(8*2^{ADCL}))
2) This parameter specifies the time during the input capacitance C_I, can be charged/discharged by the external source. It must be guaranteed, that the input capacitance C_I, is fully loaded within this time. 4TCY is 2 µs at the f_{OSC}= 16 MHz. After the end of the sample time T_S, changes of the analog input voltage have no effect on the conversion result.
3) This parameter includes the sample time T_S. 14TCY is 7 µs at f_{OSC} = 16 MHz.

AC Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB 80C515A/83C515A-5

T_A = – 40 to 85 °C for the SAB 80C515A-T3/83C515A-5-T3

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Parameter	Symbol	Limit values				Unit
		18 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 18 MHz		
		min.	max.	min.	max.	

Program Memory Characteristics

ALE pulse width	t_{LHLL}	71	–	$2\,t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	26	–	$t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX}	26	–	$t_{CLCL} - 30$	–	ns
ALE to valid instruction in	t_{LLIV}	–	122	–	$4\,t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	31	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	132	–	$3\,t_{CLCL} - 35$	–	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	–	92	–	$3\,t_{CLCL} - 75$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} *)	–	46	–	$t_{CLCL} - 10$	ns
Address valid after $\overline{PSEN}$	t_{PXAV} *)	48	–	$t_{CLCL} - 8$	–	ns
Address to valid instruction in	t_{AVIV}	–	218	–	$5\,t_{CLCL} - 60$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

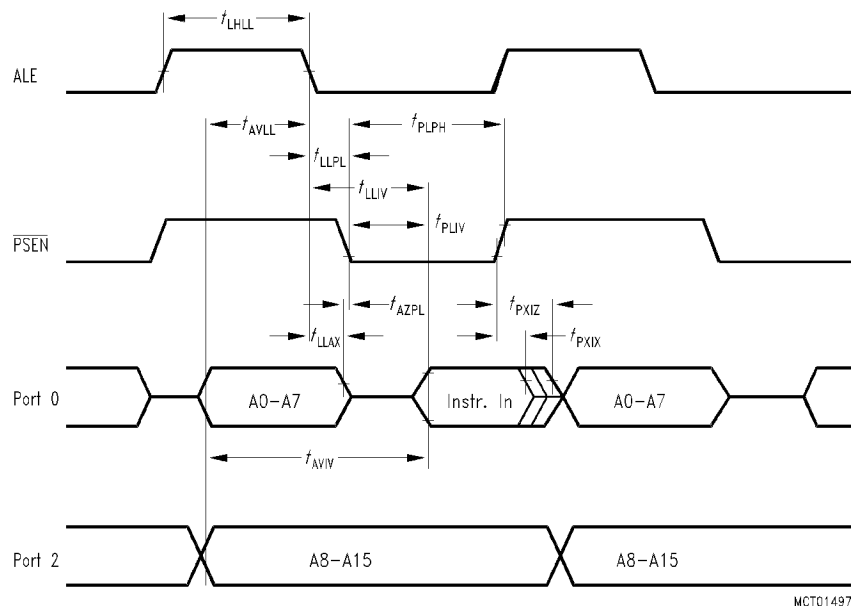
*) Interfacing the SAB 80C515A to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

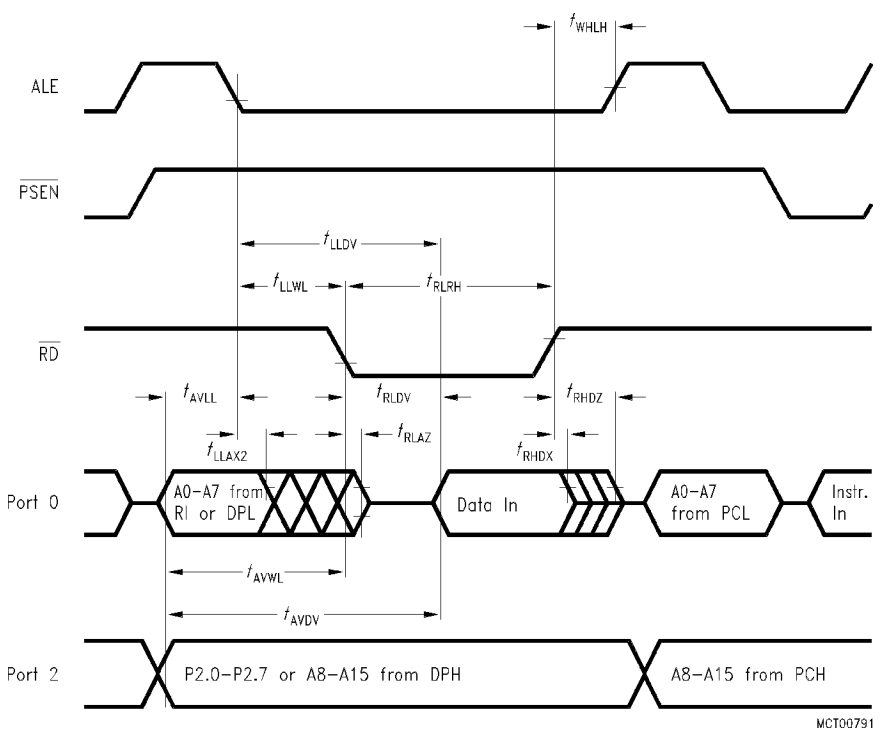
Parameter	Symbol	Limit values				Unit
		18 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 18 MHz		
		min	max.	min.	max.	

External Data Memory Characteristics

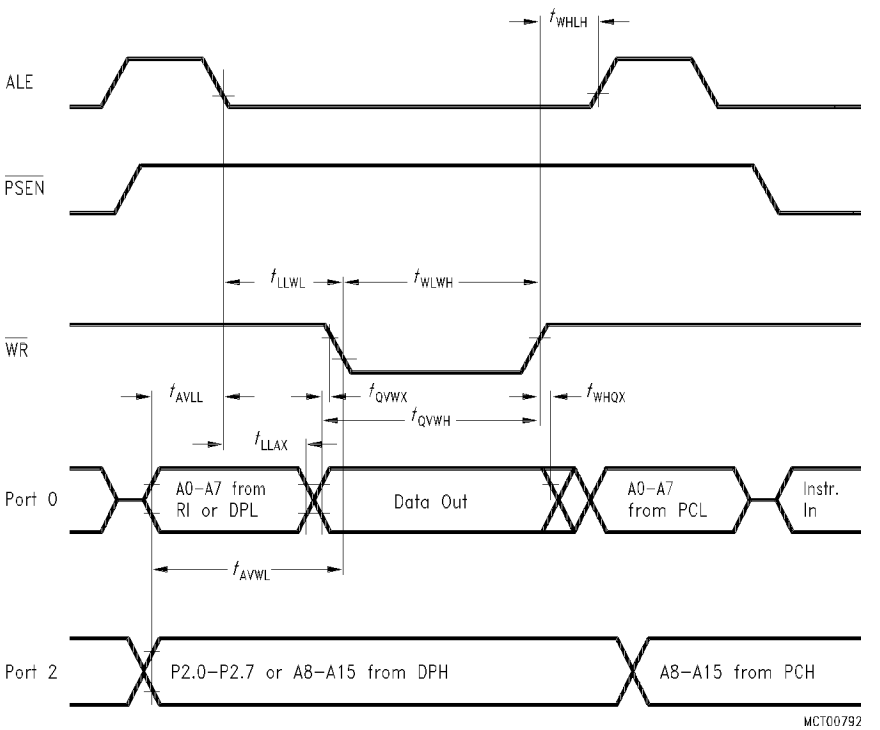
$\overline{RD}$ pulse width	t_{RLRH}	233	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	233	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	81	–	2 t_{CLCL} – 30	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	128	–	5 t_{CLCL} – 150	ns
DATA hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	51	–	2 t_{CLCL} – 60	ns
ALE to valid data in	t_{LLDV}	–	294	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	335	–	9 t_{CLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	117	217	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	16	96	t_{CLCL} – 40	t_{CLCL} + 40	ns
Address valid to $\overline{WR}$	t_{AVWL}	92	–	4 t_{CLCL} – 130	–	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	11	–	t_{CLCL} – 45	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	239	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	16	–	t_{CLCL} – 40	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns



Program Memory Read Cycle



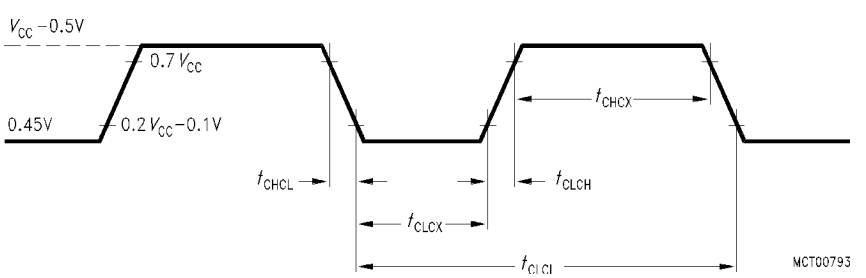
Data Memory Read Cycle



Data Memory Write Cycle

AC Characteristics (cont'd)

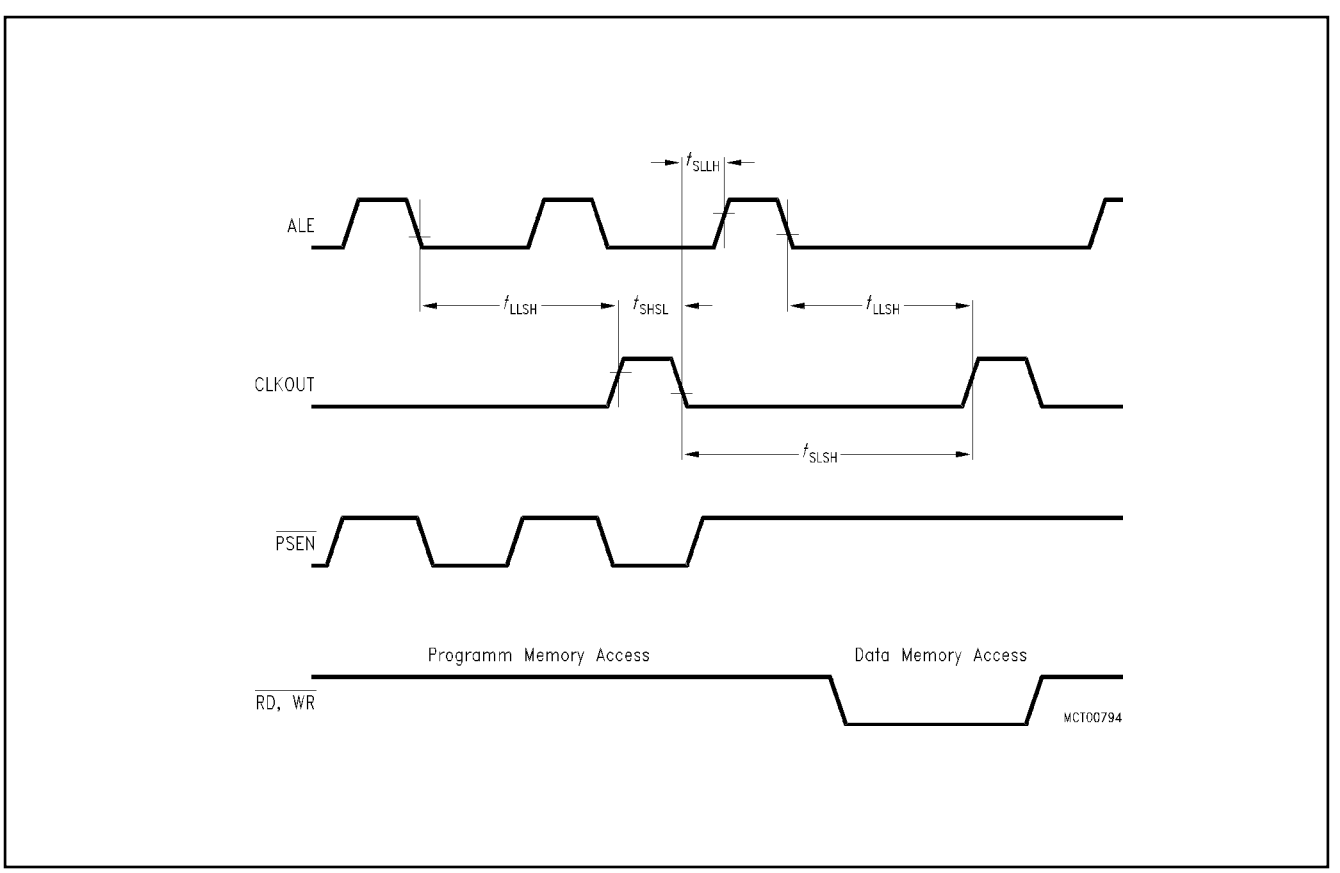
Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 3.5 MHz to 18 MHz		
		min.	max.	
External Clock Drive				
Oscillator period	t_{CLCL}	55.6	285	ns
High time	t_{CHCX}	20	t_{CLCL}-t_{CLCX}	ns
Low time	t_{CLCX}	20	t_{CLCL}-t_{CHCX}	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns
Oscillator frequency	$1/t_{CLC}$	3.5	18	MHz



External Clock Cycle

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		18 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 18 MHz		
		min.	max.	min.	max.	
System Clock Timing						
ALE to CLKOUT	t_{LLSH}	349	–	7 t_{CLCL} – 40	–	ns
CLKOUT high time	t_{SHSL}	71	–	2 t_{CLCL} – 40	–	ns
CLKOUT low time	t_{SLSH}	516	–	10 t_{CLCL} – 40	–	ns
CLKOUT low to ALE high	t_{SLLH}	16	96	t_{CLCL} – 40	t_{CLCL} + 40	ns



System Clock Timing

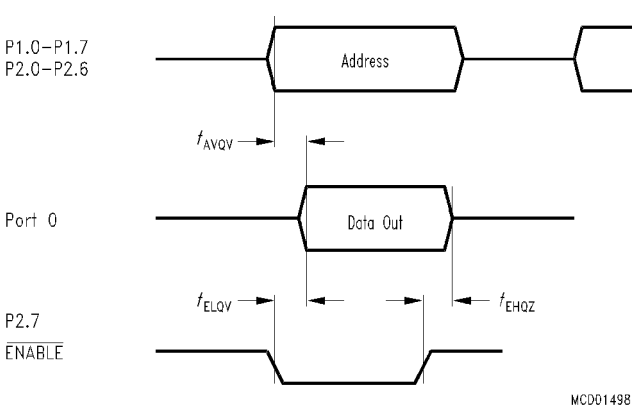
ROM Verification Characteristics

T_A = 25 °C ± 5 °C; V_{CC} = 5 V +10 %, – 15 %; V_{SS} = 0 V

Parameter	Symbol	Limit values		Unit
		min.	max.	

ROM Verification Mode 1 (Standard Verify Mode for not Read Protected ROM)

Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns
ENABLE to valid data	t_{ELQV}	–	48 t_{CLCL}	ns
Data float after ENABLE	t_{EHOZ}	0	48 t_{CLCL}	ns
Oscillator frequency	1/t_{CLCL}	4	6	MHz

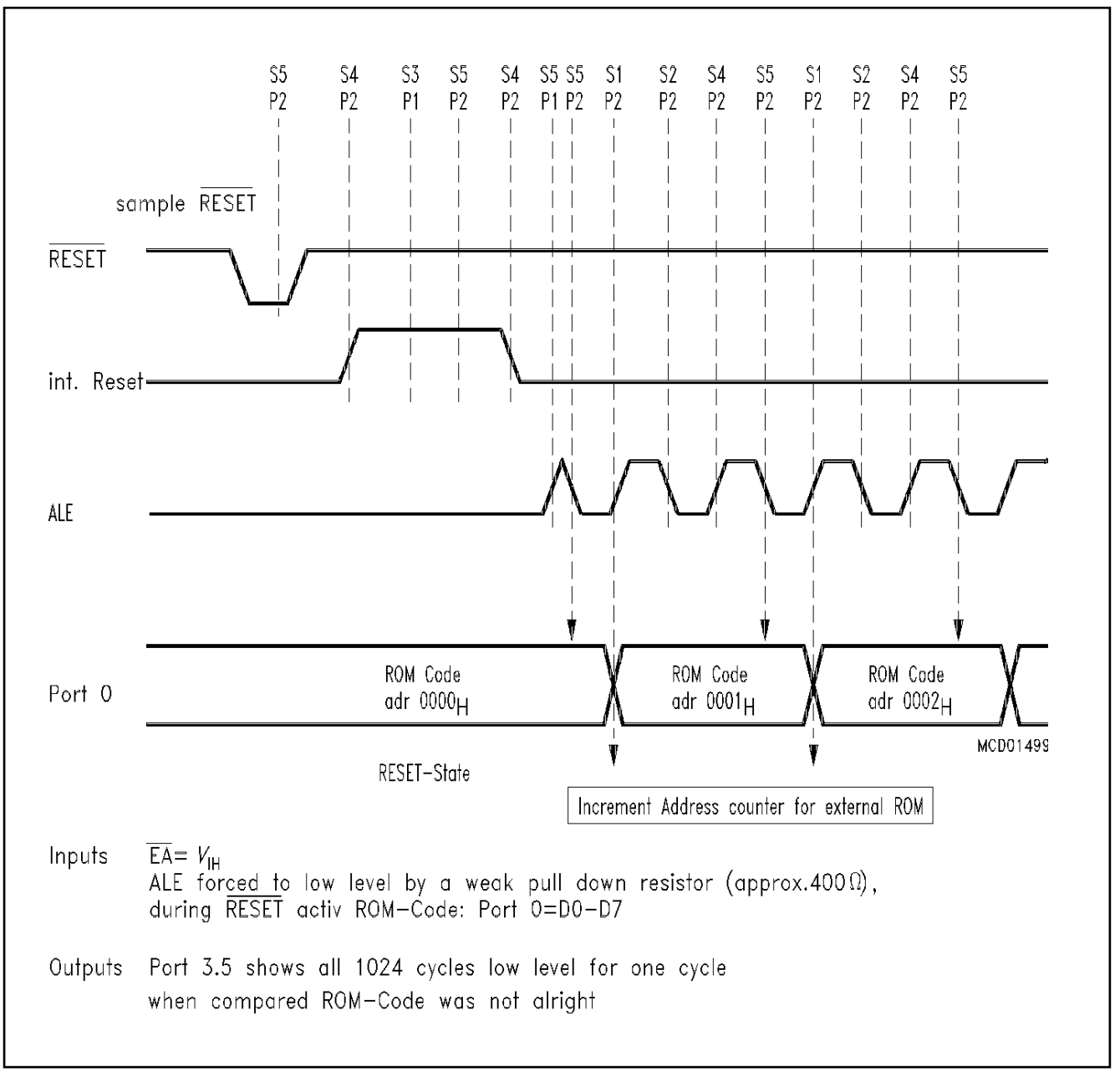


Address: P1.0–P1.7=A0–A7
P2.0–P2.6=A8–A14
Data: P0.0–0.7=D0–D7

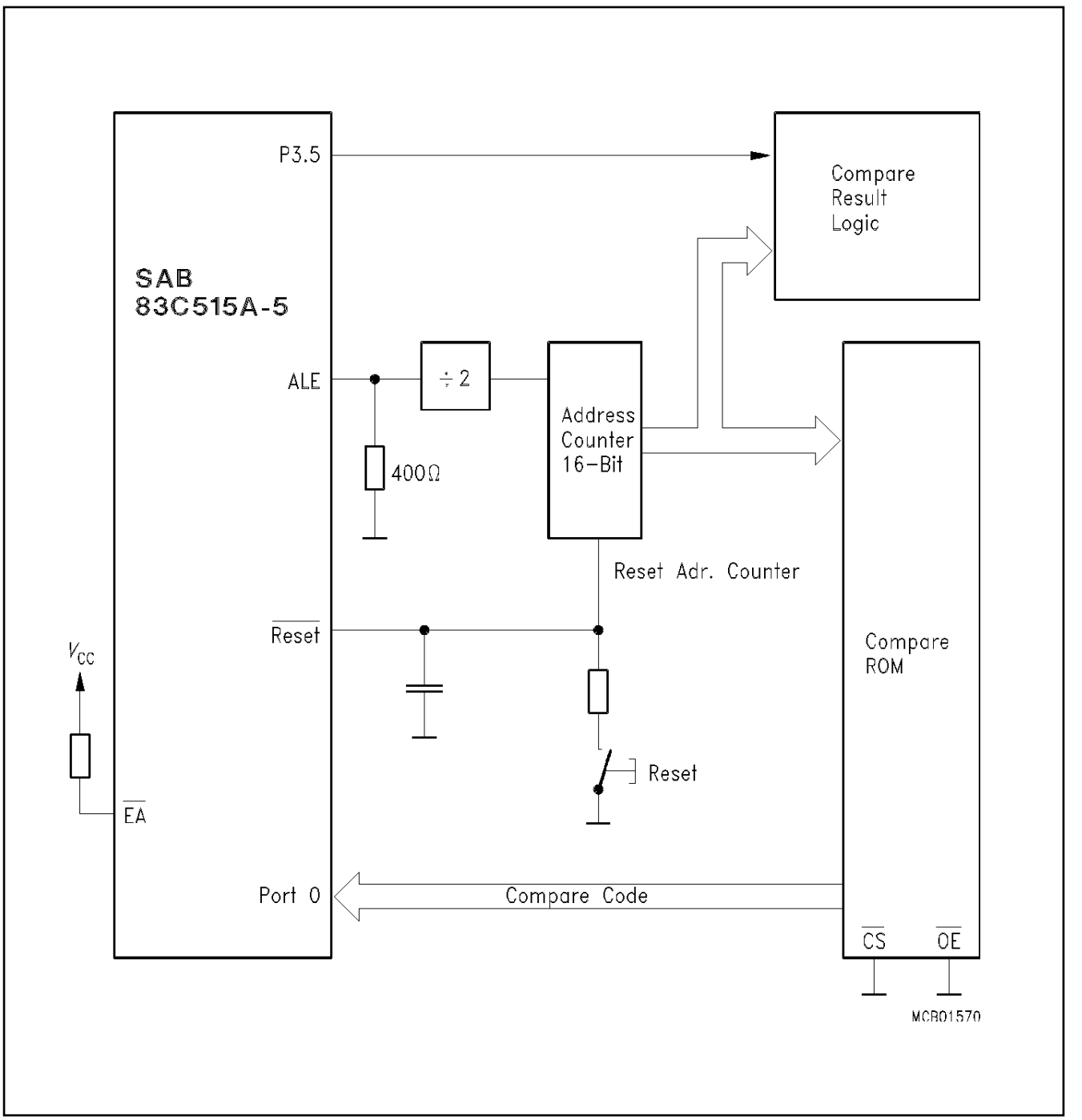
Inputs $\overline{PSEN}$ = V_{SS}
ALE,$\overline{EA}$ = V_{IH}
$\overline{RESET}$ = V_{IL}

ROM Verification Mode 1

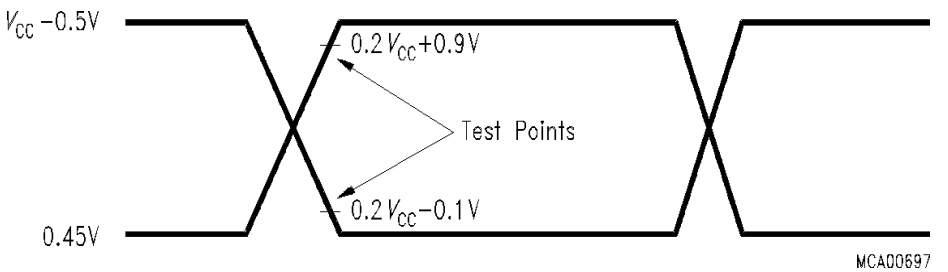
ROM Verification Mode 2 (New Verify Mode for Protected and not Protected ROM)



ROM Verification Mode 2

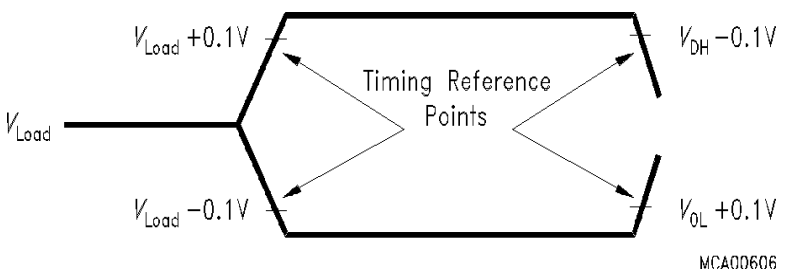


Application Example for Verifying the Internal ROM with ROM Verify Mode 2



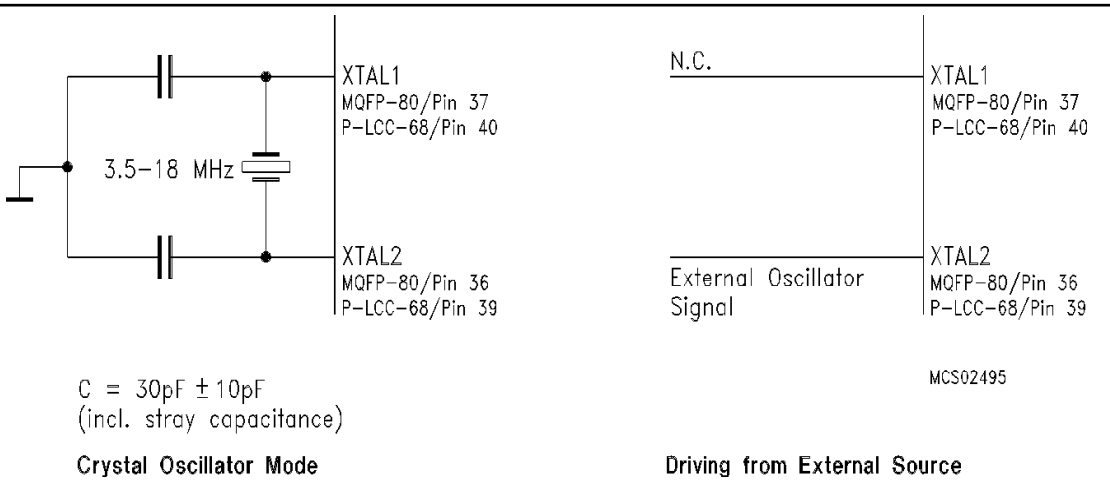
AC Inputs during testing are driven at V_{CC} – 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

AC Testing: Float Waveforms



Recommended Oscillator Circuits

SIEMENS

High-Performance 8-Bit CMOS Single-Chip Microcontroller

SAB 80C517A/83C517A-5

Preliminary

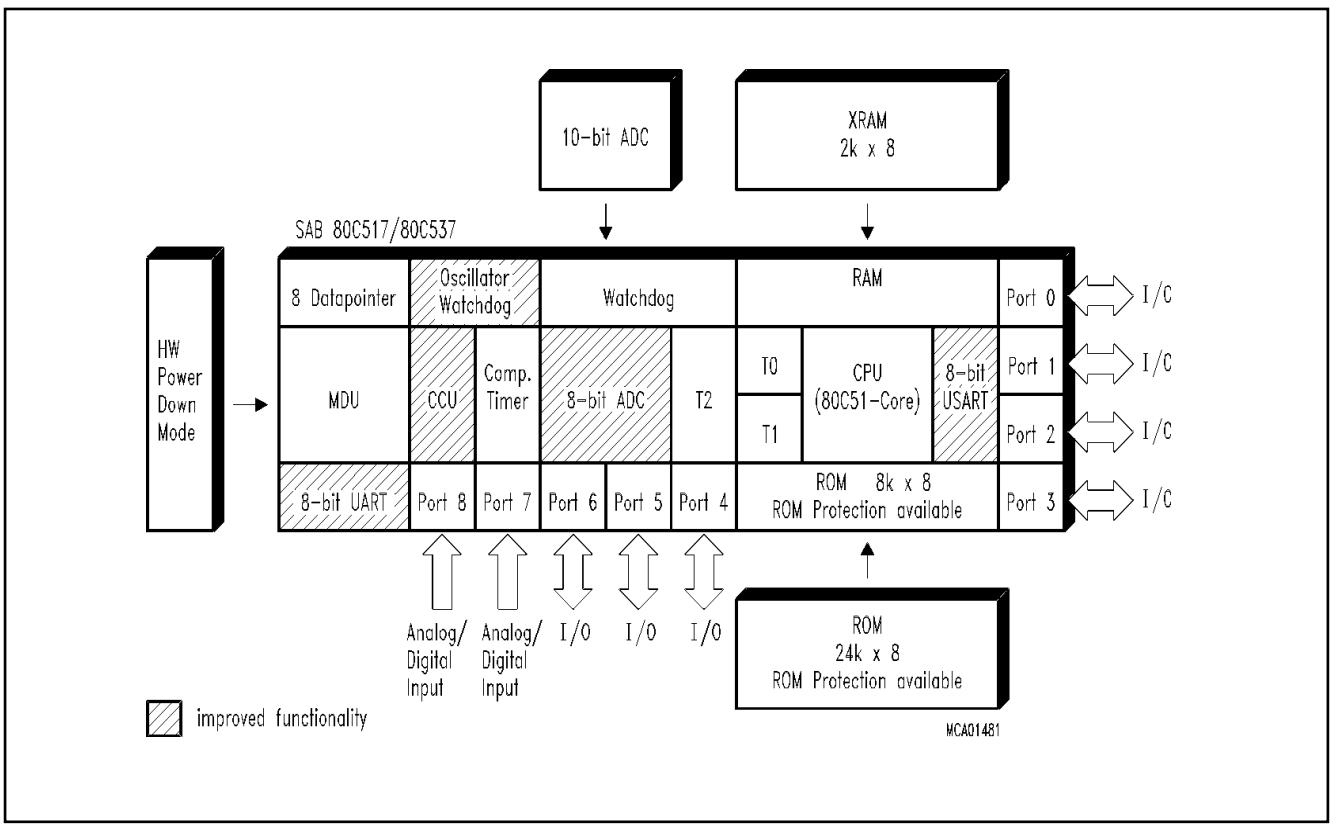
SAB 83C517A-5	Microcontroller with factory mask-programmable ROM
SAB 80C517A	Microcontroller for external ROM

- SAB 80C517A/83C517A-5, up to 18 MHz operation
- 32 K × 8 ROM (SAB 83C517A-5 only, ROM-Protection available)
- 256 × 8 on-chip RAM
- 2 K × 8 on-chip RAM (XRAM)
- Superset of SAB 80C51 architecture:
  - 1 µs instruction cycle time at 12 MHz
  - 666 ns instruction cycle time at 18 MHz
  - 256 directly addressable bits
  - Boolean processor
  - 64 Kbyte external data and program memory addressing
- Four 16-bit timer/counters
- Powerful 16-bit compare/capture unit (CCU) with up to 21 high-speed or PWM output channels and 5 capture inputs
- Versatile "fail-safe" provisions
- Fast 32-bit division, 16-bit multiplication, 32-bit normalize and shift by peripheral MUL/DIV unit (MDU)
- Eight data pointers for external memory addressing
- Seventeen interrupt vectors, four priority levels selectable
- Genuine 10-bit A/D converter with 12 multiplexed inputs
- Two full duplex serial interfaces with programmable Baudrate-Generators
- Fully upward compatible with SAB 80C515, SAB 80C517, SAB 80C515A
- Extended power saving mode
- Fast Power-On Reset
- Nine ports: 56 I/O lines, 12 input lines
- Three temperature ranges available:
  0 to 70 °C (T1)
  – 40 to 85°C (T3)
  – 40 to 110°C (T4)
- Plastic packages: P-LCC-84, P-MQFP-100-2

The SAB 80C517A/83C517A-5 is a high-end member of the Siemens SAB 8051 family of microcontrollers. It is designed in Siemens ACMOS technology and based on SAB 8051 architecture. ACMOS is a technology which combines high-speed and density characteristics with low-power consumption or dissipation.

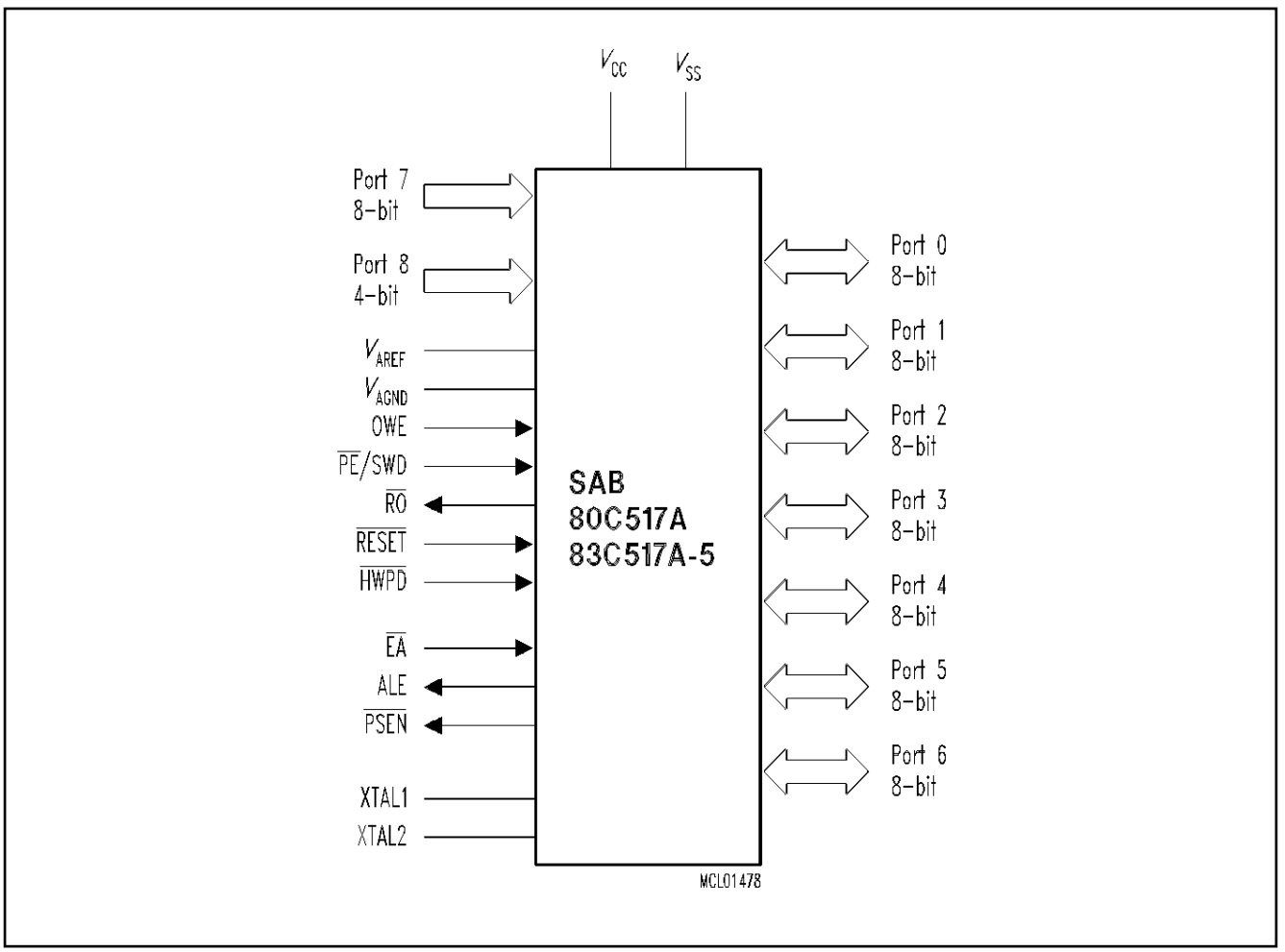
While maintaining all the SAB 80C517 features and operating characteristics the SAB 80C517A is expanded in its "fail-safe" characteristics and timer capabilities.The SAB 80C517A is identical with the SAB 83C517A-5 except that it lacks the on-chip program memory. The SAB 80C517A/83C517A-5 is supplied in a 84-pin plastic leaded chip carrier package (P-LCC-84) and in a 100-pin plastic quad flat package (P-MQFP-100-2).

SAB 80C517A/83C517A-5 **Revision History 05.94**	
Previous Releases	01.94/08.93/11.92/10.91/04.91
Page	Subjects (changes since last revision 04.91)
5 4 6-14 several 2 25,26,30 33 39 57 60 62 65 several 66 68	– Pin configuration P-MQFP-100-2 added – Pin differences updated – Pin numbers for P-MQFP-100-2 package added – Correction of P-MRFP-100 into P-MQFP-100-2 – Ordering information for -40 to +110°C versions – Correction of register names S0RELL, SCON, ADCON, ICRON, and SBUF – Figure 4 corrected – Figure 8 corrected – $\overline{PE}$/SWD function description completed – Correct ordering numbers – Test condition for V_{OH}, V_{OH1} corrected – t_{PXIZ} name corrected t_{AVIV}, t_{AZPL} values corrected – Minimum clock frequence is now 3.5 MHz – t_{QVWH} (data setup before $\overline{WR}$) corrected and added – t_{LLAX2} corrected
Page	Subjects (changes since last revision 08.93)
25 51 65 67 74	– Corrected SFR name S0RELL – Below "Termination of HWPD Mode": 4th paragraph with ident corrected – Description of t_{LLIV} corrected – Program Memory Read Cycle: t_{PXAV} added – Oscillator circuit drawings: MQFP-100-2 pin numbers added.
Page	Subjects (changes since last revision 01.94)
 47	– Minor changes on several pages – Table 6 corrected



Ordering Information

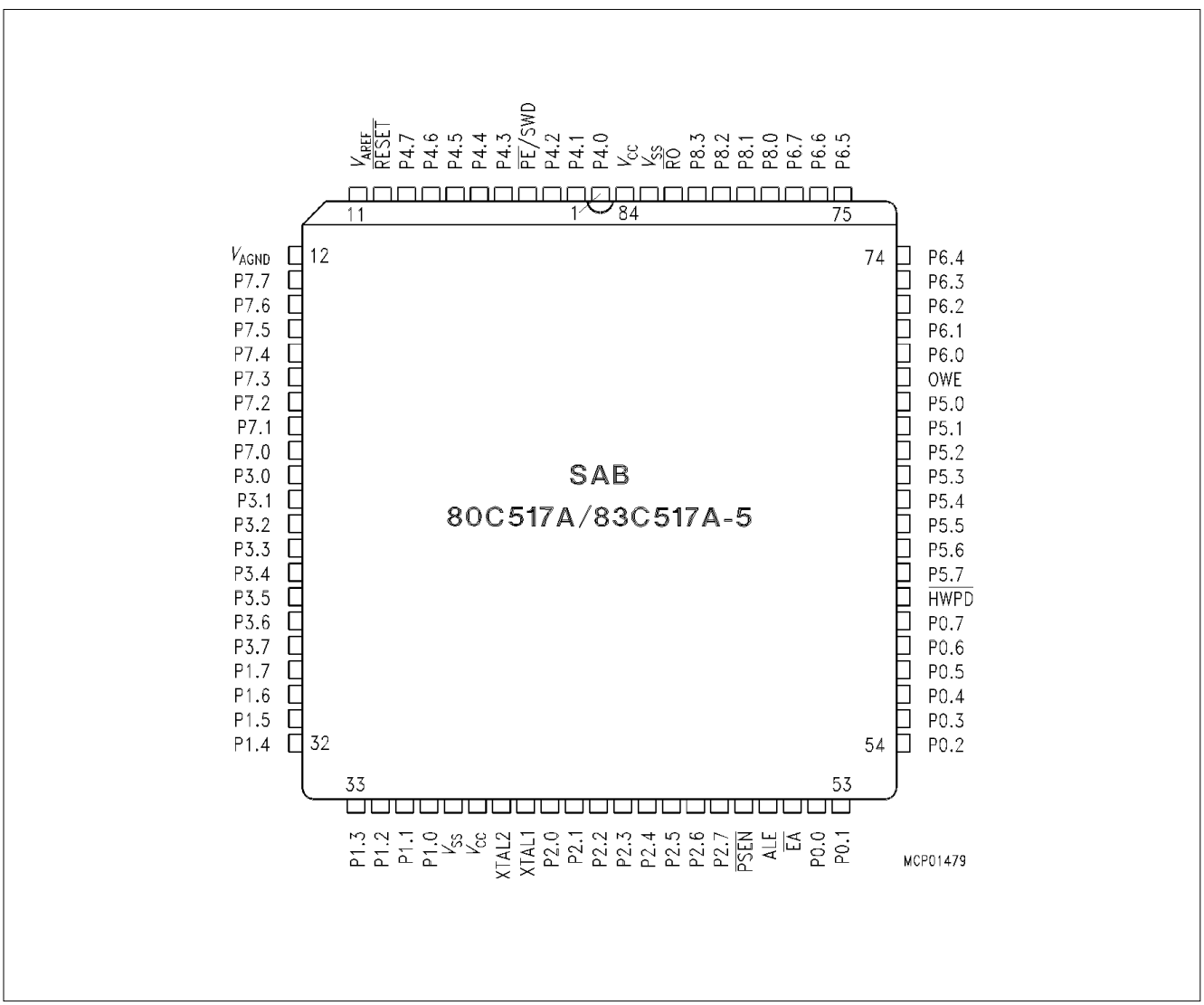
Type	Ordering code	Package	Description 8-bit CMOS microcontroller
SAB 80C517A-N18	Q67120-C583	P-LCC-84	for external memory,18 MHz
SAB 80C517A-M18	TBD	P-MRFP-100	
SAB 83C517A-5N18	Q67120-C582	P-LCC-84	with mask-programmable ROM, 18 MHz
SAB 80C517A-N18-T3	Q67120-C769	P-LCC-84	for external memory,18 MHz ext. temperature – 40 to 85 °C
SAB 83C517A-5N18-T3	Q67120-C771	P-LCC-84	with mask-programmable ROM, 18 MHz ext. temperature – 40 to 85 °C
SAB 83C517A-N18-T4	TBD	P-LCC-84	for external memory, 18 MHz ext. temperature -40 to +110°C
SAB 83C517A-5N18-T4	TBD	P-LCC-84	with mask-programmable ROM, 18 MHz ext. temperature -40 to +110°C



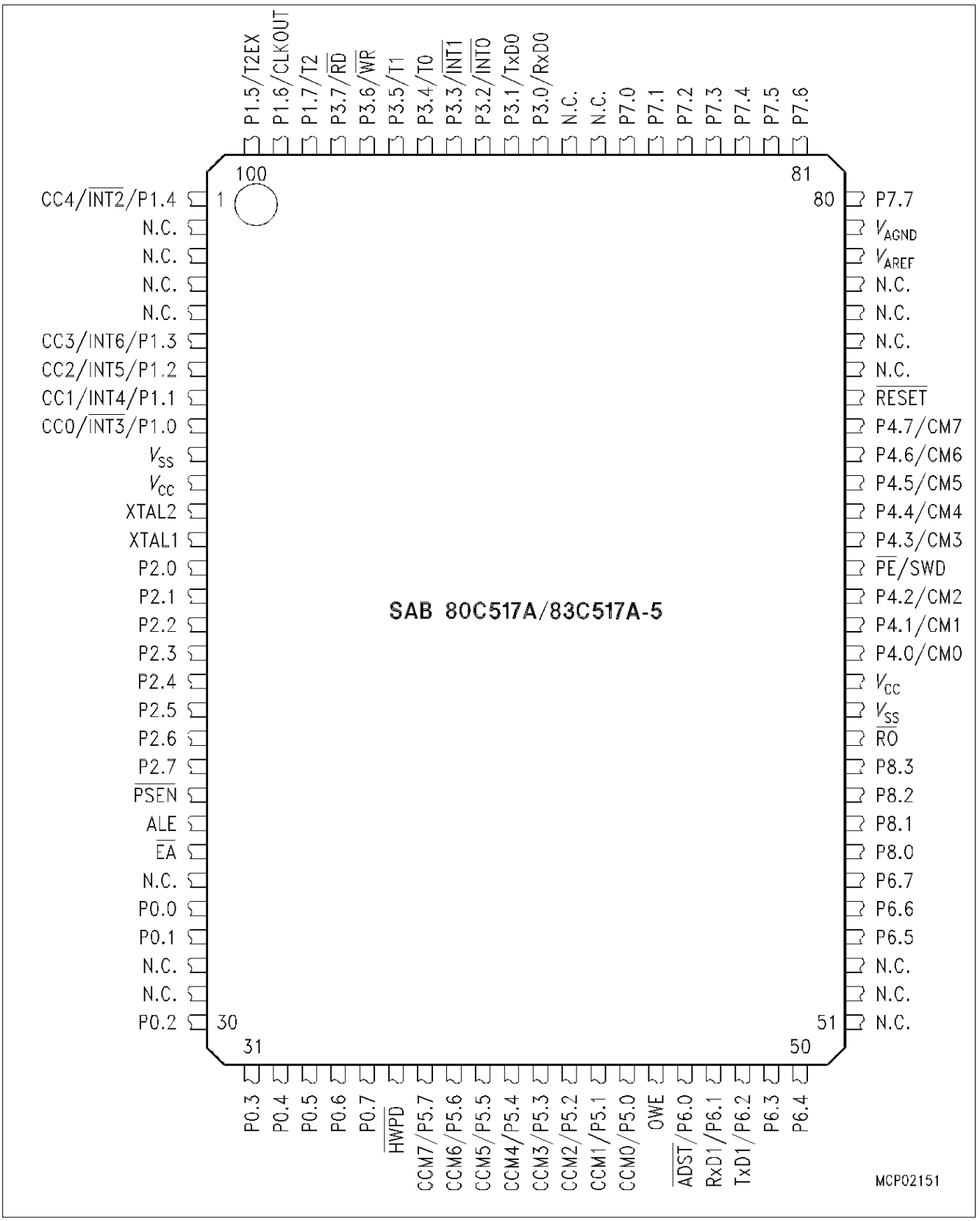
Logic Symbol

The pin functions of the SAB 80C517A are identical with those of the SAB 80C517/80C537 with one exception:

Typ	SAB 80C517A	SAB 80C517/80C537
P-LCC-84, Pin 60	$\overline{\text{HWPD}}$	N.C.
P-MQFP-100-2,Pin 36		



Pin Configuration
(P-LCC-84)



Pin Configuration
(P-MQFP-100-2)

Pin Definitions and Functions

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P4.0 – P4.7	1– 3, 5 – 9	64 - 66, 68 - 72	I/O	**Port 4** is a bidirectional I/O port with internal pull-up resistors. Port 4 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. This port also serves alternate compare functions. The secondary functions are assigned to the pins of port 4 as follows: – CM0 (P4.0): Compare Channel 0 – CM1 (P4.1): Compare Channel 1 – CM2 (P4.2): Compare Channel 2 – CM3 (P4.3): Compare Channel 3 – CM4 (P4.4): Compare Channel 4 – CM5 (P4.5): Compare Channel 5 – CM6 (P4.6): Compare Channel 6 – CM7 (P4.7): Compare Channel 7
$\overline{PE}$/SWD	4	67	I	**Power saving modes $\overline{enable}$ Start Watchdog Timer** A low level on this pin allows the software to enter the power down, idle and slow down mode. In case the low level is also seen during reset, the watchdog timer function is off on default. Use of the software controlled power saving modes is blocked, when this pin is held on high level. A high level during reset performs an automatic start of the watchdog timer immediately after reset. When left unconnected this pin is pulled high by a weak internal pull-up resistor.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
$\overline{\text{RESET}}$	10	73	I	$\overline{\text{RESET}}$ A low level on this pin for the duration of one machine cycle while the oscillator is running resets the SAB 80C517A. A small internal pull-up resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11	78		**Reference voltage** for the A/D converter.
V_{AGND}	12	79		**Reference ground** for the A/D converter.
P7.7 -P7.0	13 - 20	80 - 87	I	**Port 7** is an 8-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high/low voltages, and for the lower 8-bit of the multiplexed analog inputs of the A/D converter, simultaneously.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P3.0 - P3.7	21 - 28	90 - 97	I/O	**Port 3** is a bidirectional I/O port with internal pull-up resistors. Port 3 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current ($I_{IL,}$ in the DC characteristics) because of the internal pull-up resistors. Port 3 also contains the interrupt, timer, serial port 0 and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – R × D0 (P3.0): receiver data input (asynchronous) or data input/output (synchronous) of serial interface – T × D0 (P3.1): transmitter data output (asynchronous) or clock output (synchronous) of serial interface 0 – $\overline{INT0}$ (P3.2): $\overline{interrupt\ 0\ input}$/timer 0 gate control – $\overline{INT1}$ (P3.3): $\overline{interrupt\ 1\ input}$/timer 1 gate control – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{WR}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{RD}$ (P3.7): the read control signal enables the external data memory to port 0

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P1.7 - P1.0	29 - 36	98 - 100, 1, 6 - 9	I/O	**Port 1** is a bidirectional I/O port with internal pull-up resistors. Port 1 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. It is used for the low order address byte during program verification. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows: – $\overline{\text{INT3}}$/CC0 (P1.0): $\overline{\text{interrupt 3 input}}$/ compare 0 output /capture 0 input – INT4/CC1 (P1.1): interrupt 4 input / compare 1 output /capture 1 input – INT5/CC2 (P1.2): interrupt 5 input / compare 2 output /capture 2 input – INT6/CC3 (P1.3): interrupt 6 input / compare 3 output /capture 3 input – $\overline{\text{INT2}}$/CC4 (P1.4): $\overline{\text{interrupt 2 input}}$ / compare 4 output /capture 4 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
XTAL2	39	12	–	**XTAL2** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL1	40	13	–	**XTAL1** Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is devided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.
P2.0 - P2.7	41 - 48	14 - 21	I/O	**Port 2** is a bidirectional I/O port with internal pull-up resistors. Port 2 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as in-puts. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pull-up resistors when issuing1 s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
$\overline{\text{PSEN}}$	49	22	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periodes except during external data memory accesses. Remains high during internal program execution.
ALE	50	23	O	The **Address Latch Enable** output is used for latching the address into external memory during normal operation. It is activated every six oscillator periodes except during an external data memory access
$\overline{\text{EA}}$	51	24	I	**External Access Enable** When held at high level, instructions are fetched from the internal ROM (SAB 83C517A-5 only) when the PC is less than 8000H. When held at low level, the SAB 80C517A fetches all instructions from external program memory. For the SAB 80C517A this pin must be tied low
P0.0 - P0.7	52 - 59	26 - 27, 30 - 35	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1 s written to them float, and in that state can be used as high-impe-dance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-up resistors when issuing 1 s. Port 0 also out-puts the code bytes during program verification in the SAB 83C517A if ROM-Protection was not enabled. External pull-up resistors are required during program verification.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
$\overline{\text{HWPD}}$	60	36	I	**$\overline{\text{Hardware Power Down}}$** A low level on this pin for the duration of one machine cycle while the oscillator is running resets the SAB 80C517A. A low level for a longer period will force the part to Power Down Mode with the pins floating. (see table 7)
P5.7 - P5.0	61 - 68	37 - 44	I/O	**Port 5** is a bidirectional I/O port with internal pull-up resistors. Port 5 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. This port also serves the alternate function "Concurrent Compare" and "Set/Reset Compare". The secondary functions are assigned to the port 5 pins as follows: – CCM0 to CCM7 (P5.0 to P5.7): concurrent compare or Set/Reset
			I	
OWE	69	45	I/O	**Oscillator Watchdog Enable** A high level on this pin enables the oscillator watchdog. When left unconnected this pin is pulled high by a weak internal pull-up resistor. When held at low level the oscillator watchdog function is off.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P6.0 - P6.7	70 - 77	46 - 50, 54 - 56	I/O	**Port 6** is a bidirectional I/O port with internal pull-up resistors. Port 6 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 6 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 6 also contains the external A/D converter control pin and the transmit and receive pins for serial channel 1. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 6, as follows: – $\overline{\text{ADST}}$ (P6.0): external A/D converter start pin – R × D1 (P6.1): receiver data input of serial interface 1 – T × D1 (P6.2): transmitter data output of serial interface 1
P8.0 - P8.3	78 - 81	57 - 60	I	**Port 8** is a 4-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high/low voltages, and for the higher 4-bit of the multiplexed analog inputs of the A/D converter, simultaneously

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
$\overline{RO}$	82	61	O	**$\overline{Reset\ Output}$** This pin outputs the internally synchronized reset request signal. This signal may be generated by an external hardware reset, a watchdog timer reset or an oscillator watch-dog reset. The reset output is active low.
V_{SS}	37, 83	10, 62	–	**Circuit ground potential**
V_{CC}	38, 84	11, 63	–	**Supply Terminal** for all operating modes
N.C.	–	2 - 5, 25, 28 - 29, 51 - 53, 74 - 77, 88 - 89	–	Not connected

* I = Input
O = Output

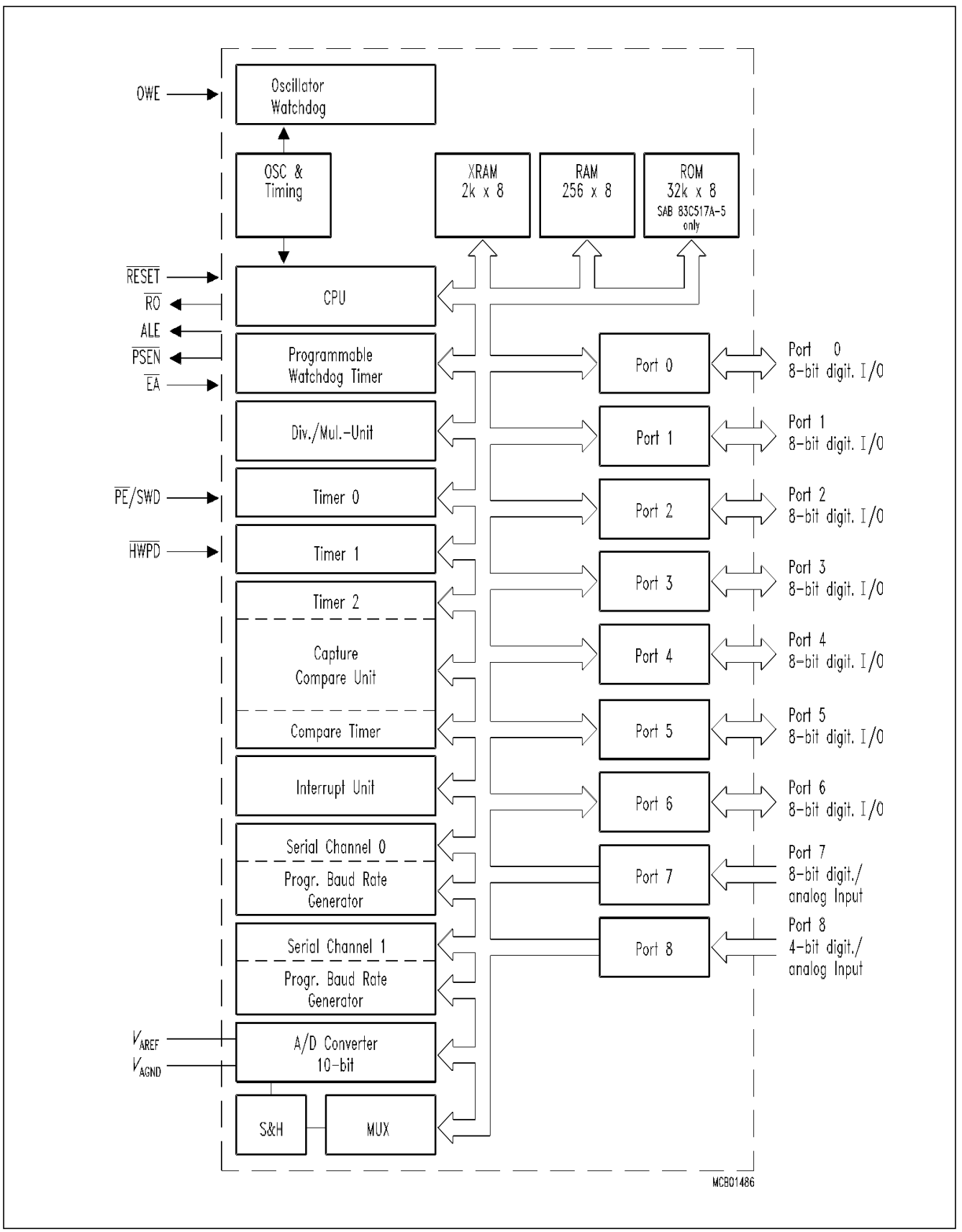


Figure 1
Block Diagram

Functional Description

The SAB 80C517A is based on 8051 architecture. It is a fully compatible member of the Siemens SAB 8051/80C51 microcontroller family being an significantly enhanced SAB 80C517. The SAB 80C517A is therefore compatible with code written for the SAB 80C517.

Having an 8-bit CPU with extensive facilities for bit-handling and binary BCD arithmetics the SAB 80C517A is optimized for control applications. With a 18 MHz crystal, 58 % of the instructions are executed in 666.67 ns.

Being designed to close the performance gap to the 16-bit microcontroller world, the SAB 80C517A's CPU is supported by a powerful 32-/16-bit arithmetic unit and a more flexible addressing of external memory by eight 16-bit datapointers.

Memory Organisation

According to the SAB 8051 architecture, the SAB 80C517A has separate address spaces for program and data memory. Figure 2 illustrates the mapping of address spaces.

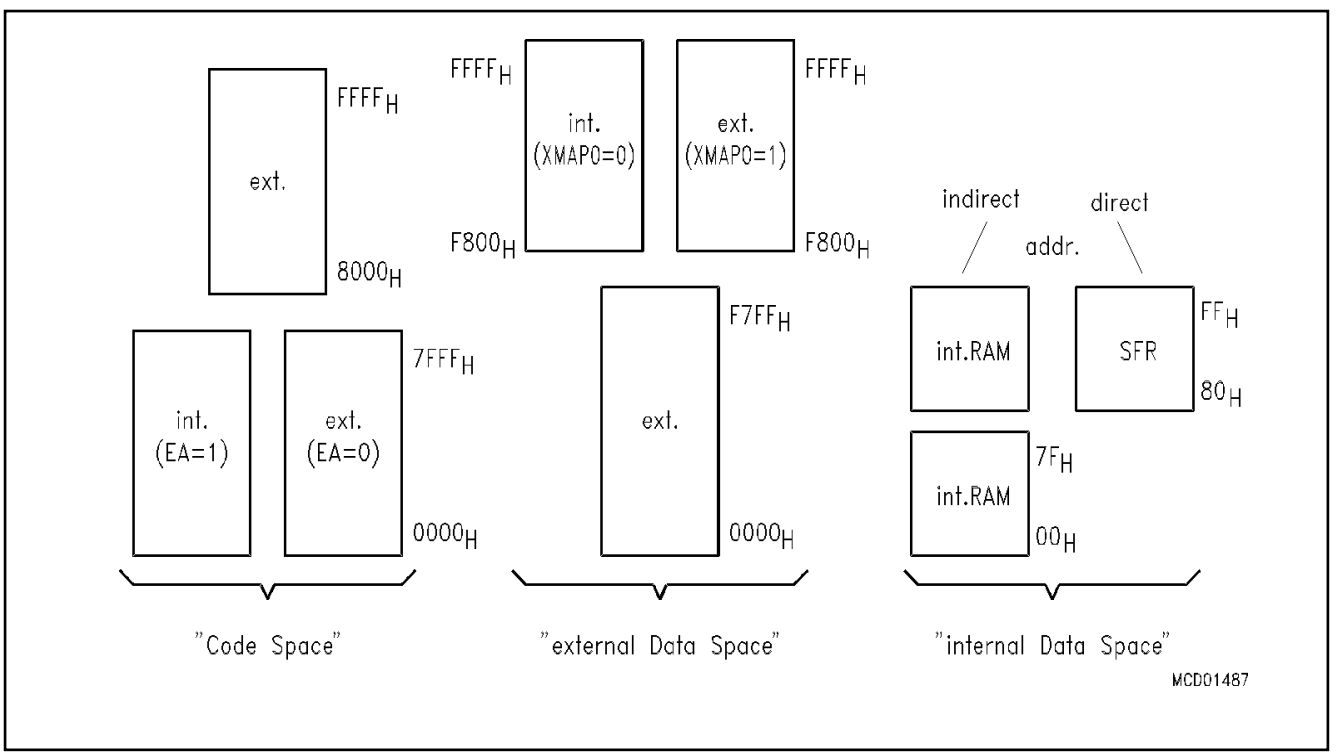


Figure 2
Memory Map

Program Memory ('Code Space')

The SAB 83C517A-5 has 32 Kbyte of on-chip ROM, while the SAB 80C517A has no internal ROM. The program memory can externally be expanded up to 64 Kbyte. Pin $\overline{EA}$ controls whether program fetches below address 8000H are done from internal or external memory.

As a new feature the SAB 83C517A-5 offers the possibility of protecting the internal ROM against unauthorized access. This protection is implemented in the ROM-Mask.Therefore, the decision ROM-Protection 'yes' or 'no' has to be made when delivering the ROM-Code. Once enabled, there is no way of disabling the ROM-Protection.

Effect: The access to internal ROM done by an externally fetched MOVC instruction is disabled. Nevertheless, an access from internal ROM to external ROM is possible.

To verify the read protected ROM-Code a special ROM-Verify-Mode is implemented. This mode also can be used to verify unprotected internal ROM.

ROM -Protection	**ROM-Verification Mode (see 'AC Characteristics')**	**Restrictions**
no	ROM-Verification Mode 1 (standard 8051 Verification Mode) ROM-Verification Mode 2	–
yes	ROM-Verification Mode 2	– standard 8051 Verification Mode is disabled – externally applied MOVC accessing internal ROM is disabled

Data Memory ('Code Space')

The data memory space consists of an internal and an external memory space. The SAB 80C517A contains another 2 Kbyte on On-Chip RAM above the 256-bytes internal RAM of the base type SAB 80C517. This RAM is called XRAM in this document.

External Data Memory

Up to 64 Kbyte external data memory can be addressed by instructions that use 8-bit or 16-bit indirect addressing. For 8-bit addressing MOVX instructions in combination with registers R0 and R1 can be used. A 16-bit external memory addressing is supported by eight 16-bit datapointers. Registers XPAGE and SYSCON are controlling whether data fetches at addresses $F800_H$ to $FFFF_H$ are done from internal XRAM or from external data memory.

Internal Data Memory

The internal data memory is divided into four physically distinct blocks:

– the lower 128 bytes of RAM including four banks containing eight registers each

– the upper 128 byte of RAM

– the 128 byte special function register area.

– a 2 K $\times$ 8 area which is accessed like external RAM (MOVX-instructions), implemented on chip at the address range from $F800_H$ to $FFFF_H$. Special Function Register SYSCON controls whether data is read or written to XRAM or external RAM.

A mapping of the internal data memory is also shown in figure 2. The overlapping address spaces are accessed by different addressing modes (see User's Manual SAB 80C517). The stack can be located anywhere in the internal data memory.

Architecture for the XRAM

The contents of the XRAM is not affected by a reset or HW Power Down. After power-up the contents is undefined, while it remains unchanged during and after a reset or HW Power Down if the power supply is not turned off.

The additional On-Chip RAM is logically located in the "external data memory" range at the upper end of the 64 Kbyte address range ($F800_H$-$FFFF_H$). It is possible to enable and disable (only by reset) the XRAM. If it is disabled the device shows the same behaviour as the parts without XRAM, i.e. all MOVX accesses use the external bus to physically external data memory.

Accesses to XRAM

Because the XRAM is used in the same way as external data memory the same instruction types must be used for accessing the XRAM.

Note: *If a reset occurs during a write operation to XRAM, the effect on XRAM depends on the cycle which the reset is detected at (MOVX is a 2-cycle instruction):*

Reset detection at cycle 1: *The new value will not be written to XRAM. The old value is not affected.*

Reset detection at cycle 2: *The old value in XRAM is overwritten by the new value.*

Accesses to XRAM using the DPTR

There are a Read and a Write instruction from and to XRAM which use one of the 16-bit DPTR for indirect addressing. The instructions are:

MOVX A, @DPTR (Read)

MOVX @DPTR, A (Write)

Normally the use of these instructions would use a physically external memory. However, in the SAB 80C517A the XRAM is accessed if it is enabled and if the DPTR points to the XRAM address space (DPTR $\geqq$ $F800_H$).

Accesses to XRAM using the Registers R0/R1

The 8051 architecture provides also instructions for accesses to external data memory range which use only an 8-bit address (indirect addressing with registers R0 or R1). The instructions are:

MOVX A, @Ri (Read)

MOVX @Ri, A (Write)

In application systems, either a real 8-bit bus (with 8-bit address) is used or Port 2 serves as page register which selects pages of 256-byte. However, the distinction, whether Port 2 is used as general purpose I/O or as "page address" is made by the external system design. From the device’s point of view it cannot be decided whether the Port 2 data is used externally as address or as I/O data!

Hence, a special page register is implemented into the SAB 80C517A to provide the possibility of accessing the XRAM also with the MOVX @Ri instructions, i.e. XPAGE serves the same function for the XRAM as Port 2 for external data memory.

Special Function Register XPAGE

Addr. 91_H									XPAGE

The reset value of XPAGE is 00_H.

XPAGE can be set and read by software.

The register XPAGE provides the upper address byte for accesses to XRAM with MOVX @Ri instructions. If the address formed from XPAGE and Ri is less than the XRAM address range, then an external access is performed. For the SAB 80C517A the contents of XPAGE must be greater or equal than F8H in order to use the XRAM. Of course, the XRAM must be enabled if it shall be used with MOVX @Ri instructions.

Thus, the register XPAGE is used for addressing of the XRAM; additionally its contents are used for generating the internal XRAM select. If the contents of XPAGE is less than the XRAM address range then an external bus access is performed where the upper address byte is provided by P2 and not by XPAGE!

Therefore, the software has to distinguish two cases, if the MOVX @Ri instructions with paging shall be used:

a) Access to XRAM: The upper address byte must be written to XPAGE or P2; both writes selects the XRAM address range.

b) Access to external memory: The upper address byte must be written to P2; XPAGE will be loaded with the same address in order to deselect the XRAM.

Control of XRAM in the SAB 80C517A

There are two control bits in register SYSCON which control the use and the bus operation during accesses to the additional On-Chip RAM (XRAM).

Special Function Register SYSCON

Addr. $0B1_H$	—	—	—	—	—	—	XMAP1	XMAP0	SYSCON

Bit	Function
XMAP0	Global enable/disable bit for XRAM memory. XMAP0 = 0: The access to XRAM (= On-Chip XDATA memory) is enabled. XMAP0 = 1: The access to XRAM is disabled. All MOVX accesses are performed by the external bus (reset state).
XMAP1	Control bit for $\overline{RD}$/$\overline{WR}$ signals during accesses to XRAM; this bit has no effect if XRAM is disabled (XMAP0 = 1) or if addresses exceeding the XRAM address range are used for MOVX accesses. XMAP1 = 0: The signals $\overline{RD}$ and $\overline{WR}$ are not activated during accesses to XRAM. XMAP1 = 1: The signals $\overline{RD}$ and $\overline{WR}$ are activated during accesses to XRAM.

Reset value of SYSCON is xxxx xx01B.

The control bit XMAP0 is a global enable/disable bit for the additional On-Chip RAM (XRAM). If this bit is set, the XRAM is disabled, all MOVX accesses use external memory via the external bus. In this case the SAB 80C517A does not use the additional On-Chip RAM and is compatible with the types without XRAM.

XMAP0 is hardware protected by an unsymmetric latch. An unintentional disabling of XRAM could be dangerous since indeterminate values would be read from external bus. To avoid this the XMAP-bit is forced to '1' only by reset. Additionally, during reset an internal capacitor is loaded. So after reset state XRAM is disabled. Because of the load time of the capacitor XMAP0-bit once written to '0' (that is, discharging capacitor) cannot be set to '1' again by software. On the other hand any distortion (software hang up, noise, ...) is not able to load this capacitor, too. That is, the stable status is XRAM enabled. The only way to disable XRAM after it was enabled is a reset.

The clear instruction for XMAP0 should be integrated in the program initialization routine before XRAM is used. In extremely noisy systems the user may have redundant clear instructions.

The control bit XMAP1 is relevant only if the XRAM is accessed. In this case the externa $\overline{RD}$ and $\overline{WR}$ signals at P3.6 and P3.7 are not activated during the access, if XMAP1 is cleared. For debug purposes it might be useful to have these signals and the addresses at Ports 0.2 available. This is performed if XMAP1 is set.

The behaviour of Port 0 and P2 during a MOVX access depends on the control bits in register SYSCON and on the state of pin $\overline{EA}$. The table 1 lists the various operating conditions. It shows the following characteristics:

a) Use of P0 and P2 pins during the MOVX access.

   Bus: The pins work as external address/data bus. If (internal) XRAM is accessed, the data written to the XRAM can be seen on the bus in debug mode.

   I/0: The pins work as Input/Output lines under control of their latch.

b) Activation of the $\overline{RD}$ and $\overline{WR}$ pin during the access.

c) Use of internal or external XDATA memory.

The shaded areas describe the standard operation as each 80C51 device without on-chip XRAM behaves.

Table 1:
Behaviour of P0/P2 and $\overline{RD}/\overline{WR}$ during MOVX accesses

		= 0				
		XMAP1, XMAP0				XMA
		00	10	X1	00	
MOVX @DPTR	DPTR < XRAM address range	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/ b) $\overline{RD}$ c) ext. use
	DPTR ≥ XRAM address range	a) P0/P2→BUS ($\overline{WR}$ -Data only) b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→BUS ($\overline{WR}$ -Data only) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→I/0 b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/ ($\overline{WR}$ -D b) $\overline{RD}$ c) XR
MOVX @Ri	XPAGE < XRAM addr. page range	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0 P2→I b) $\overline{RD}$ c) ext. use
	XPAGE ≥ XRAM addr. page range	a) P0/P2→BUS ($\overline{WR}$ -Data only) P2→I/0 b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→BUS ($\overline{WR}$ -Data only) P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0→Bus P2→I/0 b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2→I/0 b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0 ($\overline{WR}$ -D P2→I b) $\overline{RD}$ c) XR

modes compatible to 8051 - family

Multiple Datapointers

As a functional enhancement to standard 8051 controllers, the SAB 80C517A contains eight 16-bit datapointers. The instruction set uses just one of these datapointers at a time. The selection of the actual datapointer is done in special function register DPSEL (data pointer select, addr. 92_H). Figure 3 illustrates the addressing mechanism.

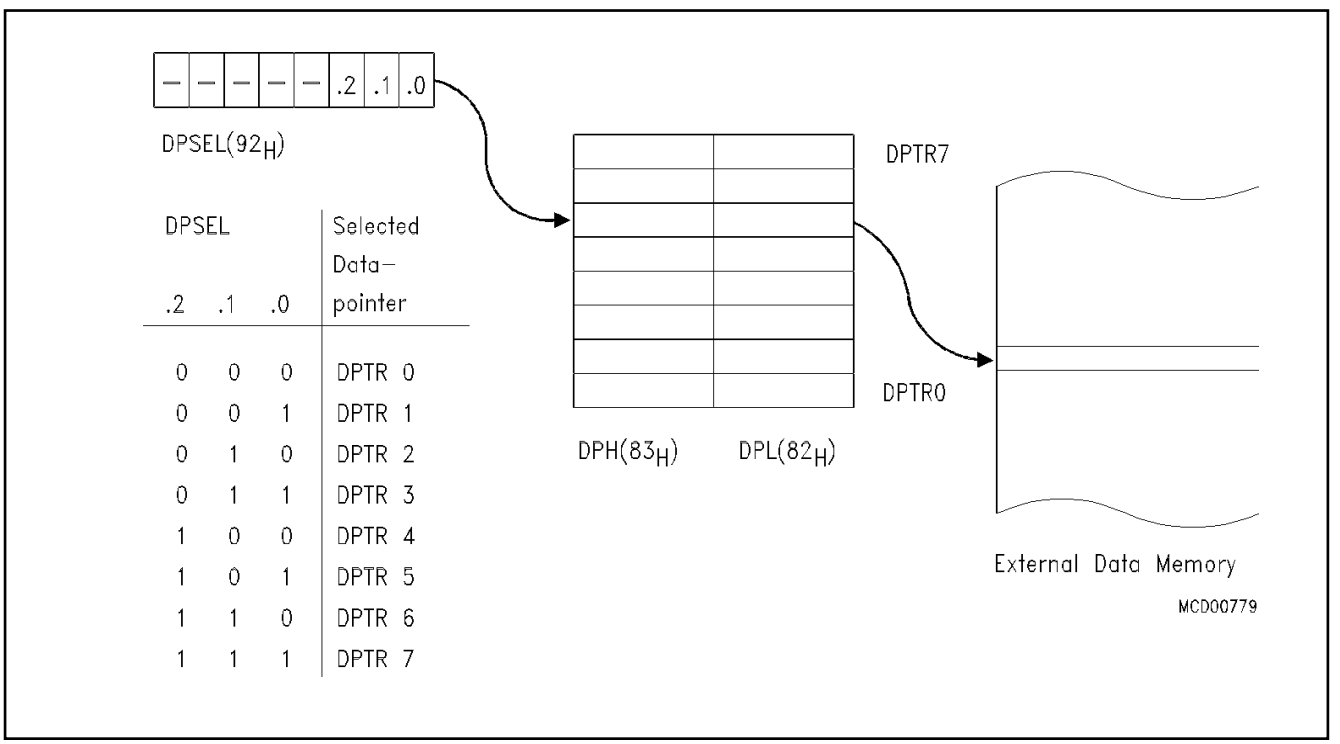


Figure 3
Addressing of External Data Memory

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area. The 81 special function registers include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripherals. There are also 128 directly addressable bits within the SFR area. All special function registers are listed in table 1 and table 2.

In table 1 they are organized in numeric order of their addresses. In table 2 they are organized in groups which refer to the functional blocks of the SAB 80C517A.

Table 2
Special Function Register

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80_H	**P0** [1]	**FF_H**	**98_H**	**S0CON** [1]	**00_H**
81_H	SP	07_H	99_H	S0BUF	XX_H
82_H	DPL	00_H	$9A_H$	IEN2	$XX00\ 00X0_B$
83_H	DPH	00_H	$9B_H$	S1CON	$0X00\ 0000_B$
84_H	(WDTL) [3]	(00_H)	$9C_H$	S1BUF	XX_H
85_H	(WDTH) [3]	(00_H)	$9D_H$	S1RELL	00_H
86_H	WDTREL	00_H	$9E_H$	reserved	XX_H
87_H	PCON	00_H	$9F_H$	reserved	XX_H
88_H	**TCON** [1]	**00_H**	**$A0_H$**	**P2** [1]	**FF_H**
89_H	TMOD	00_H	$A1_H$	COMSETL	00_H
$8A_H$	TL0	00_H	$A2_H$	COMSETH	00_H
$8B_H$	TL1	00_H	$A3_H$	COMCLRL	00_H
$8C_H$	TH0	00_H	$A4_H$	COMCLRH	00_H
$8D_H$	TH1	00_H	$A5_H$	SETMSK	00_H
$8E_H$	reserved	XX_H [2]	$A6_H$	CLRMSK	00_H
$8F_H$	reserved	XX_H [2]	$A7_H$	reserved	XX_H [2]
90_H	**P1** [1]	**FF_H**	**$A8_H$**	**IEN0** [1]	**00_H**
91_H	XPAGE	00_H	$A9_H$	IP0	00_H
92_H	DPSEL	$XXXXX000_B$	AA_H	S0RELL	$D9_H$
93_H	reserved	XX_H [2]	AB_H	reserved	XX_H [2]
94_H	reserved	XX_H [2]	AC_H	reserved	XX_H [2]
95_H	reserved	XX_H [2]	AD_H	reserved	XX_H [2]
96_H	reserved	XX_H [2]	AE_H	reserved	XX_H [2]
97_H	reserved	XX_H [2]	AF_H	reserved	XX_H [2]

[1] Bit-addressable special function registers
[2] X means that the value is indeterminate and the location is reserved
[3] ( )... SFRs not user accessable

Table 2
Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
$B0_H$	**P3** [1]	**FF_H**	**$D0_H$**	**PSW** [1]	**00_H**
$B1_H$	SYSCON	$XXXX\ XX01_B$	$D1_H$	IRCON1	00_H
$B2_H$	reserved	XX_H [2]	$D2_H$	CML0	00_H
$B3_H$	reserved	XX_H [2]	$D3_H$	CMH0	00_H
$B4_H$	reserved	XX_H [2]	$D4_H$	CML1	00_H
$B5_H$	reserved	XX_H [2]	$D5_H$	CMH1	00_H
$B6_H$	reserved	XX_H [2]	$D6_H$	CML2	00_H
$B7_H$	reserved	XX_H [2]	$D7_H$	CMH2	00_H
$B8_H$	**IEN1** [1]	**00_H**	**$D8_H$**	**ADCON0** [1]	**00_H**
$B9_H$	IP1	$XX00\ 0000_B$	$D9_H$	ADDATH	00_H
BA_H	S0RELH	$XXXX\ XX11_B$	DA_H	ADDATL	00_H
BB_H	S1RELH	$XXXX\ XX11_B$	DB_H	P7	XX_H
BC_H	reserved	XX_H	DC_H	ADCON1	$XXXX0000_B$
BD_H	reserved	XX_H	DD_H	P8	XX_H
BS_H	reserved	XX_H	DE_H	CTRELL	00_H
BF_H	reserved	XX_H	DF_H	CTRELH	00_H
$C0_H$	**IRCON0** [1]	**00_H**	**$E0_H$**	**ACC** [1]	**00_H**
$C1_H$	CCEN	00_H	$E1_H$	CTCON	$0X00\ 0000_B$
$C2_H$	CCL1	00_H	$E2_H$	CML3	XX_H
$C3_H$	CCH1	00H	$E3_H$	CMH3	00_H
$C4_H$	CCL2	00_H	$E4_H$	CML4	00_H
$C5_H$	CCH2	00_H	$E5_H$	CMH4	00_H
$C6_H$	CCL3	00_H	$E6_H$	CML5	00_H
$C7_H$	CCH3	00_H	$E7_H$	CMH5	00_H
$C8_H$	**T2CON** [1]	**00_H**	**$E8_H$**	**P4** [1]	**FF_H**
$C9_H$	CC4EN	00_H	$E9_H$	MD0	XX_H
CA_H	CRCL	00_H	EA_H	MD1	XX_H
CB_H	CRCH	00_H	EB_H	MD2	XX_H
CC_H	TL2	00_H	EC_H	MD3	XX_H
CD_H	TH2	00_H	ED_H	MD4	XX_H
CE_H	CCL4	00_H	EE_H	MD5	XX_H
CF_H	CCH4	00_H	EF_H	ARCON	$0XXX\ XXXX_B$

[1] Bit-addressable special function registers
[2] X means that the value is indeterminate and the location is reserved
[3] ( )... SFRs not user accessable

Table 2
Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
$F0_H$	**B** [1]	**00_H**	**$F8_H$**	**P5** [1]	**FF_H**
$F1_H$	reserved	XX_H	$F9_H$	reserved	XX_H
$F2_H$	CML6	00_H	FA_H	P6	FF_H
$F3_H$	CMH6	00_H	FB_H	reserved	XX_H
$F4_H$	CML7	00_H	FC_H	reserved	XX_H
$F5_H$	CMH7	00_H	FD_H	(IS0)	XX_H
$F6_H$	CMEN	00_H	FE_H	(IS1)	XX_H
$F7_H$	CMSEL	00_H	FF_H	reserved	XX_H

[1] Bit-addressable special function registers
[2] X means that the value is indeterminate and the location is reserved
[3] ( )... SFRs not user accessable

Table 3
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$** [1]	00_H
	B	B-Register	**$F0_H$** [1]	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	DPSEL	Data Pointer Select Register	92_H	$XXXX\ X000_B$ [3]
	PSW	Program Status Word Register	**$D0_H$** [1]	00_H
	SP	Stack Pointer	81_H	07_H
A/D-Converter	ADCON0	A/D Converter Control Register 0	**$D8_H$** [1]	00_H
	ADCON1	A/D Converter Control Register 1	DC_H	00_H
	ADDATH	A/D Converter Data Reg. High Byte	$D9_H$	00_H
	ADDATL	A/D Converter Data Reg. Low Byte	DA_H	00_H
Interrupt System	IEN0	Interrupt Enable Register 0	**$A8_H$** [1]	**00_H**
	CTCON [2]	Com. Timer Control Register	$E1_H$	$0XXX.0000_B$
	IEN1	Interrupt Enable Register 1	**$B8_H$** [1]	**00_H**
	IEN2	Interrupt Enable Register 2	$9A_H$	$XXXX.00X0_B$ [3]
	IP0	Interrupt Priority Register 0	$A9_H$	00_H
	IP1	Interrupt Priority Register 1	$B9_H$	$XX00\ 0000_B$
	IRCON0	Interrupt Request Control Register	**$C0_H$** [1]	00_H
	IRCON1	Interrupt Request Control Register	$D1_H$	00_H
	TCON [2]	Timer Control Register	**88_H** [1]	00_H
	TCON [2]	Timer 2 Control Register	**$C8_H$**	00_H
MUL/DIV Unit	ARCON	Arithmetic Control Register	EF_H	$0XXXX\ XXXX_B$
	MD0	Multiplication/Division Register 0	$E9_H$	XX_H
	MD1	Multiplication/Division Register 1	EA_H	XX_H
	MD2	Multiplication/Division Register 2	EB_H	XX_H
	MD3	Multiplication/Division Register 3	EC_H	XX_H
	MD4	Multiplication/Division Register 4	ED_H	XX_H
	MD5	Multiplication/Division Register 5	EE_H	XX_H

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Compare/ Capture- Unit (CCU) Timer 2	CCEN	Comp./Capture Enable Reg.	$C1_H$	00_H
	CC4EN	Comp./Capture Enable 4 Reg.	$C9_H$	00_H
	CCH1	Comp./Capture Reg. 1, High Byte	$C3_H$	00_H
	CCH2	Comp./Capture Reg. 2, High Byte	$C5_H$	00_H
	CCH3	Comp./Capture Reg. 3, High Byte	$C7_H$	00_H
	CCH4	Comp./Capture Reg. 4, High Byte	CF_H	00_H
	CCL1	Comp./Capture Reg. 1, Low Byte	$C2_H$	00_H
	CCL2	Comp./Capture Reg. 2, Low Byte	$C4_H$	00_H
	CCL3	Comp./Capture Reg. 3, Low Byte	$C6_H$	00_H
	CCL4	Comp./Capture Reg. 4, Low Byte	CE_H	00_H
	CMEN	Compare Enable Register	$F6_H$	00_H
	CMH0	Compare Register 0, High Byte	$D3_H$	00_H
	CMH1	Compare Register 1, High Byte	$D5_H$	00_H
	CMH2	Compare Register 2, High Byte	$D7_H$	00_H
	CMH3	Compare Register 3, High Byte	$E3_H$	00_H
	CMH4	Compare Register 4, High Byte	$E5_H$	00_H
	CMH5	Compare Register 5, High Byte	$E7_H$	00_H
	CMH6	Compare Register 6, High Byte	$F3_H$	00_H
	CMH7	Compare Register 7, High Byte	$F5_H$	00_H
	CML0	Compare Register 0, Low Byte	$D2_H$	00_H
	CML1	Compare Register 1, Low Byte	$D4_H$	00_H
	CML2	Compare Register 2, Low Byte	$D6_H$	00_H
	CML3	Compare Register 3, Low Byte	$E2_H$	00_H
	CML4	Compare Register 4, Low Byte	$E4_H$	00_H
	CML5	Compare Register 5, Low Byte	$E6_H$	00_H
	CML6	Compare Register 6, Low Byte	$F2_H$	00_H
	CML7	Compare Register 7, Low Byte	$F4_H$	00_H
	CMSEL	Compare Input Select	$F7_H$	00_H
	CRCH	Com./Rel./Capt. Reg. High Byte	CB_H	00_H
	CRCL	Com./Rel./Capt. Reg. Low Byte	CA_H	00_H
	COMSETL	Compare Register, Low Byte	$A1_H$	00_H
	COMSETH	Compare Register, High Byte	$A2_H$	00_H
	COMCLRL	Compare Register, Low Byte	$A3_H$	00_H
	COMCLRH	Compare Register, High Byte	$A4_H$	00_H
	SETMSK	Mask Register, concerning COMSET	$A5_H$	00_H

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Compare/ Capture- Unit (CCU), (cont'd)	CLRMSK	Mask Register, concerning COMCLR	$A6_H$	00_H
	CTCON	Com. Timer Control Reg.	$E1_H$	$0X00\ 0000_B$ [3]
	CTRELH	Com. Timer Rel. Reg., High Byte	DF_H	00_H
	CTRELL	Com. Timer Rel. Reg., Low Byte	DE_H	00_H
	TH2	Timer 2, High Byte	CD_H	00_H
	TL2	Timer 2, Low Byte	CC_H	00_H
	T2CON	Timer 2 Control Register	**$C8_H$** [1]	00_H
Ports	P0	Port 0	**80_H** [1]	FF_H
	P1	Port 1	**90_H** [1]	FF_H
	P2	Port 2	**$A0_H$** [1]	FF_H
	P3	Port 3	**$B0_H$** [1]	FF_H
	P4	Port 4	**$E8_H$** [1]	FF_H
	P5	Port 5	**$F8_H$** [1]	FF_H
	P6	Port 6,	FA_H	FF_H
	P7	Port 7, Analog/Digital Input	DB_H	
	P8	Port 8, Analog/Digital Input, 4-bit	DD_H	
Pow.Sav. Modes	PCON	Power Control Register	87_H	00_H
Serial Channels	**ADCON0** [2]	**A/D Converter Control Reg.**	**$D8_H$** [1]	**00_H**
	PCON [2]	Power Control Register	87_H	00_H
	S0BUF	Serial Channel 0 Buffer Reg.	99_H	XX_H [3]
	S0CON	**Serial Channel 0 Control Reg**.	**98_H** [1]	**00_H**
	S0RELL	Serial Channel 0, Reload Reg., low byte	$B2_H$	$0D9_H$
	S0RELH	Serial Channel 0, Reload Reg., high byte	BA_H	$XXXX.XX11_B$ [3]
	S1BUF	Serial Channel 1 Buffer Reg.,	$9C_H$	$0XX_H$ [3]
	S1CON	Serial Channel 1 Control Reg.	$9B_H$	$0X00.0000_B$ [3]
	S1REL	Serial Channel 1 Reload Reg., low byte	$9D_H$	00_H
	S1RELH	Serial Channel 1 Reload Reg., high byte	BB_H	$XXXX.XX11_B$ [3]

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Timer 0/ Timer 1	TCON	Timer Control Register	**88_H** [1]	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Watchdog	IEN0 [2]	Interrupt Enable Register 0	**$A8_H$** [1]	00_H
	IEN1 [2]	Interrupt Enable Register 1	**$B8_H$** [1]	00_H
	IP0 [2]	Interrupt Priority Register 0	$A9_H$	00_H
	IP1 [2]	Interrupt Priority Register 1	$B9_H$	$XX00\ 0000_B$ [3]
	WDTREL	Watchdog Timer Reload Reg.	86_H	00_H

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

A/D Converter

In the SAB 80C517A a new high performance / high-speed 12-channel 10-bit A/D-Converter is implemented. Its successive approximation technique provides 7 µs con-version time (f_{OSC}= 16 MHz). The conversion principle is upward compatible to the one used in the SAB 80C517. The main functional blocks are shown in figure 4.

The comparator is a fully differential comparator for a high power supply rejection ratio and very low offset voltages. The capacitor network is binary weighted providing genuine 10-bit resolution.

The table below shows the sample time T_S and the conversion time T_C, which are dependend on f_{OSC} and a new prescaler (see also Bit ADCL in SFR ADCON 1).

f_{OSC} [MHz]	Prescaler	f_{ADC} [MHz]	Sample Time T_S [µs]	Conversion Time (incl. sample time) T_C [µs]
12	÷ 8	1.5	2.67	9.33
	÷ 16	0.75	5.33	18.66
16	÷ 8	2.0	2.0	7.0
	÷ 16	1.0	4.0	14.0
18	÷ 8	–	–	–
	÷ 16	1.125	3.55	12.4

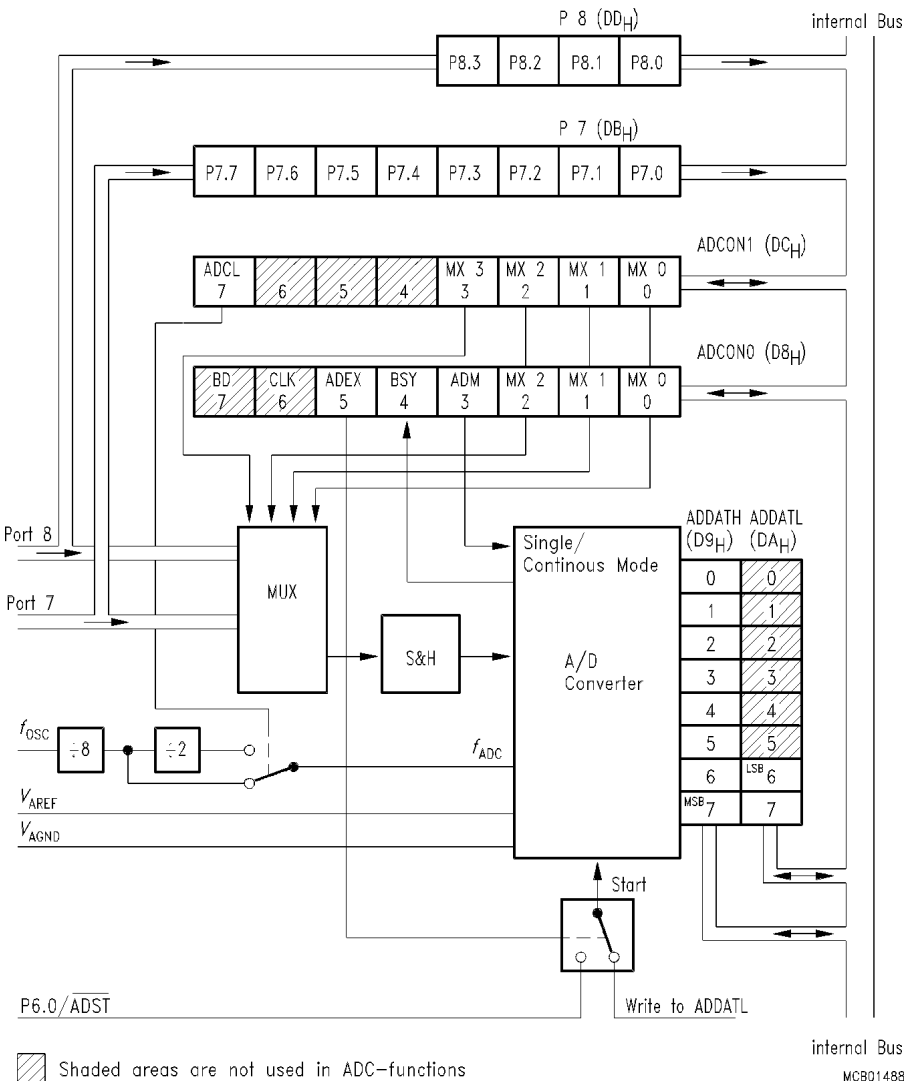


Figure 4
Block Diagram A/D Converter

Compare/Capture Unit (CCU)

The compare/capture unit is a complex timer/register array for applications that require high speed I/O pulse width modulation and more timer/counter capabilities.
The CCU contains

- one 16-bit timer/counter **(timer2)** with 2-bit prescaler, reload capability and a max. clock frequency of $f_{OSC/12}$ (1 MHz with a 12 MHz crystal).
- one 16-bit timer **(compare timer)** with 8-bit prescaler, reload capability and a max. clock frequency of $f_{OSC/2}$ (6 MHz with a 12 MHz crystal).
- fifteen 16-bit compare registers.
- five of which can be used as 16-bit capture registers.
- up to 21 output lines controlled by the CCU.
- nine interrupts which can be generated by CCU-events.

Figure 5 shows a block diagram of the CCU. Eight compare registers (CM0 to CM7) can individually be assigned to either timer 2 or the compare timer. Diagrams of the two timers are shown in figures 6 and 7. The four compare/capture registers, the compare/reload/capture register and the comset/comclr register are always connected to timer 2. Depending on the register type and the assigned timer three different compare modes can be selected.
Table 3 illustrates possible combinations and the corresponding output lines.

Table 4
CCU Compare Configuration

Assigned Timer	Compare Register	Compare Output	Possible Modes
Timer 2	CRCH/CRCL	P1.0/$\overline{\text{INT3}}$/CC0	Comp. mode 0, 1 + Reload
	CC1H/CC1L	P1.1/INT4/CC1	Comp. mode 0, 1
	CC2H/CC2L	P1.2/INT5/CC2	Comp. mode 0, 1
	CC3H/CC3L	P1.3/INT6/CC3	Comp. mode 0, 1
	CC4H/CC4L	P1.4/$\overline{\text{INT2}}$/CC4	Comp. mode 0, 1
	CC4H/CC4L	P5.0/CCM0	Comp. mode 1
	:	:	:
	CC4H/CC4L	P5.7/CCM7	Comp. mode 1
	COMSETL/COMSETH	P5.0/CCM0	Comp. mode 2
		:	:
		P5.7/CCM7	Comp. mode 2
	COMCLRL/	P5.0/CCM0	Comp. mode 2
	COMCLRH	:	:
		P5.7/CCM7	Comp. mode 2
		P4.0/CM0	Comp. mode 1
	CM0H/CM0L	:	:
	:	P4.7/CM7	Comp. mode 1
	CM7H/CM7L		
Compare timer	CM0H/CM0L	P4.0/CM0	Comp. mode 0 (with shadow latches)
	:	:	:
	CM7H/CM7L	P4.7/CM7	Comp. mode 0 (with shadow latches)

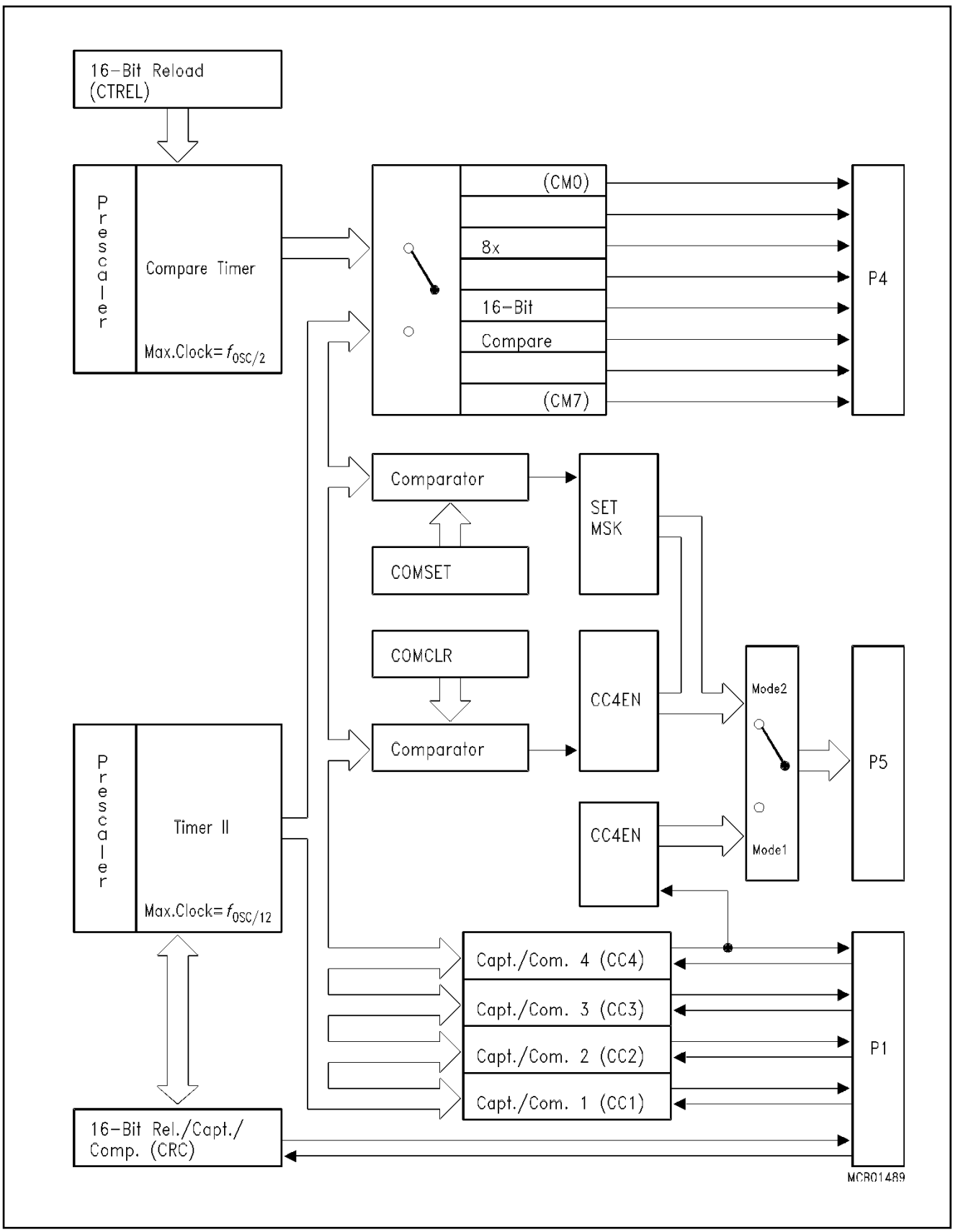


Figure 5
Block Diagram of the Compare/Capture Unit

Compare

In compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 register or the compare timer register. If the count value in the timer registers matches one of the stored value, an appropriate output signal is generated at the corresponding pin(s) and an interrupt is requested. Three compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It returns to low level at timer overflow.

Mode 1: The transition of the output signal can be determined by software. A timer overflow signal does not affect the compare-output.

Mode 2: In compare mode 2 the concurrent compare output pins on Port 5 are used as follows (see figure 9)

- When a compare match occurs with register COMSET, a high level appears at the pins of port 5 whose corresponding bits in the mask register SETMSK (address $0A5_H$) are set.
- When a compare match occurs in register COMCLR, a low level appears at the pins of port 5 whose corresponding bits in the mask register CLRMSK (address $0A6_H$) are set.

  Additionally the Port 5 pins used for compare mode 2 may also be directly written to by write instructions to SFR P5. Of course, the pins can also be read under program control.

Compare registers CM0 to CM7 use additional compare latches when operated in mode 0. Figure 8 shows the function of these latches. The latches are implemented to prevent from loss of compare matches which may occur when loading of the compare values is not correlated with the timer count. The compare latches are automatically loaded from the compare registers at every timer overflow.

Capture

This feature permits saving of the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to 'freeze' the current 16-bit value of timer 2 registers into a dedicated capture register.

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

Reload of Timer 2

A 16-bit reload can be performed with the 16-bit CRC register, which is a concatenation of the 8-bit registers CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

Timer/Counters 0 and 1

These timer/counters are fully compatible with timer/counter 0 or 1 of the SAB 8051 and can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer; timer/counter 1 in this mode holds its count.

External inputs $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

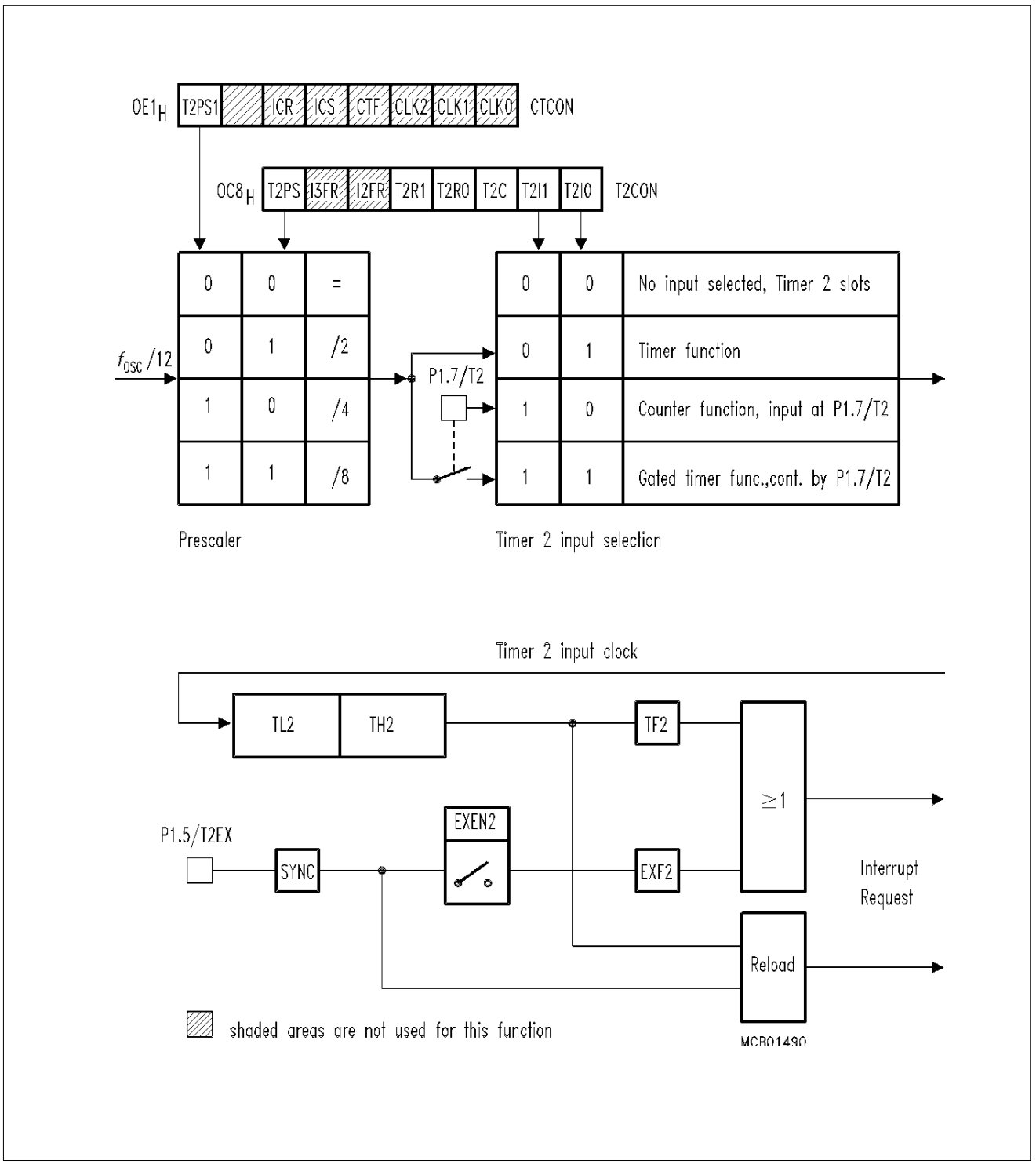


Figure 6
Block Diagram of Timer 2

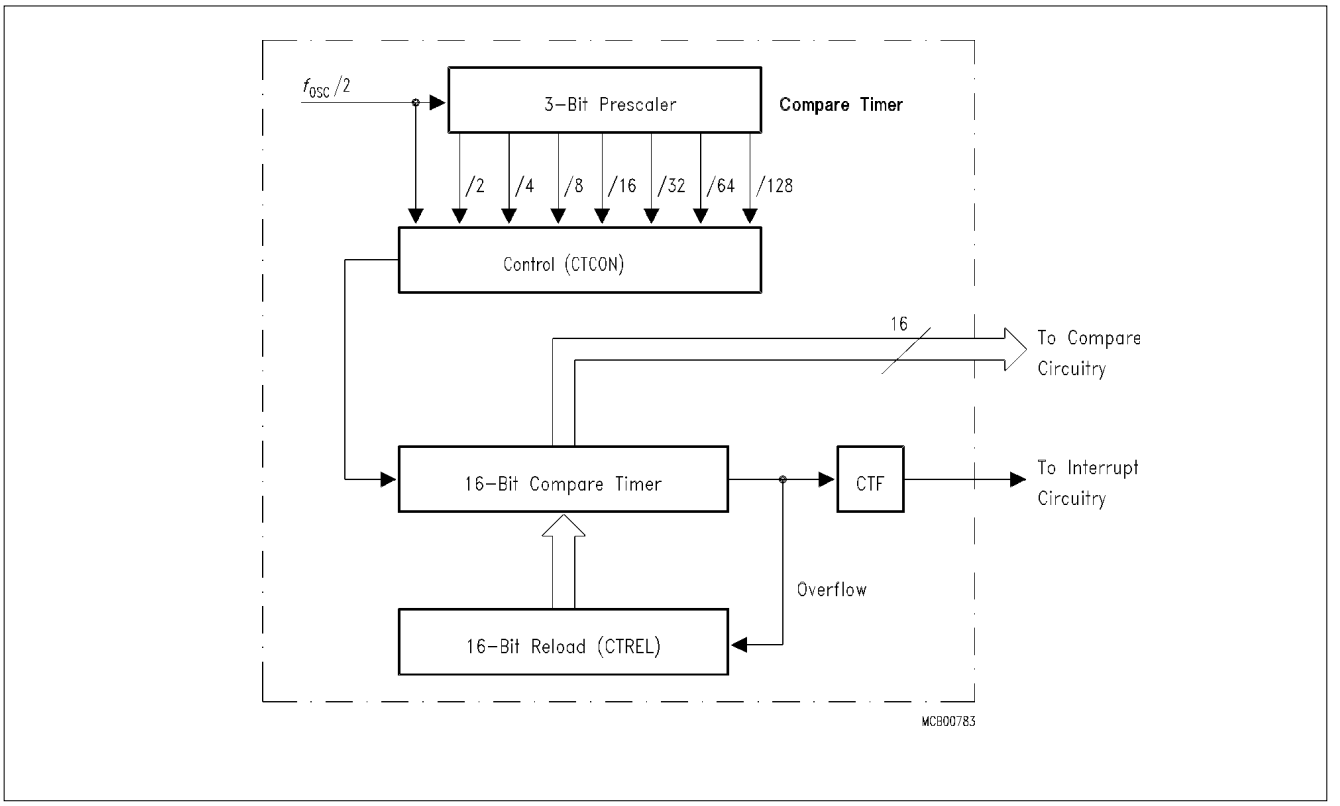


Figure 7
Block Diagram of the Compare Timer

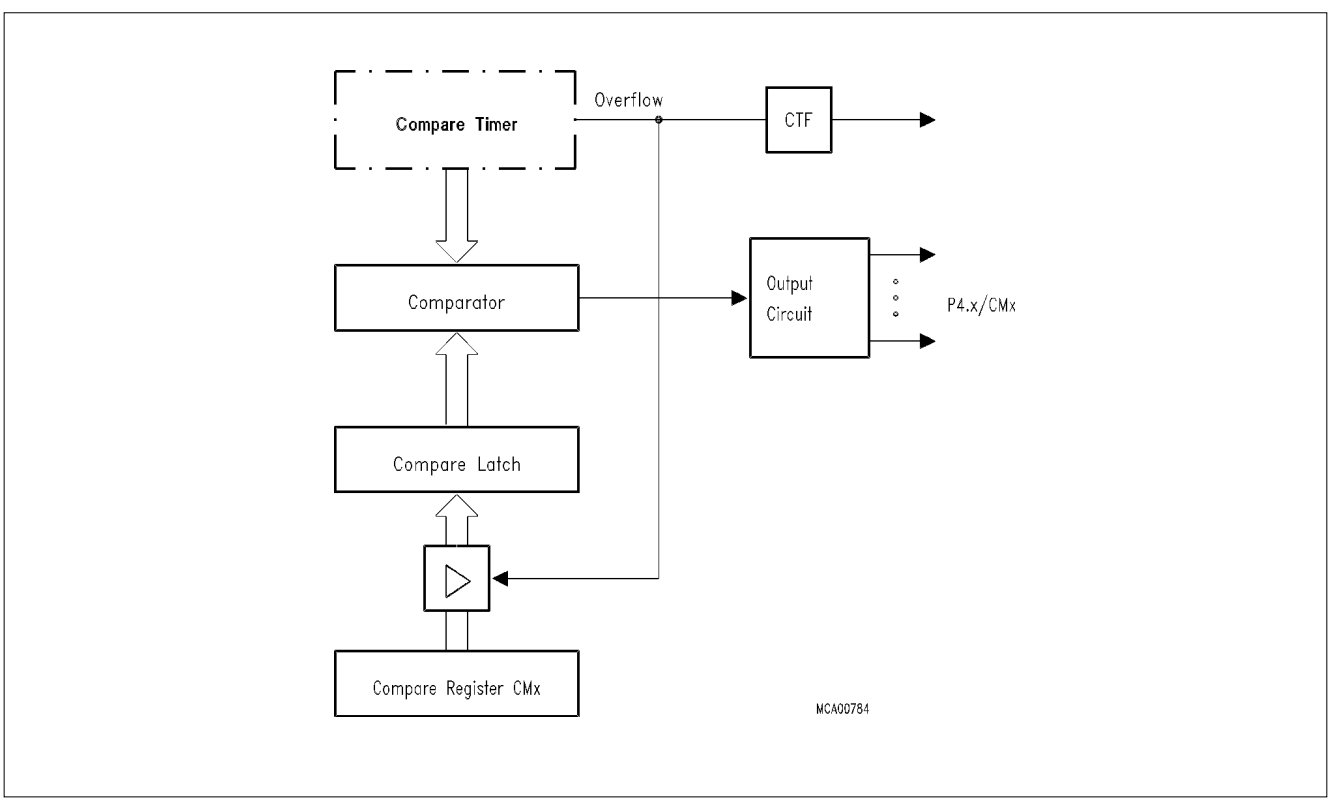


Figure 8
Compare-Mode 0 with Registers CM0 to CM7

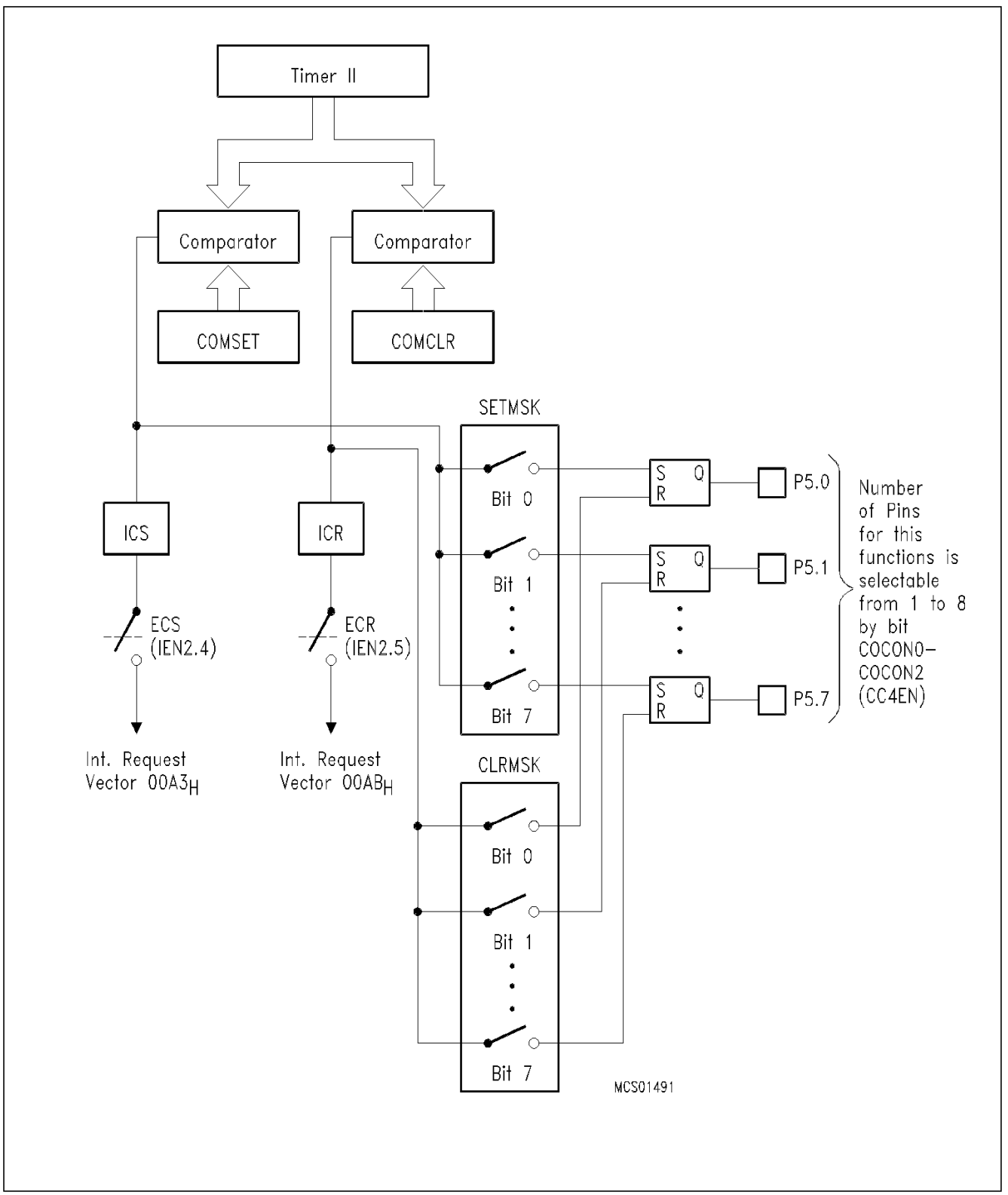


Figure 9
Compare-Mode 2 (Port 5 only)

Interrupt Structure

The SAB 80C517A has 17 interrupt vectors with the following vector addresses and request flags.

Table 5
Interrupt Sources and Vectors

Interrupt Request Flags	Interrupt Vector Address	Interrupt Source
IE0	0003_H	External interrupt 0
TF0	$000B_H$	Timer 0 overflow
IE1	0013_H	External interrupt 1
TF1	$001B_H$	Timer 1 overflow
RI0 + TI0	0023_H	Serial channel 0
TF2 + EXF2	$002B_H$	Timer 2 overflow/ext. reload
IADC	0043_H	A/D converter
IEX2	$004B_H$	External interrupt 2
IEX3	0053_H	External interrupt 3
IEX4	$005B_H$	External interrupt 4
IEX5	0063_H	External interrupt 5
IEX6	$006B_H$	External interrupt 6
RI1/TI1	0083_H	Serial channel 1
ICMP0 to ICMP7	0093_H	Compare match interrupt of Compare Registers CM0-CM7 assigned to Timer 2
CTF	$009B_H$	Compare timer overflow
ICS	$00A3_H$	Compare match interrupt of Compare Register COMSET
ICR	$00AB_H$	Compare match interrupt of Compare Register COMCLR

Each interrupt vector can be individually enabled/disabled. The response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 2 to 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs or triples. Each pair or triple can be programmed individually to one of four priority levels by setting or clearing one bit in special function register IP0 and one in IP1. Figure 9 shows the interrupt request sources, the enabling and the priority level structure.

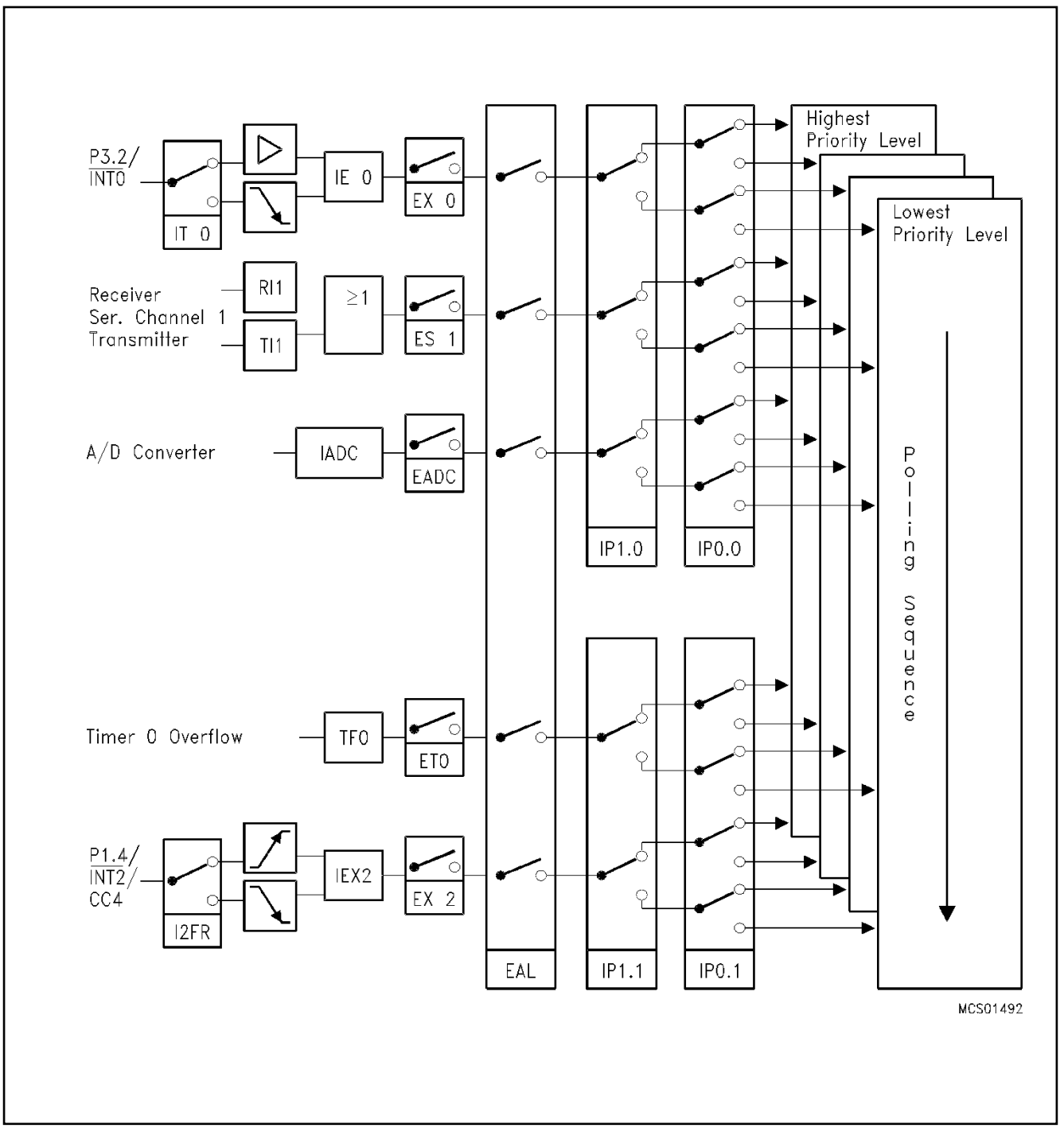


Figure 10
Interrupt Structure of the SAB 80C517A

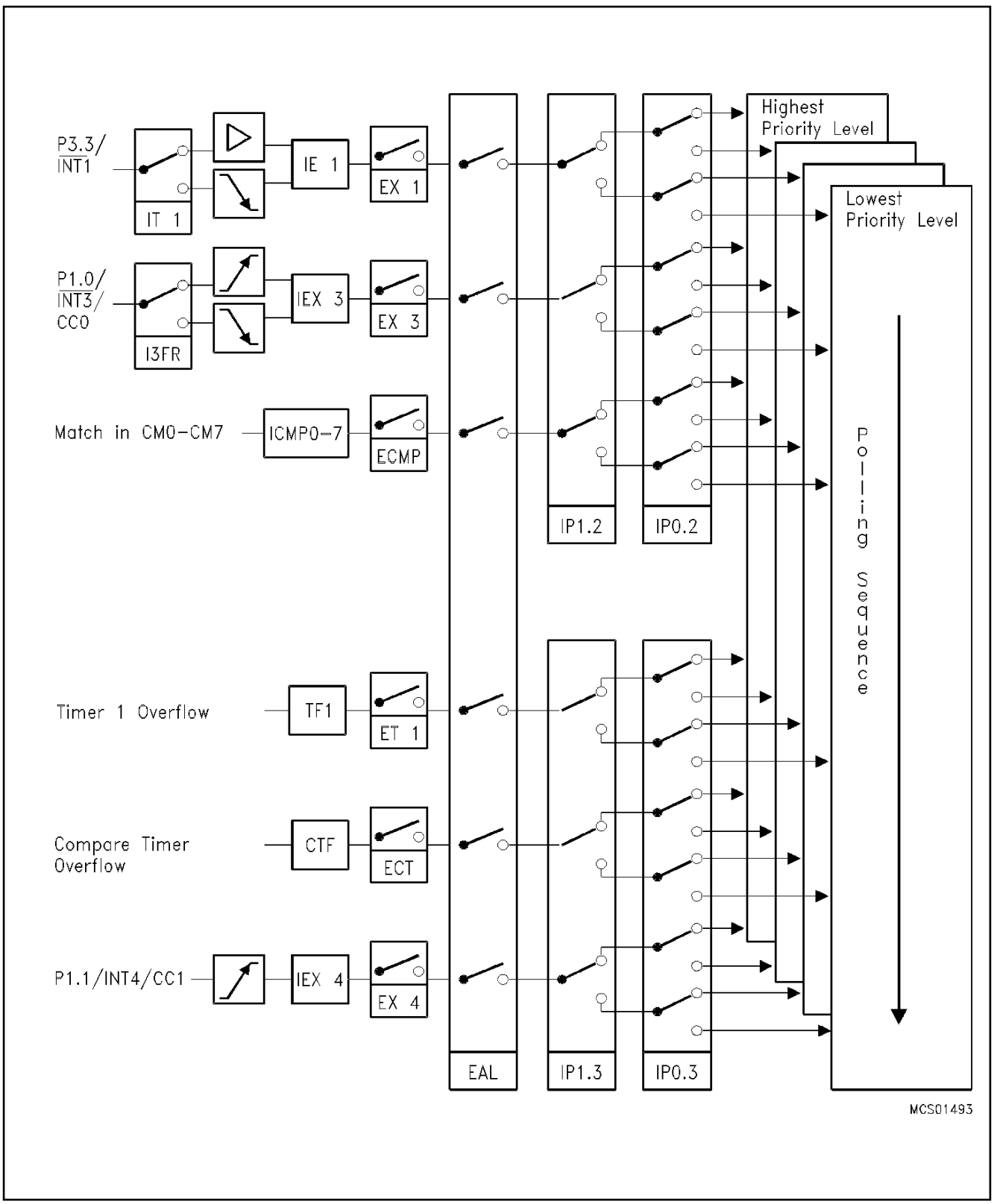


Figure 10
Interrupt Structure of the SAB 80C517A (cont'd)

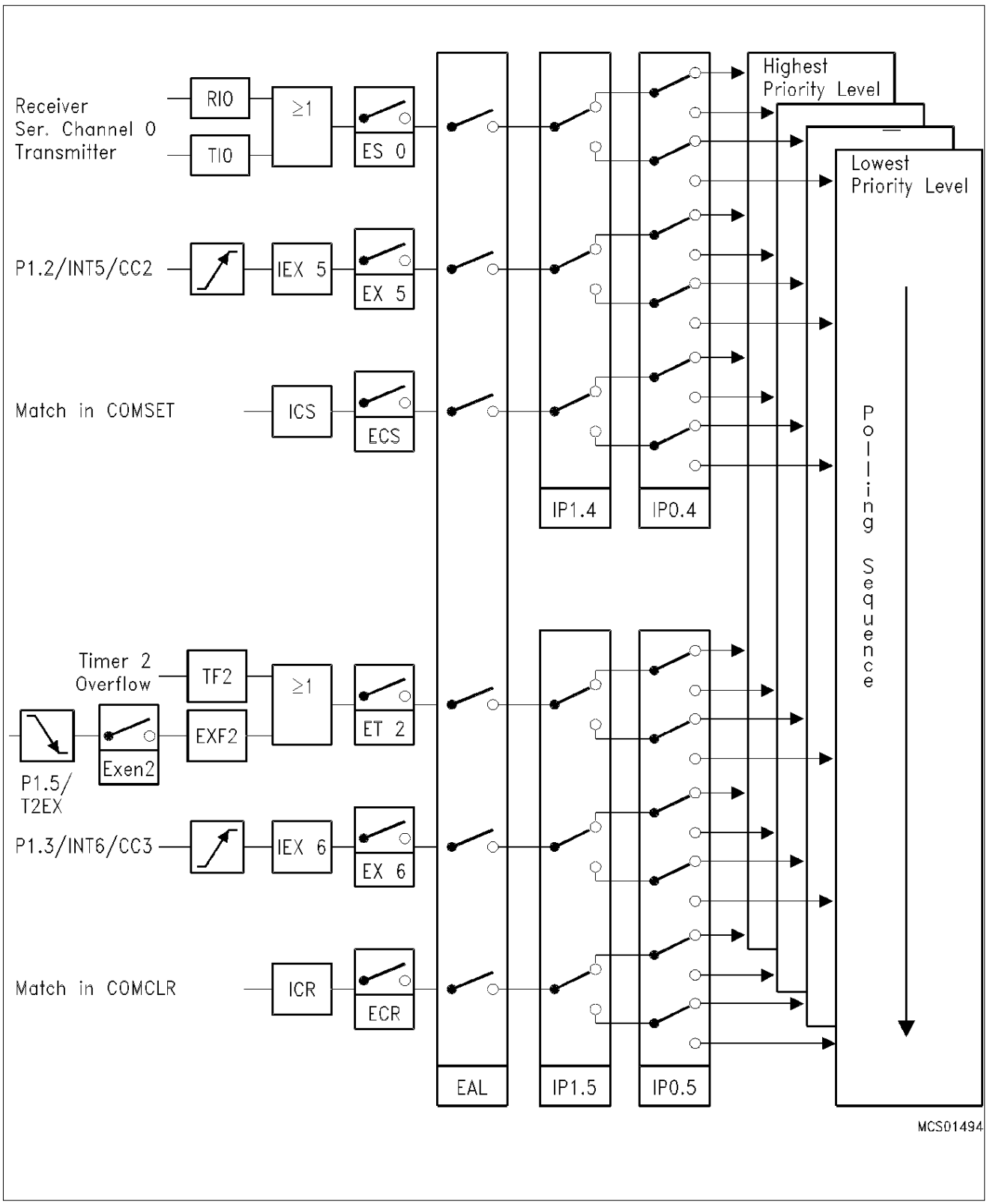


Figure 10
Interrupt Structure of the SAB 80C517A (cont'd)

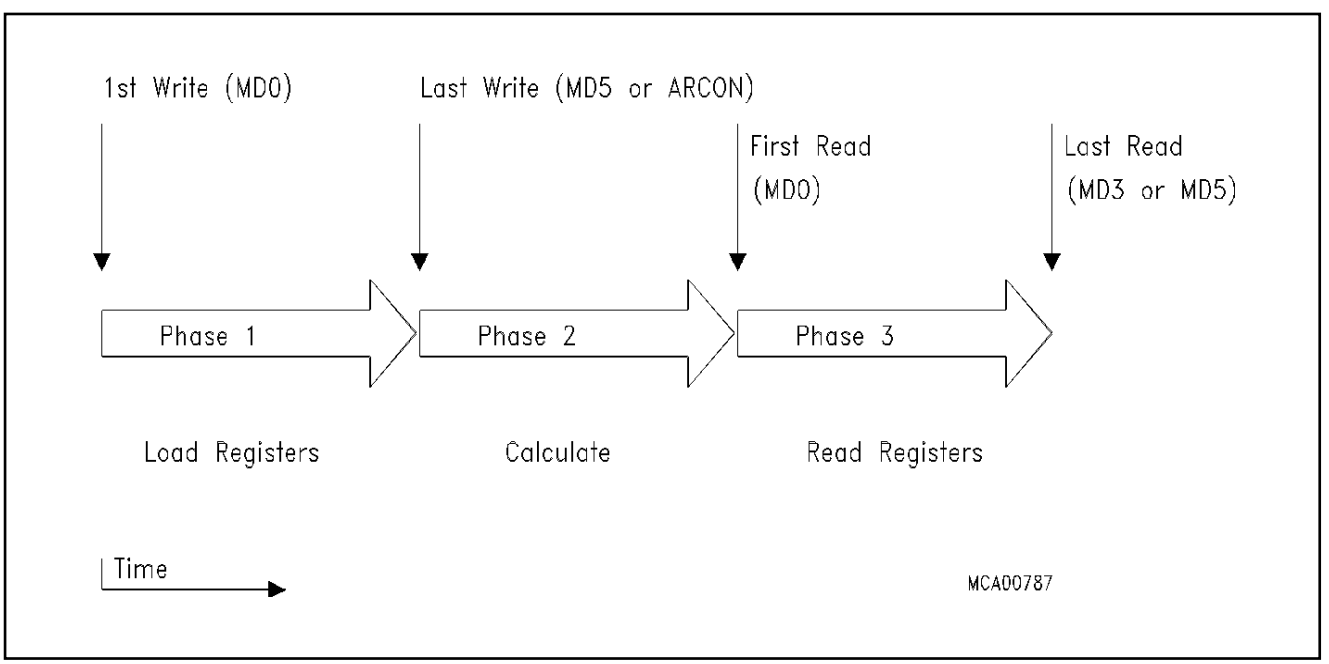
Multiplication/Division Unit

This on-chip arithmetic unit provides fast 32-bit division, 16-bit multiplication as well as shift and normalize features. All operations are integer operation.

Operation	Result	Remainder	Execution Time
32-bit/16-bit	32-bit	16-bit	6 t_{cy} [1]
16-bit/16-bit	16-bit	16-bit	4 t_{cy}
16-bit *16-bit	32-bit	–	4 t_{cy}
32-bit normalize	–	–	6 t_{cy} [2]
32-bit shift left/right	–	–	6 t_{cy} [2]

[1] 1 t_{cy} = 1 µs @ 12 MHz oscillator frequency.
[2] The maximal shift speed is 6 shifts/cycle.

The MDU consists of six registers used for operands and results and one control register. Operation of the MDU can be divided in three phases:



Operation of the MDU

To start an operation, register MD0 to MD5 (or ARCON) must be written to in a certain sequence according to table 5 or 6. The order the registers are accessed determines the type of the operation. A shift operation is started by a final write operation to register ARCON (see also the register description).

I/O Ports

The SAB 80C517A has seven 8-bit I/O ports and two input ports (8-bit and 4-bit wide).

Port 0 is an open-drain bidirectional I/O port, while ports 1 to 6 are quasi-bidirectional I/O ports with internal pull-up resistors. That means, when configured as inputs, ports 1 to 6 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pull-up FET. Port 1, 3, 4, 5 and port 6 provide several alternate functions. Please see the "Pin Description" for details.

Port pins show the information written to the port latches, when used as general purpose port. When an alternate function is used, the port pin is controlled by the respective peripheral unit. Therefore the port latch must contain a "one" for that function to operate. The same applies when the port pins are used as inputs. Ports 1, 3, 4 and 5 are bit- addressable.

The SAB 80C517A has two dual-purpose input ports. The twelve port lines at port 7 and port 8 can be used as analog inputs for the A/D converter. If input voltages at P7 and P8 meet the specified digital input levels (V_{IL} and V_{IH}) the port can also be used as digital input port.

In Hardware Power Down Mode the port pins and several control lines enter a floating state. For more details see the section about Hardware Power Down Mode.

Power Saving Modes

The SAB 80C517A provides – due to Siemens ACMOS technology – four modes in which power consumption can be significantly reduced.

- The **Slow Down Mode**
  The controller keeps up the full operating functionality, but is driven with one eighth of its normal operating frequency. Slowing down the frequency remarkable reduces power consumption.
- The **Idle Mode**
  The CPU is gated off from the oscillator, but all peripherals are still supplied with the clock and continue working.
- The **Power Down Mode**
  Operation of the SAB 80C517A is stopped, the on-chip oscillator and the RC-oscillator are turned off. This mode is used to save the contents of the internal RAM with a very low standby current.
- **The Hardware Power Down Mode**
  Operation of the SAB 80C517A is stopped, the on-chip oscillator and the RC-Oscillator are turned off. The pin $\overline{\text{HWPD}}$ controls this mode. Port pins and several control lines enter a floating state. The Hardware Power Down Mode is independent of the state of pin $\overline{\text{PE}}$/SWD.

Hardware Enable for Software controlled Power Saving Modes

A dedicated Pin $\overline{\text{PE}}$/SWD) of the SAB 80C517A allows to block the Software controlled power saving modes. Since this pin is mostly used in noise-critical application it is combined with an automatic start of the Watchdog Timer.

$\overline{\text{PE}}$/SWD = V_{IH} (logic high level):	Using of the power saving modes is not possible. The watchdog timer starts immediately after reset. The instruction sequences used for entering of power saving modes will not affect the normal operation of the device.
$\overline{\text{PE}}$/SWD = V_{IL} (logic low level):	All power saving modes can be activated by software.

When left unconnected, Pin /$\overline{\text{PE}}$/SWD is pulled high by a weak internal pullup. This is done to provide system protection on default.

The logic-level applied to pin $\overline{\text{PE}}$/SWD can be changed during program execution to allow or to block the use of the power saving modes without any effect on the on-chip watchdog circuitry.

Requirements for Hardware Power Down Mode

There is no dedicated pin to enable the Hardware Power Down Mode. Nevertheless for a correct function of the Hardware Power Down Mode the oscillator watchdog unit including its internal RC oscillator is needed. Therefore this unit must be enabled by pin OWE (OWE = high). However, the control pin $\overline{PE}$/SWD has no control function in this mode. It enables and disables only the use of software controlled power saving modes.

Software controlled power saving modes

All of these modes are entered by software. Special function register PCON (power control register, address is 87_H) is used to select one of these modes.

Slow Down Mode

During slow down operation all signal frequencies that are derived from the oscillator clock, are divided by eight, also the clockout signal and the watchdog timer count.

The slow down mode is enabled by setting bit SD. The controller actually enters the slow down mode after a short synchronisation period (max. 2 machine cycles).

The slow down mode is disabled by clearing bit SD.

Idle Mode

During idle mode all peripherals of the SAB 80C517A (except for the watchdog timer) are still supplied by the oscillator clock. Thus the user has to take care which peripheral should continue to run and which has to be stopped during Idle.

The procedure to enter the idle mode is similar to the one entering the power down mode. The two bits IDLE and IDLS must be set by two consecutive instructions to minimize the chance of unintentional activating of the idle mode.

There are two ways to terminate the idle mode:

– The idle mode can be terminated by activating any enabled interrupt. This interrupt will be serviced and the instruction to be executed following the RETI instruction will be the one following the instruction that set the bit IDLS.

– The other way to terminate the idle mode, is a hardware reset. Since the oscillator is still running, the hardware reset must be held active only for two machine cycles for a complete reset.

Normally the port pins hold the logical state they had at the time idle mode was activated. If some pins are programmed to serve their alternate functions they still continue to output during idle mode if the assigned function is on. The control signals ALE and hold at logic high levels $\overline{PSEN}$ (see table 8).

Power Down Mode

The power down mode is entered by two consecutive instructions directly following each other. The first instruction has to set the flag PDE (power down enable) and must not set PDS (power down set). The following instruction has to set the start bit PDS. Bits PDE and PDS will automatically be cleared after having been set.

The instruction that sets bit PDS is the last instruction executed before going into power down mode. The only exit from power down mode is a hardware reset.

The status of all output lines of the controller can be looked up in table 8.

Hardware Controlled Power Down Mode

The pin $\overline{\text{HWPD}}$ controls this mode. If it is on logic high level (inactive) the part is running in the normal operating modes. If pin $\overline{\text{HWPD}}$ gets active (low level) the part enters the Hardware Power Down Mode; this is independent of the state of pin $\overline{\text{PE}}$/SWD.

$\overline{\text{HWPD}}$ is sampled once per machine cycle. If it is found active, the device starts a complete internal reset sequence. The watchdog timer is stopped and its status flag WDTS is cleared exactly the same effects as a hardware reset. In this phase the power consumption is not yet reduced. After completion of the internal reset both oscillators of the chip are disabled. At the same time the port pins and several control lines enter a floating state as shown in table 8. In this state the power consumption is reduced to the power down current IPD. Also the supply voltage can be reduced. Table 8 also lists the voltages which may be applied at the pins during Hardware Power Down Mode without affecting the low power consumption.

Termination of HWPD Mode:

This power down state is maintained while pin $\overline{\text{HWPD}}$ is held active. If HWPD goes to high level (inactive state) an automatic start up procedure is performed:

- First the pins leave their floating condition and enter their default reset state (as they had immediately before going to float state).
- Both oscillators are enabled (only if OWE = high). The oscillator watchdog's RC oscillator starts up very fast (typ. less than 2 microseconds).
- Because the oscillator watchdog is active it detects a failure condition if the on-chip oscillator hasn't yet started. Hence, the watchdog keeps the part in reset and supplies the internal clock from the RC oscillator.
- Finally, when the on-chip oscillator has started, the oscillator watchdog releases the part from reset with oscillator watchdog status flag not set.
  When automatic start of the watchdog was enabled ($\overline{\text{PE}}$/SWD connected to V_{CC}), the Watchdog Timer will start, too (with its default reload value for time-out period).
- The $\overline{\text{Reset}}$ pin overrides the Hardware Power Down function, i.e. if reset gets active during Hardware Power Down it is terminated and the device performs the normal reset function. (Thus, pin $\overline{\text{Reset}}$ has to be inactive during Hardware Power Down Mode).

Table 8
Status of all pins during Idle Mode, Power Down Mode and Hardware Power Down Mode

Pins	Idle Mode Last instruction executed from		Power Down Mode Last instruction executed from		Hardware Power Down	
	internal ROM	external ROM	internal ROM	external ROM	Status	Voltage range at pin
P0	Data	float	Data	float		
P1	Data alt outputs	Data alt outputs	Data last outputs	Data last outputs	floating	
P2	Data	Address	Data	Data	output	
P3	Data alt outputs	Data alt outputs	Data last output	Data last output	outputs	
P4	Data alt outputs	Data alt outputs	Data last outputs	Data last output	disabled	$V_{SS} \leq V_{IN} \leq V_{CC}$
P5	Data alt output	Data alt output	Data last output	Data last output	input	
P6	Data alt output	Data alt output	Data last output	Data last output	function	
P7						
P8						
EA					active input	$V_{IN} = V_{CC}$ or $V_{IN} = V_{SS}$
$\overline{PE}$/SWD					active input pull-up disabled	$V_{IN} = V_{CC}$ or $V_{IN} = V_{SS}$
XTAL1					active output	pin may not be driven
XTAL2					disabled input functions	$V_{SS} \leq V_{IN} \leq V_{CC}$

Table 8
Status of all pins during Idle Mode, Power Down Mode and Hardware Power Down Mode (cont'd)

Pins	Idle Mode Last instruction executed from		Power Down Mode Last instruction executed from		Hardware Power Down	
	internal ROM	**external ROM**	**internal ROM**	**external ROM**	**Status**	**Voltage range at pin**
$\overline{\text{PSEN}}$					floating outp. disabled input functions	$V_{SS} \leq V_{IN} \leq V_{CC}$
ALE						
VAREF VAGND					active supply pins	$V_{AGND} \leq V_{IN} \leq V_{CC}$
OWE					active input, must be high pull-up disabl.	$V_{IN} = V_{CC}$
$\overline{\text{RESET}}$					active input must be high	$V_{IN} = V_{CC}$
$\overline{\text{RO}}$					floating output	$V_{SS} \leq V_{IN} \leq V_{CC}$

Serial Interfaces

The SAB 80C517A has two serial interfaces. Both interfaces are full duplex and receive buffered. They are functionally identical with the serial interface of the SAB 8051 when working as asynchronous channels. Serial interface 0 additionally has a synchronous mode. Table 9 shows possible configurations and the according baud rates.

Table 9
Baud Rate Generation

	Mode		**Mode 0**			–
8-Bit syn-chron-ous channel	Baud-rate	f_{OSC} =12 MHz	1MHz			–
		f_{OSC} = 16 MHz	1.33 MHz			–
		f_{OSC} = 18 MHz	1.5 MHz			–
	derived from		f_{OSC}			–
	Mode		**Mode 1**			**Mode B**
8-Bit UART	Baud-rate	f_{OSC} = 12 MHz	1 Baud – 62.5 kBaud		183 Baud – 375 kBaud	366 Baud – 375 kBaud
		f_{OSC} = 16 MHz	1 Baud – 83 kBaud		244 Baud – 500 kBaud	244 Baud – 500 kBaud
		f_{OSC} = 18 MHz	1 Baud – 93.7 kBaud		2375 Baud – 562.5 kBaud	549 Baud – 562.5 kBaud
	derived from		Timer 1		10-Bit Baudrate Generator	10-Bit Baudrate Generator
	Mode		**Mode 2**	**Mode 3**		**Mode A**
9-Bit UART	Baud-rate	f_{OSC} = 12 MHz	187.5 kBaud/ 375 kBaud	1 Baud – 62.5 kBaud	183 Baud – 75 kBaud	183 Baud – 75 kBaud
		f_{OSC}= 16 MHz	250 Baud/ 500 kBaud	1 Baud – 83.3 kBaud	244 Baud – 500 kBaud	244 Baud – 500 kBaud
		f_{OSC} = 18 MHz	281.2 kBaud/ 562.5 kBaud	1 Baud – 93.7 kBaud	275 Baud 562.5 kBaud	549 Baud – 562.5 kBaud
	derived from	$f_{OSC}/2$	Timer 1	10-Bit Baudrate Generator		10-Bit Baudrate Generator

Serial Interface 0

Serial Interface 0 can operate in 4 modes:

Mode 0: Shift register mode:
Serial data enters and exits through R × D0. T × D0 outputs the shift clock 8 data bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 8-bit UART, variable baud rate:
10-bit are transmitted (through T × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On reception, the stop bit goes into RB80 in special function register S0CON. The baud rate is variable.

Mode 2: 9-bit UART, fixed baud rate:
11-bit are transmitted (through T × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). On transmission, the 9th data bit (TB80 in S0CON) can be assigned to the value of 0 or 1. For example, the parity bit (P in the PSW) could be moved into TB80 or a second stop bit by setting TB80 to 1. On reception the 9th data bit goes into RB80 in special function register S0CON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 9-bit UART, variable baud rate:
11-bit are transmitted (through T × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). In fact, mode 3 is the same as mode 2 in all respects except the baud rate. The baud rate in mode 3 is variable.

Variable Baud Rates for Serial Interface 0

Variable baud rates for modes 1 and 3 of serial interface 0 can be derived from either timer 1 or a dedicated Baudrate Generator.

The baud rate is generated by a free running 10-bit timer with programmable reload register.

$$\text{Mode 1.3 baud rate} = \frac{2^{SMOD} * f_{OSC}}{64*(2^{10}\text{-S0REL})}$$

The default value after reset in the reload registers S0RELL and S0RELH provide a baud rate of 4.8 kBaud (SMOD = 0) or 9.6 kBaud (SMOD = 1) at 12 MHz oscillator frequency. This guarantees full compatibility to the SAB 80C517.

Serial Interface 1

Serial interface 1 can operate in two asynchronous modes:

Mode A: 9-bit UART, variable baud rate.
11 bits are transmitted (through T × D1) or received (through R × D1): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). On transmission, the 9th data bit (TB81 in S1CON) can be assigned to the value of 0 or 1. For example, the parity bit (P in the PSW) could be moved into TB81 or a second stop bit by setting TB81 to 1. On reception the 9th data bit goes into RB81 in special function register S1CON, while the stop bit is ignored.

Mode B: 8-bit UART, variable baud rate.
10 bits are transmitted (through T × D1) or received (through R × D1): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On reception, the stop bit goes into RB81 in special function register S1CON.

Variable Baud Rates for Serial Interface 1.

Variable baud rates for modes A and B of serial interface 1 are derived from a dedicated baud rate generator.

The baud rate clock (baud rate = $\frac{\text{baud rate clock}}{16}$) is generated by an 10-bit free running timer with programmable reload register.

Mode A, B baudrate = $\frac{f_{OSC}}{32 * (2^{10} - \text{SREL})}$

Watchdog Units

The SAB 80C517A offers two enhanced fail safe mechanisms, which allow an automatic recovery from hardware failure or software upset:

– programmable watchdog timer (WDT), variable from 512 µs up to appr. 1.1 s time-out period @12 MHz. Upward compatible to SAB 80515 watchdog.

– oscillator watchdog (OWD), monitors the on-chip oscillator and forces the micro-controller into reset state, in case the on-chip oscillator fails, controls the restart from the Hardware Power Down Mode and provides clock for a fast internal reset after power-on.

Programmable Watchdog Timer

The WDT can be activated by hardware or software.

Hardware initialization is done when pin $\overline{PE}$/SWD (Pin 4) is held high during RESET. The SAB 80C517A then starts program execution with the WDT running. Since Pin $\overline{PE}$/SWD is only sampled during Reset (and hardware power down at parts with stepping code AD and later) dynamical switching of the WDT is not possible.

Software initialization is done by setting bit SWDT.

A refresh of the watchdog timer is done by setting bits WDT and SWDT consecutively.

A block diagram of the watchdog timer is shown in figure 11.

When a watchdog timer resest occurs, the watchdog timer keeps on running, but a status flag WDTS is set. This flag can also be cleared by software.

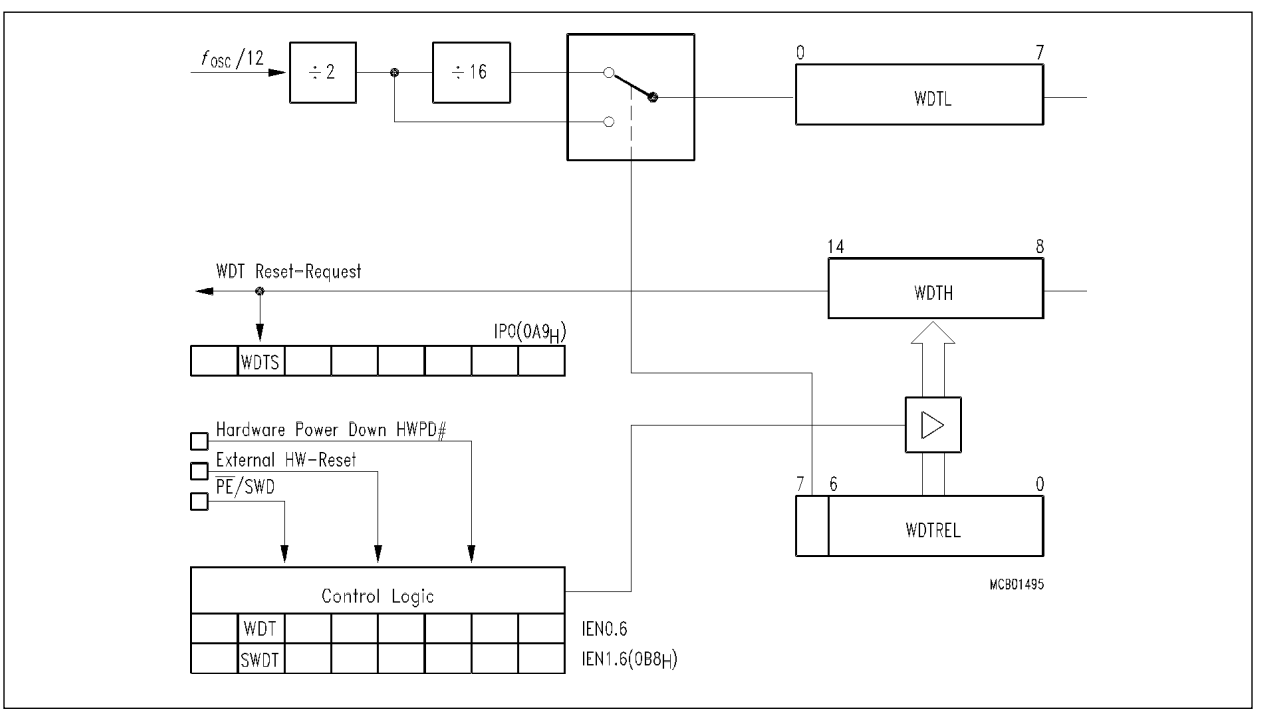


Figure 11
Block Diagram of the Programmable Watchdog Timer

Oscillator Watchdog

The unit serves three functions:

– Monitoring of the on-chip oscillator's function.
  The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is forced into reset; if the failure condition disappears (i.e. the on-chip oscillator has again a higher frequency than the RC oscillator), the part executes a final reset phase of appr. 0.25 ms in order to allow the oscillator to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.

– Restart from the Hardware Power Down Mode.
  If the Hardware Power Down Mode is terminated the oscillator watchdog has to control the correct start-up of the on-chip oscillator and to restart the program. The oscillator watchdog function is only part of the complete Hardware Power Down sequence; however, the watchdog works identically to the monitoring function.

– Fast internal reset after power-on.
  In this function the oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. In this case the oscillator watchdog unit also works identically to the monitoring function.

If the oscillator watchdog unit is to be used it must be enabled (this is done by applying high level to the control pin OWE).

Figure 12 shows the block diagram of the oscillator watchdog unit. It consists of an internal RC oscillator which provides the reference frequency of the on-chip oscillator. The RC oscillator can be enabled/disabled by the control pin OWE. If it is disabled the complete unit has no function.

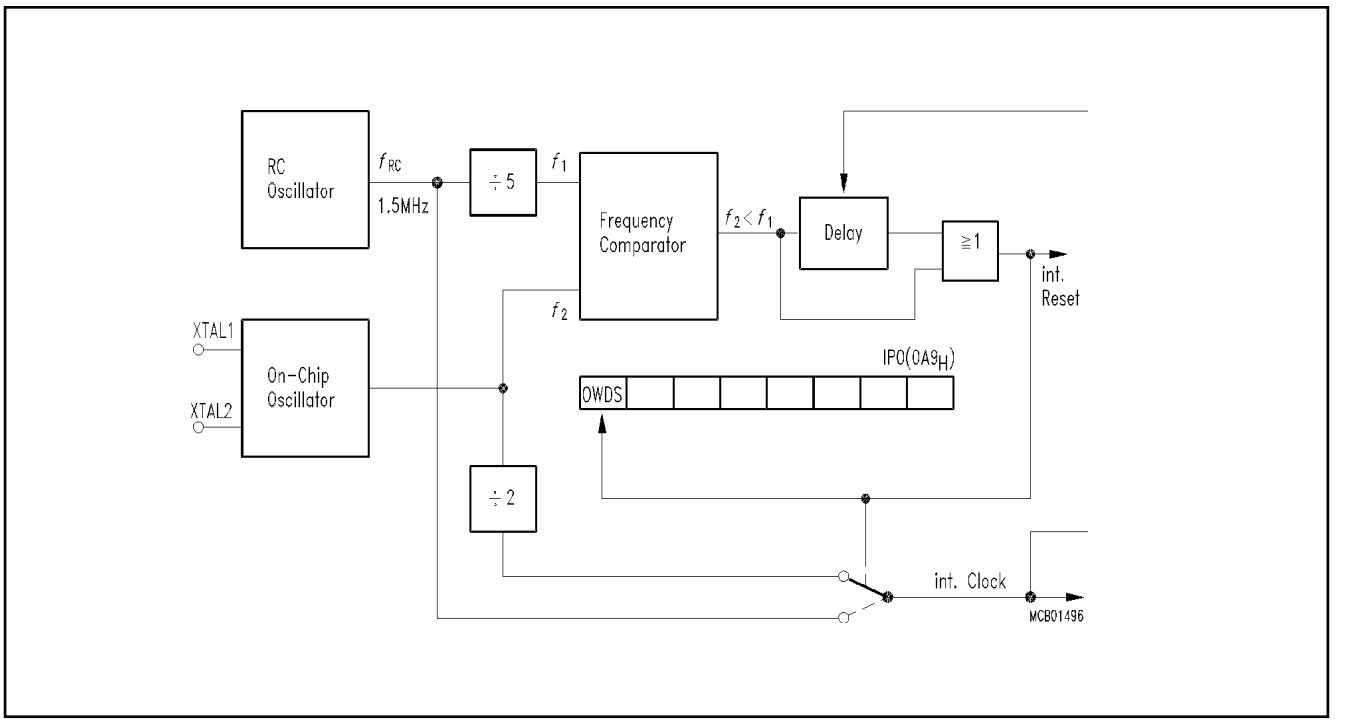


Figure 12
Functional Block Diagram of the Oscillator Watchdog

Fast internal reset after power-on

The SAB 80C517A can use the oscillator watchdog unit for a fast internal reset procedure after power-on.

Normally members of the 8051 family (like the SAB 80C517) enter their default reset state not before the on-chip oscillator starts. The reason is that the external reset signal must be internally synchronized and processed in order to bring the device into the correct reset state. Especially if a crystal is used the start up time of the oscillator is relatively long (typ. 1 ms). During this time period the pins have an undefined state which could have severe effects e.g. to actuators connected to port pins.

In the SAB 80C517A the oscillator watchdog unit avoids this situation. However, the oscillator watchdog must be enabled. In this case, after power-on the oscillator watch-dog's RC oscillator starts working within a very short start-up time (typ. less than 2 micro-seconds). In the following the watchdog circuitry detects a failure condition for the on-chip oscillator because this has not yet started (a failure is always recognized if the watchdog's RC oscillator runs faster than the on-chip oscillator). As long as this condition is valid the watchdog uses the RC oscillator output as clock source for the chip rather than the on-chip oscillator's output.This allows correct resetting of the part and brings also all ports to the defined state.

Delay time between power-on and correct reset state:

Typ.: 18 µs
Max.: 34 µs

Instruction Set

The SAB 80C517A / 83C517A-5 has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function Registers, Interrupt Vectors and Assembler Directives.

Literature Information

Title	Ordering No.
Microcontroller Family SAB 8051 Pocket Guide	B158-H6497-X-X-7600

Absolute Maximum Ratings

Ambient temperature under bias ..... – 40 to 110° C
Storage temperature ..... – 65 to 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS}) ..... – 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}) ..... – 0.5 to V_{CC} +0.5 V
Input current on any pin during overload condition ..... – 10mA to +10mA
Absolute sum of all input currents during overload condition ..... |100mA|
Power dissipation ..... 1 W

Note *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions (V_{IN} > V_{CC} or V_{IN} < V_{SS}) theVoltage on V_{CC} pins with respect to ground (V_{SS}) must not exeed the values definded by the absolute maximum ratings.*

DC Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V
T_A = 0 to 70 °C for the SAB 80C517A/83C517A-5
T_A = – 40 to 85 °C for the SAB 80C517A-T3/83C517A-5-T3
T_A = – 40 to 110 °C for the SAB 80C517A-T4/83C517A-5-T4

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Input low voltage (except $\overline{EA}$, $\overline{RESET}$, $\overline{HWPD}$)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage ($\overline{HWPD}$, $\overline{RESET}$)	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (except $\overline{RESET}$, XTAL2 and $\overline{HWPD}$	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL2	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage to $\overline{RESET}$ and $\overline{HWPD}$	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Output low voltage (ports 1, 2, 3, 4, 5, 6)	V_{OL}	–	0.45	V	I_{OL}=1.6 mA[1]
Output low voltage (ports ALE, $\overline{PSEN}$, $\overline{RO}$)	V_{OL1}	–	0.45	V	I_{OL}=3.2 mA [1]
Output high voltage (ports 1, 2, 3, 4, 5, 6)	V_{OH}	2.4 0.9 V_{CC}	– –	V V	I_{OH} =–80 µA I_{OH} =–10 µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$, $\overline{RO}$)	V_{OH1}	2.4 0.9 V_{CC}	– –	V V	I_{OH} =–800 µA[2] I_{OH} =–80 µA[2]
Logic input low current (ports 1, 2, 3, 4, 5, 6)	I_{IL}	– 10	– 70	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 1, 2, 3, 4, 5, 6)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$, ports 7, 8, $\overline{HWPD}$)	I_{LI}	–	± 100	nA	0.45 < V_{IN} < V_{CC}
			± 150	nA	0.45 < V_{IN} < V_{CC} T_A > 100 °C
Input low current to $\overline{RESET}$ for reset	I_{IL2}	– 10	–100	µA	V_{IN} = 0.45 V
Input low current (XTAL2)	I_{IL3}	–	– 15	µA	V_{IN} = 0.45 V
Input low current ($\overline{PE}$/SWD, OWE)	I_{IL4}	–	– 20	µA	V_{IN} = 0.45 V
Pin capacitance	C_{IO}	–	10	pF	f_C= 1 MHz T_A= 25 °C
Power supply current:					
Active mode, 12 MHz[7]	I_{CC}	–	28	mA	V_{CC} = 5 V,[4]
Active mode, 18 MHz[7]	I_{CC}	–	37	mA	V_{CC} = 5 V,[4]
Idle mode, 12 MHz[7]	I_{CC}	–	24	mA	V_{CC} = 5 V,[5]
Idle mode, 18 MHz[7]	I_{CC}	–	31	mA	V_{CC} = 5 V,[5]
Slow down mode, 12 MHz	I_{CC}	–	12	mA	V_{CC} = 5 V,[6]
Slow down mode, 18 MHz	I_{CC}	–	16	mA	V_{CC} = 5 V,[6]
Power Down Mode	I_{PD}	–	50	µA	V_{CC} = 2...5.5 V, [3]

Notes see page 63.

Notes for page 62:

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1, 3, 4, 5 and 6. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (Power down mode) is measured with:
$\overline{EA}$ = $\overline{RESET}$ = V_{CC}; Port0 = Port7 = Port8 = V_{CC}; XTAL1 = N.C.; XTAL2 = V_{SS};
$\overline{PE}$/SWD = OWE = V_{SS};$\overline{HWDP}$ = V_{CC} (Software Power Down mode); V_{AREF} = V_{CC};
V_{AGND} = V_{SS}; all other pins are disconnected. Hardware Powerdown I_{PD} : OWE =V_{CC} or V_{SS}. No certain pin connection for the other pins.

4) I_{CC} (active mode) is measured with:
XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL1 = N.C.;
$\overline{EA}$ = $\overline{PE}$/SWD = V_{CC}; Port0 = Port7 = Port8 = V_{CC}; $\overline{HWPD}$ = V_{CC}; $\overline{RESET}$ = V_{SS}
all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V;
XTAL1 = N.C.; $\overline{RESET}$ = V_{CC}; $\overline{HWPD}$ = V_{CC}; Port0 = Port7 = Port8 =V_{CC} ;
$\overline{EA}$ = $\overline{PE}$/SWD = V_{SS}; all other pins are disconnected;

6) I_{CC} (slow down mode) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} =V_{CC} – 0.5 V;
XTAL1 = N.C.;$\overline{RESET}$= V_{CC}; $\overline{HWPD}$ = V_{CC}; Port7 = Port8 = V_{CC}; $\overline{EA}$ = $\overline{PE}$/SWD = V_{SS} ;
all other pins are disconnected;

7) $I_{CC\,Max}$ at other frequencies is given by:
active mode: I_{CC} (max) = 1.50* f_{OSC} + 10
idle mode: I_{CC} (max) = 1.17* f_{OSC} + 10
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

A/D Converter Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V
V_{AREF} = V_{CC} ± 5%; V_{AGND} = V_{SS} ± 0.2 V;
T_A = 0 to 70 °C for the SAB 80C517A/83C517A-5
T_A = – 40 to 85 ° C for the SAB 80C517A-T3/83C517A-5-T3
T_A = – 40 to 110 °C for the SAB 80C517A-T4/83C517A-5-T4

Parameter	Symbol	Limit values			Unit	Test condition
		min.	typ.	max.		
Analog input capacitance	C_I		25	70	pF	
Sample time (inc. load time)	T_S			4 t_{CY}[1]	µs	[2]
Conversion time (inc. sample time)	T_C			14 t_{CY}[1]	µs	[3]
Total unadjusted error	TUE			± 2	LSB	V_{AREF} = V_{CC} V_{AGND} = V_{SS}
V_{AREF} supply current	I_{REF}		± 20		µA	[4]

1) t_{CY} = (8*2^{ADCL}) /f_{OSC}; (t_{CY} = 1/f_{ADC}; f_{ADC} = f_{OSC}/(8*2^{ADCL}))
2) This parameter specifies the time during the input capacitance C_I, can be charged/discharged by the external source. It must be guaranteed, that the input capacitance C_I, is fully loaded within this time. 4TCY is 2 µs at the f_{OSC}= 16 MHz. After the end of the sample time T_S, changes of the analog input voltage have no effect on the conversion result.
3) This parameter includes the sample time T_S. 14TCY is 7 µs at f_{OSC} = 16 MHz.
4) The differencial impedance r_D of the analog reference source must be less than 1 KΩ at reference supply voltage.

AC Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB 80C517A/83C517A-5
T_A = – 40 to 85 °C for the SAB 80C517A-T3/83C517A-5-T3
T_A = – 40 to110 ° C for the SAB 80C517A-T4/83C517A-5-T4

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Parameter	Symbol	Limit values				Unit
		18 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 18 MHz		
		min.	max.	min.	max.	

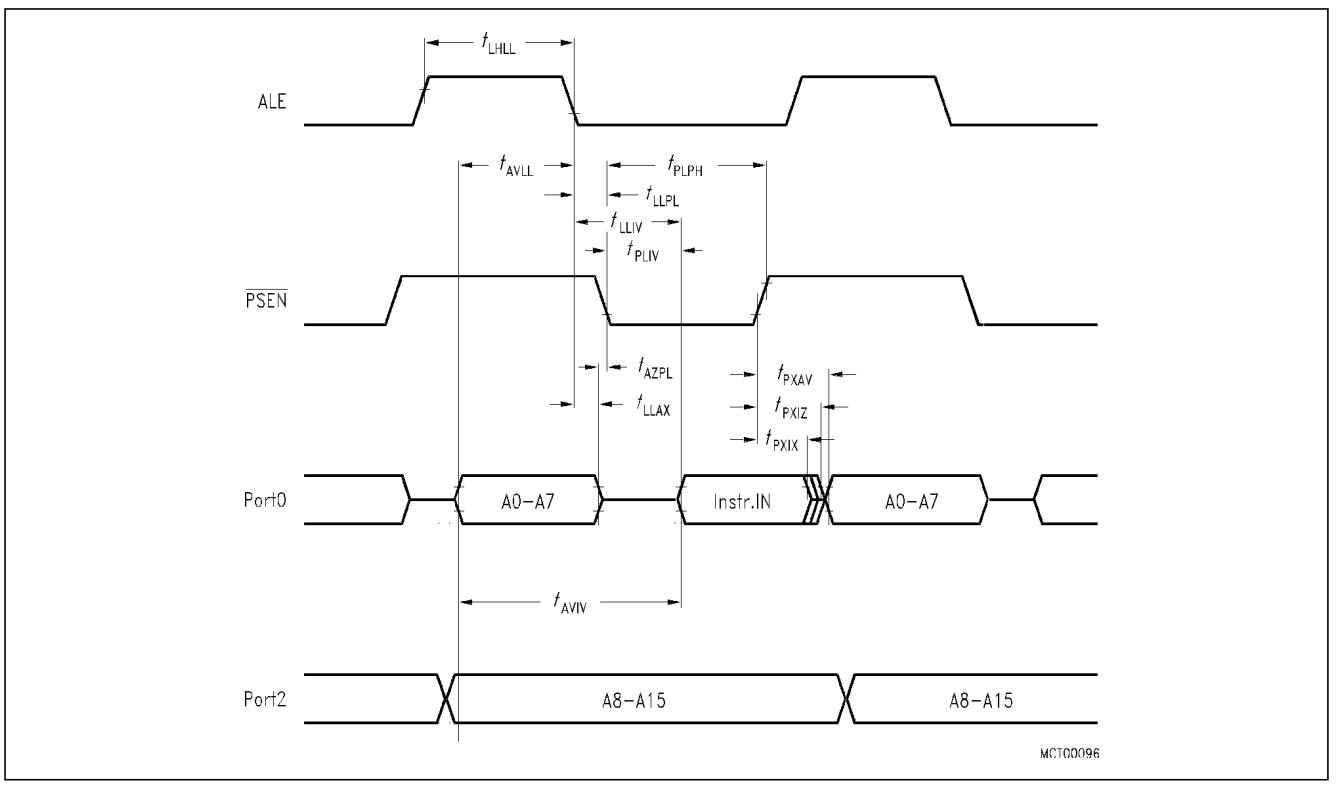
Program Memory Characteristics

ALE pulse width	t_{LHLL}	71	–	2 t_{CLCL} – 40	–	ns
Address setup to ALE	t_{AVLL}	26	–	t_{CLCL} – 30	–	ns
Address hold after ALE	t_{LLAX}	26	–	t_{CLCL} – 30	–	ns
ALE to valid instruction	t_{LLIV}	–	122	–	4t_{CLCL} – 100	ns
ALE to $\overline{PSEN}$	t_{LLPL}	31	–	t_{CLCL} – 25	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	132	–	3 t_{CLCL} – 35	–	ns
$\overline{PSEN}$ to valid instruction	t_{PLIV}	–	92	–	3t_{CLCL} – 75	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0		ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}	–	46	–	t_{CLCL} – 10	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	48	–	t_{CLCL} – 8	–	ns
Address to valid instr in	t_{AVIV}	–	218	–	5t_{CLCL} – 60	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

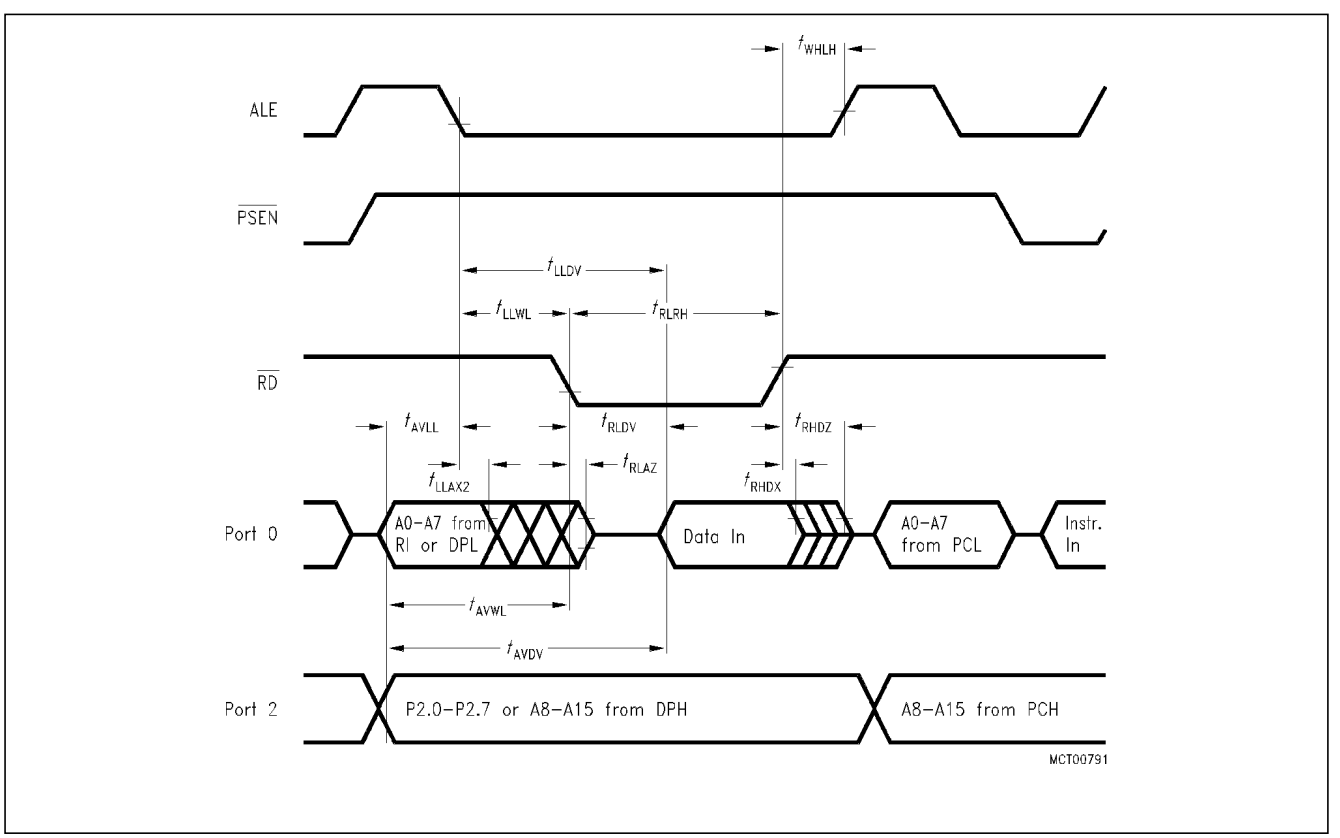
*) Interfacing the SAB 80C517A to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

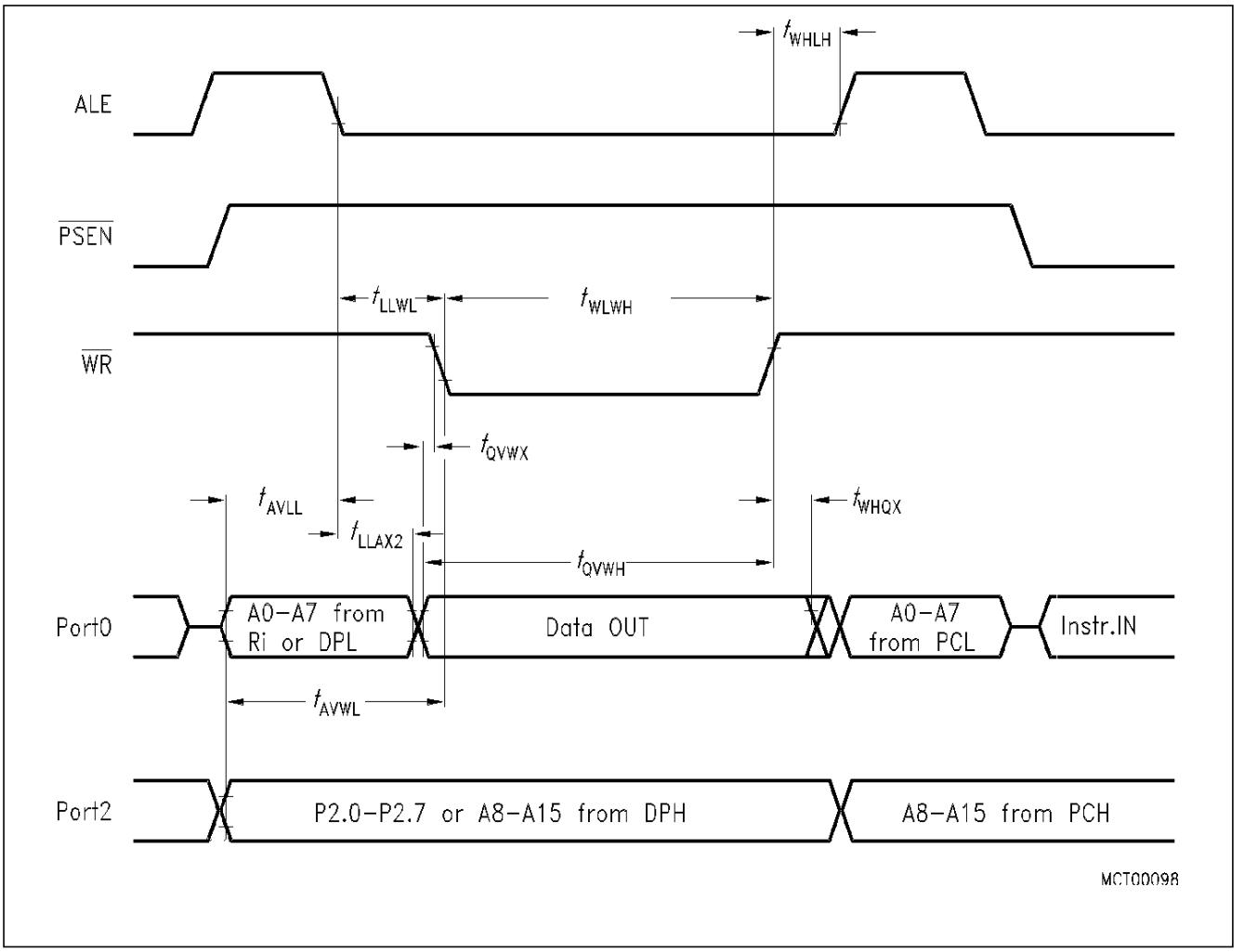
Parameter	Symbol	Limit values				Unit
		18 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 18 MHz		
		min.	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	233	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	233	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	81	–	2 t_{CLCL} – 30	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	128	–	5 t_{CLCL} – 150	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	51	–	2 t_{CLCL} – 60	ns
ALE to valid data in	t_{LLDV}	–	294	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	335	–	9 t_{CLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	117	217	3 t_{CLCL} – 50	3 t_{CLCL} +50	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	16	96	t_{CLCL} – 40	t_{CLCL} +40	ns
Address valid to $\overline{WR}$	t_{AVWL}	92	–	4 t_{CLCL} – 130	–	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	11	–	t_{CLCL} – 45	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	239	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	16	–	t_{CLCL} – 40	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns



Program Memory Read Cycle



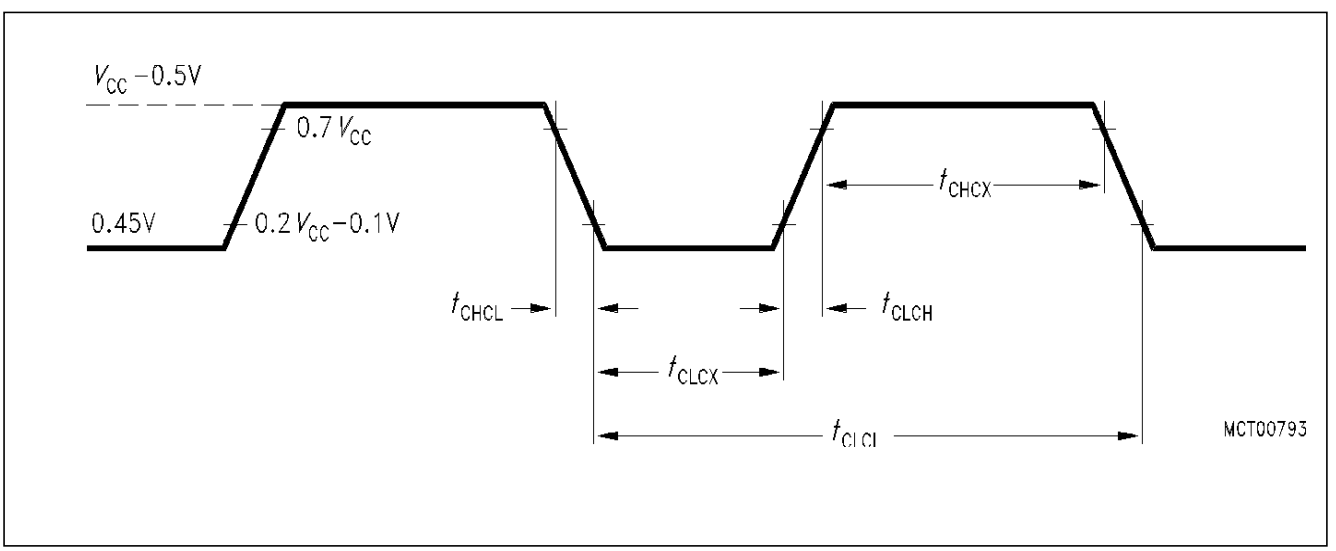
Data Memory Read Cycle



Data Memory Write Cycle

AC Characteristics (cont'd)

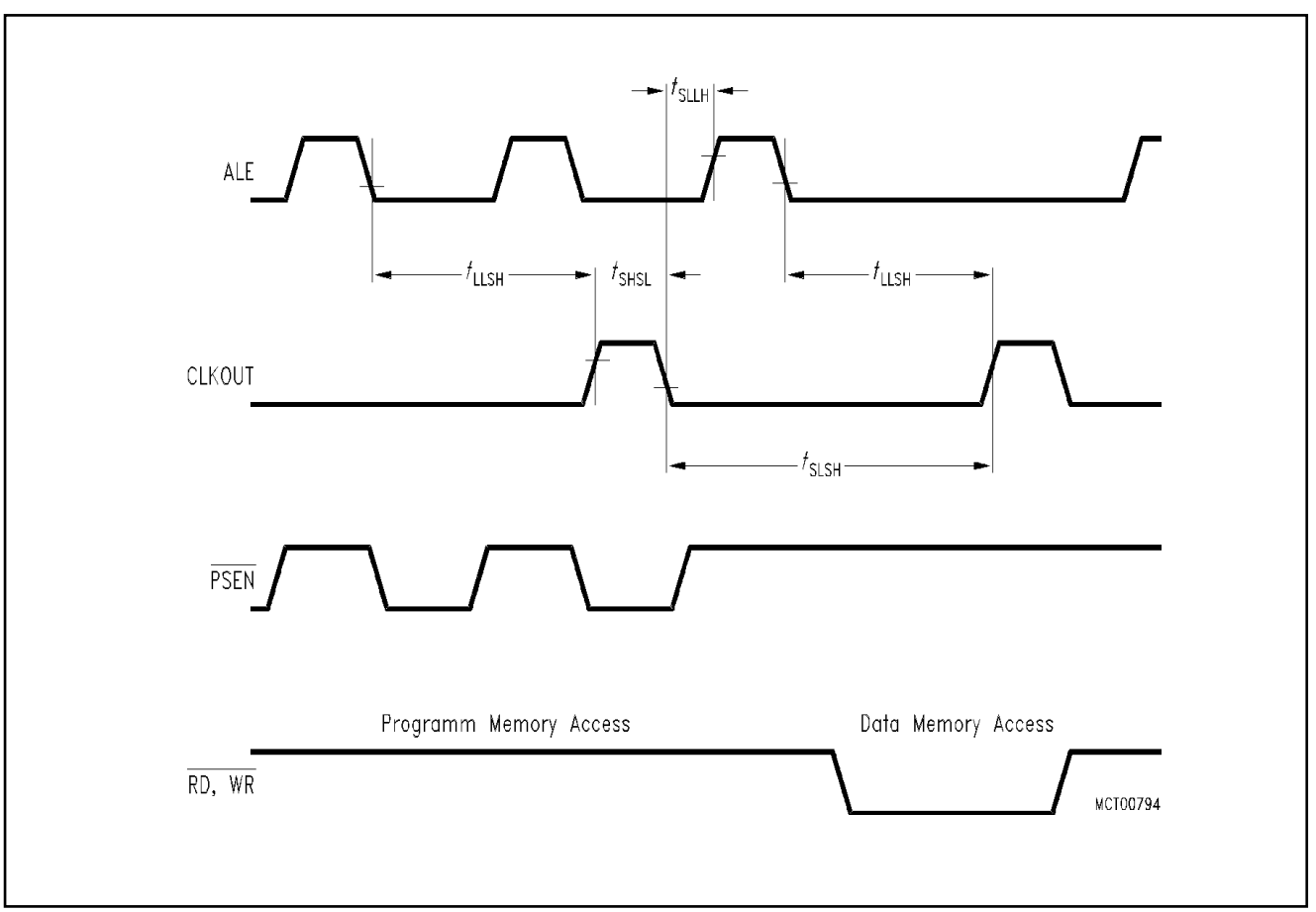
Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 3.5 MHz to 18 MHz		
		min.	max.	
External Clock Drive				
Oscillator period	t_{CLCL}	55.6	285	ns
High time	t_{CHCX}	20	t_{CLCL}-t_{CHCX}	ns
Low time	t_{CLCX}	20	t_{CLCL}-t_{CHCX}	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns
Oscillator frequency	$1/t_{CLC}$	3.5	18	MHz



External Clock Cycle

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		18 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 18 MHz		
		min.	max.	min.	max.	
System Clock Timing						
ALE to CLKOUT	t_{LLSH}	349	–	7 t_{CLCL} – 40	–	ns
CLKOUT high time	t_{SHSL}	71	–	2 t_{CLCL} – 40	–	ns
CLKOUT low time	t_{SLSH}	516	–	10 t_{CLCL} – 40	–	ns
CLKOUT low to ALE high	t_{SLLH}	16	96	t_{CLCL} – 40	t_{CLCL} +40	ns



System Clock Timing

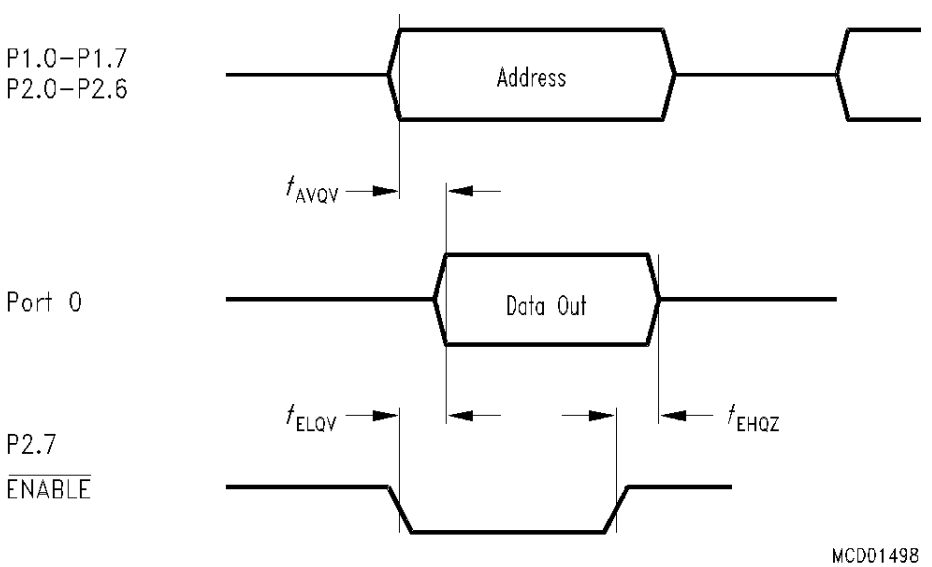
ROM Verification Characteristics

T_A = 25°C ± 5°C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Parameter	Symbol	Limit values		Unit
		min.	max.	

ROM Verification Mode 1 (Standard Verify Mode for not Read Protected ROM)

Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns
ENABLE to valid data	t_{ELQV}	–	48 t_{CLCL}	ns
Data float after ENABLE	t_{EHOZ}	0	48 t_{CLCL}	ns
Oscillator frequency	1/t_{CLCL}	4	6	MHz

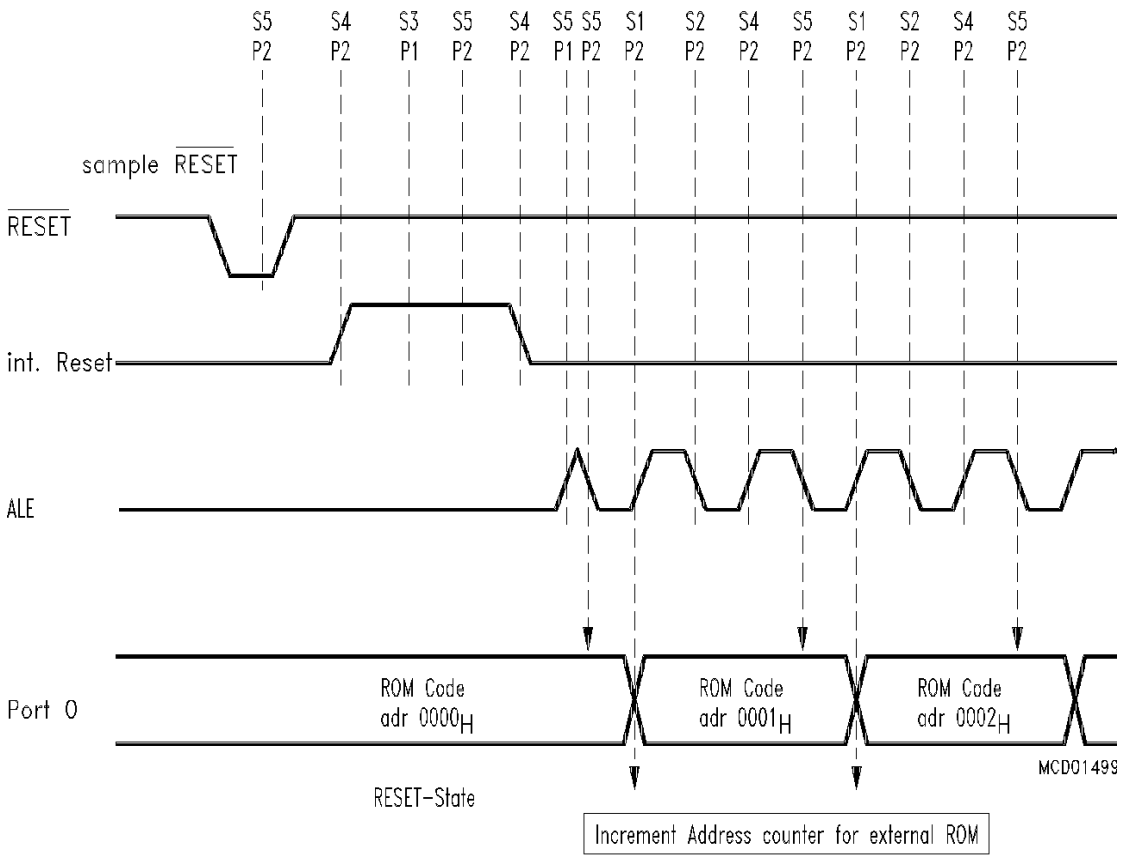


Address: P1.0–P1.7=A0–A7
P2.0–P2.6=A8–A14
Data: P0.0–0.7=D0–D7

Inputs $\overline{PSEN}$ = V_{SS}
ALE,$\overline{EA}$ = V_{IH}
$\overline{RESET}$ = V_{II}

ROM Verification Mode 1

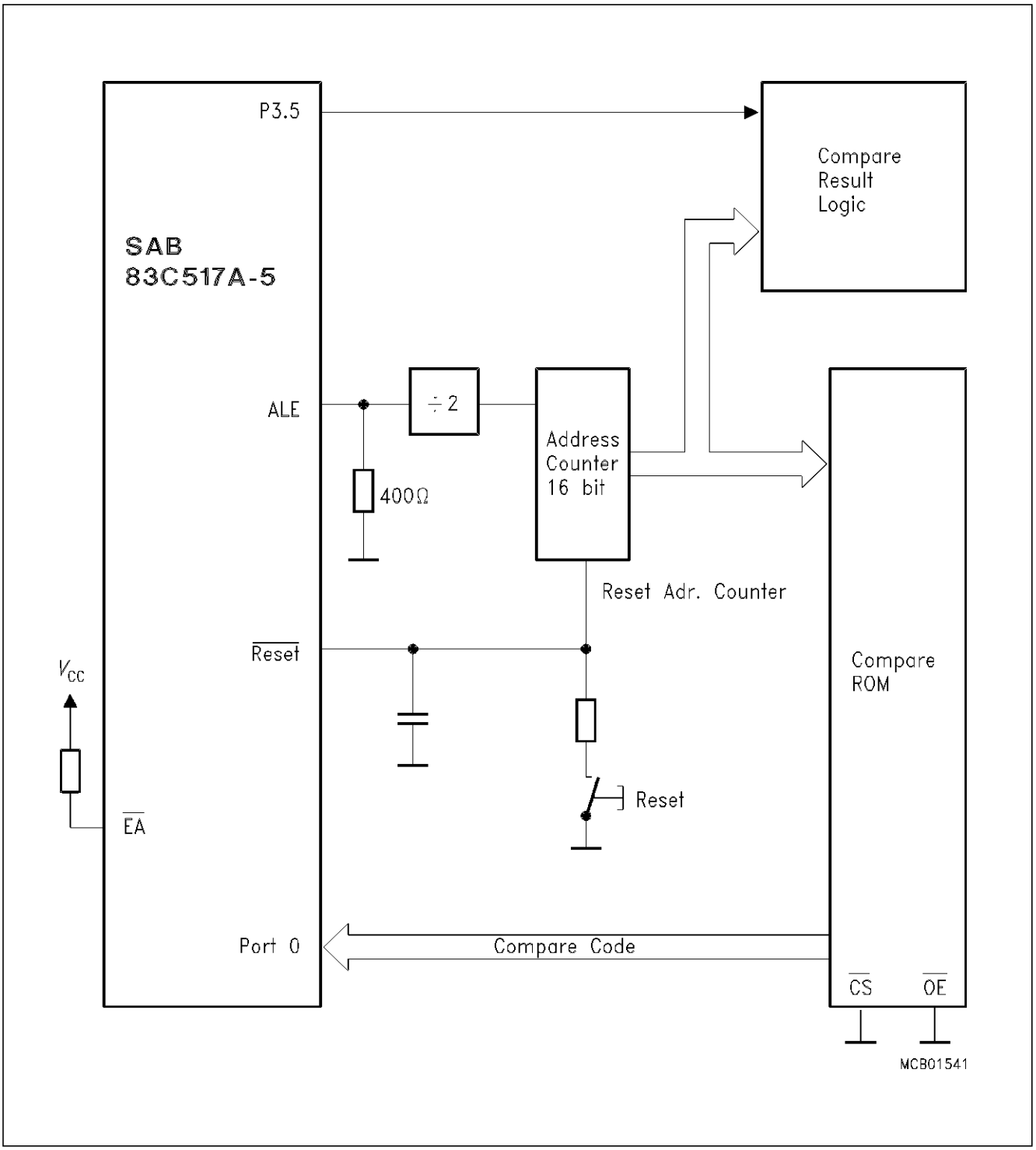
ROM Verification Mode 2 (New Verify Mode for Protected and not Protected ROM)



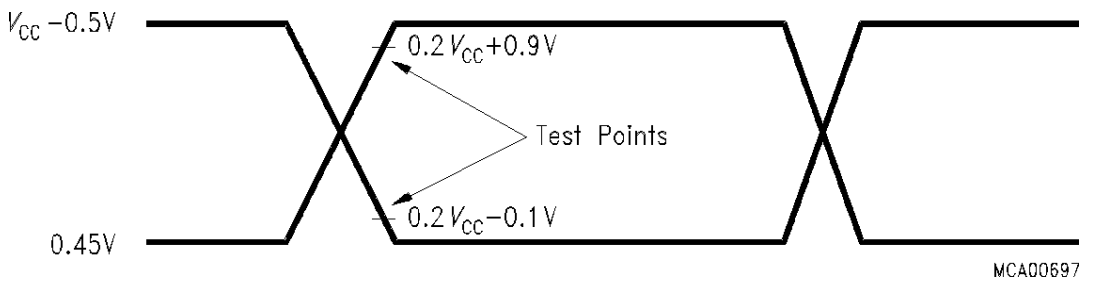
Inputs $\overline{EA}= V_{IH}$
ALE forced to low level by a weak pull down resistor (approx.400Ω),
during $\overline{RESET}$ activ ROM-Code: Port 0=D0-D7

Outputs Port 3.5 shows all 1024 cycles low level for one cycle
when compared ROM-Code was not alright

ROM Verification Mode 2

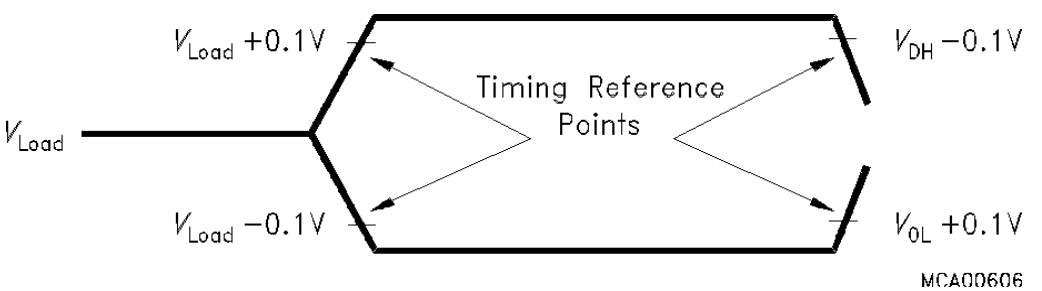


Application Circuitry for Verifying the Internal ROM



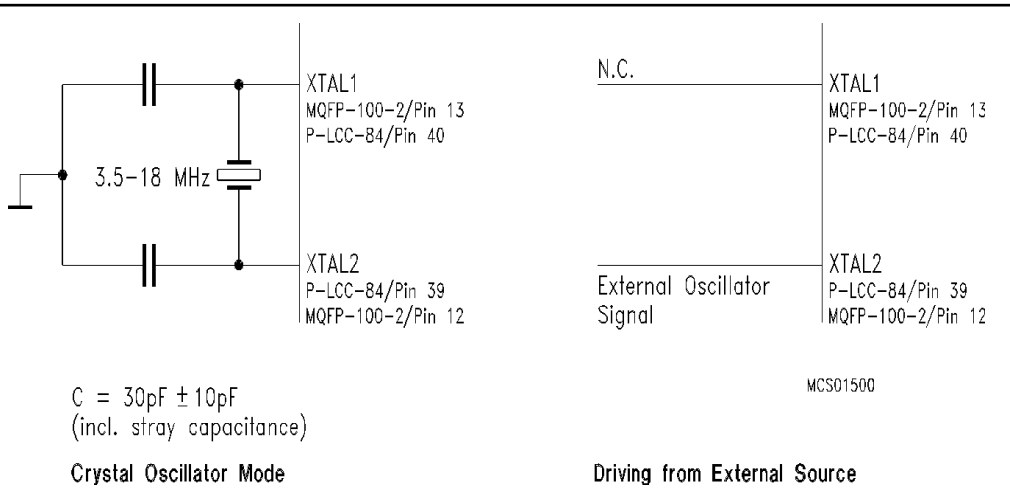
AC Inputs during testing are driven at V_{CC} - 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

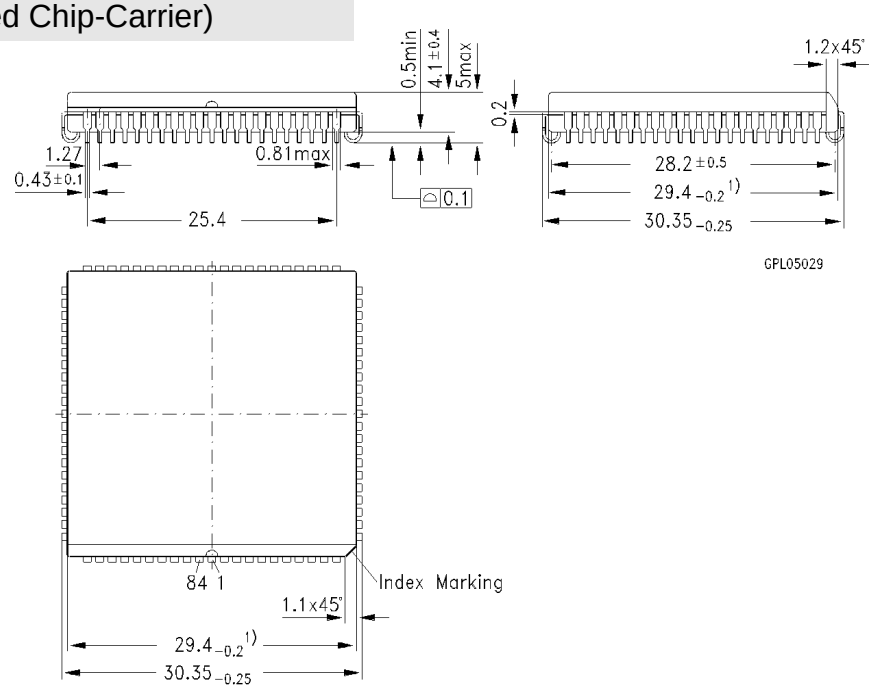
AC Testing: Float Waveforms



Recommended Oscillator Circuits

Package Outlines

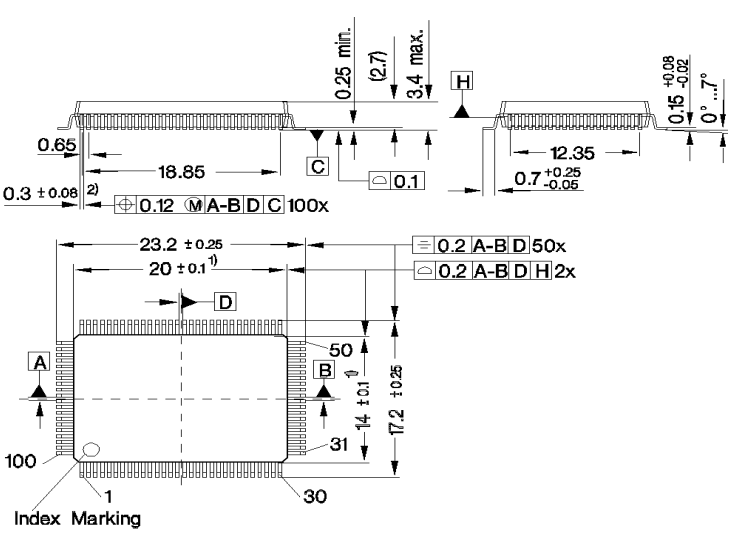
Plastic Package, P-LCC-84 – SMD
(Plastic Leaded Chip-Carrier)



1) Does not include plastic or metal protrusions of 0.15max per side

Dimensions in mm

Plastic Package, P-MQFP-100-2 – SMD
(Plastic Metric Rectangular Flat Package)



2) Does not include dambar protrusion of 0.08 max. per side
1) Does not include plastic or metal protrusion of 0.25 max. per side

Dimensions in mm

SMD = Surface Mounted Device

SIEMENS

High-Performance 8-Bit CMOS Single-Chip Microcontroller

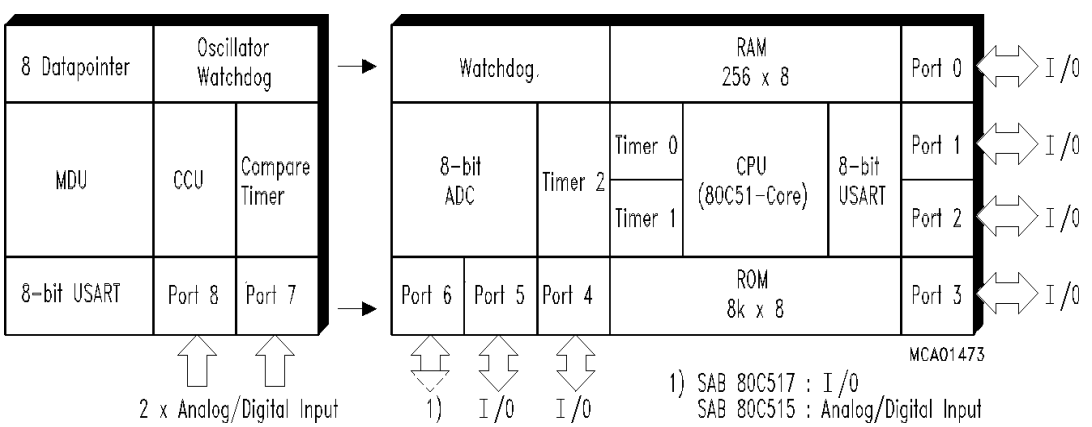
SAB 80C517/80C537

Advanced Information

SAB 80C517	Microcontroller with factory mask-programmable ROM
SAB 80C537	Microcontroller for external ROM

- Versions for 12 MHz and 16 MHz operating frequency
- 8 K × 8 ROM (SAB 80C517 only)
- 256 × 8 on-chip RAM
- Superset of SAB 80C51 architecture:
  1 µs instruction cycle time at 12 MHz
  750 ns instruction cycle time at 16 MHz
  256 directly addressable bits
  Boolean processor
  64 Kbyte external data and program memory addressing
- Four 16-bit timer/counters
- Powerful 16-bit compare/capture unit (CCU) with up to 21 high-speed or PWM output
  channels and 5 capture inputs
- Versatile "fail-safe" provisions
- Fast 32-bit division, 16-bit 2 multiplication, 32-bit normalize and shift by peripheral MUL/DIV unit (MDU)
- Eight data pointers for external memory addressing
- Fourteen interrupt vectors, four priority levels selectable
- 8-bit A/D converter with 12 multiplexed inputs and programmable ref. voltages
- Two full duplex serial interfaces
- Fully upward compatible with SAB 80C515
- Extended power saving modes
- Nine ports: 56 I/O lines, 12 input lines
- Three temperature ranges available:
  0 to 70 °C
  – 40 to 85 °C
- Plastic packages: P-LCC-84, P-MQFP-100-2

SAB 80C517/80C537

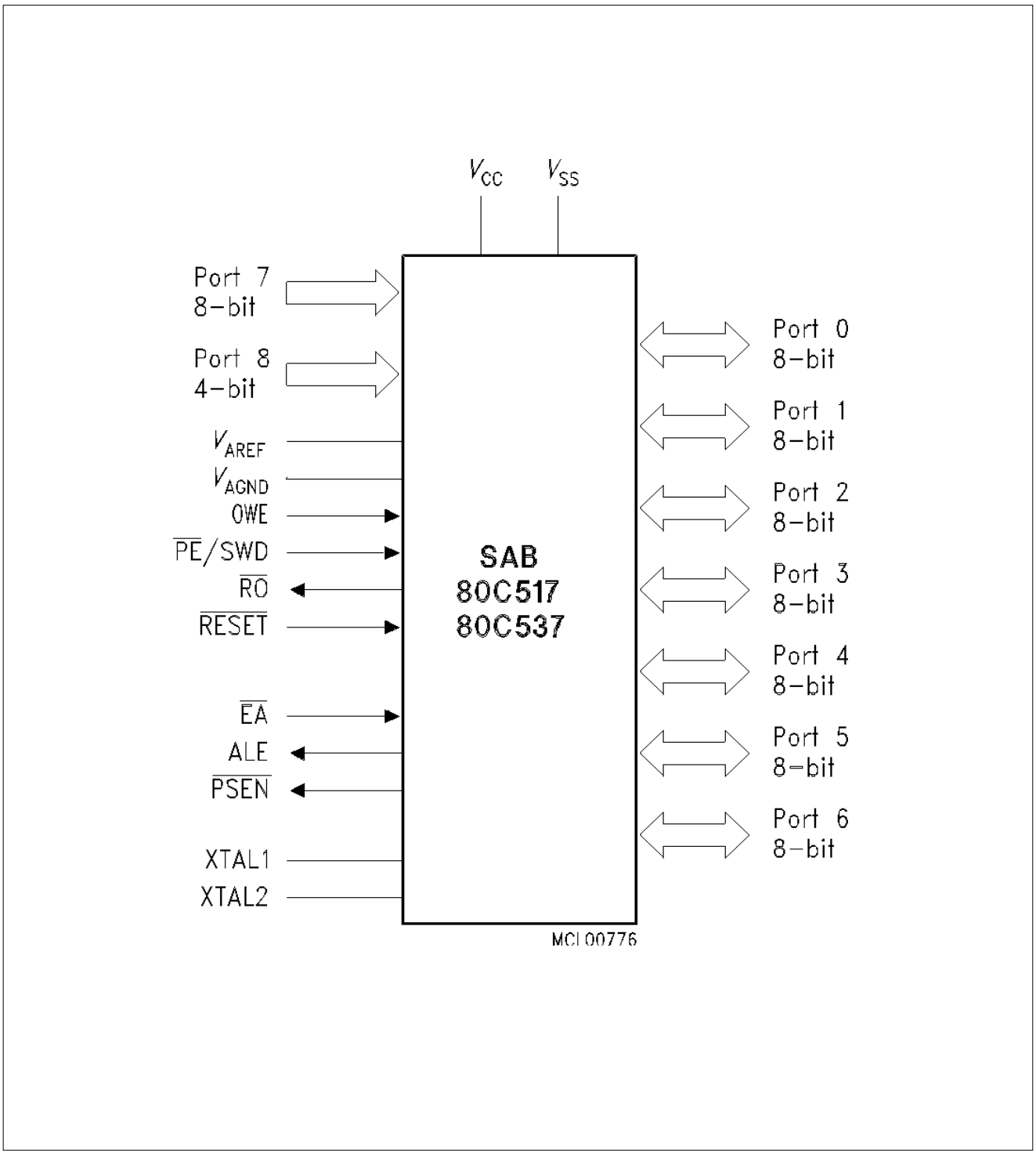


The SAB 80C517/80C537 is a high-end member of the Siemens SAB 8051 family of microcontrollers. It is designed in Siemens ACMOS technology and based on the SAB 8051 architecture. ACMOS is a technology which combines high-speed and density characteristics with low-power consumption or dissipation.

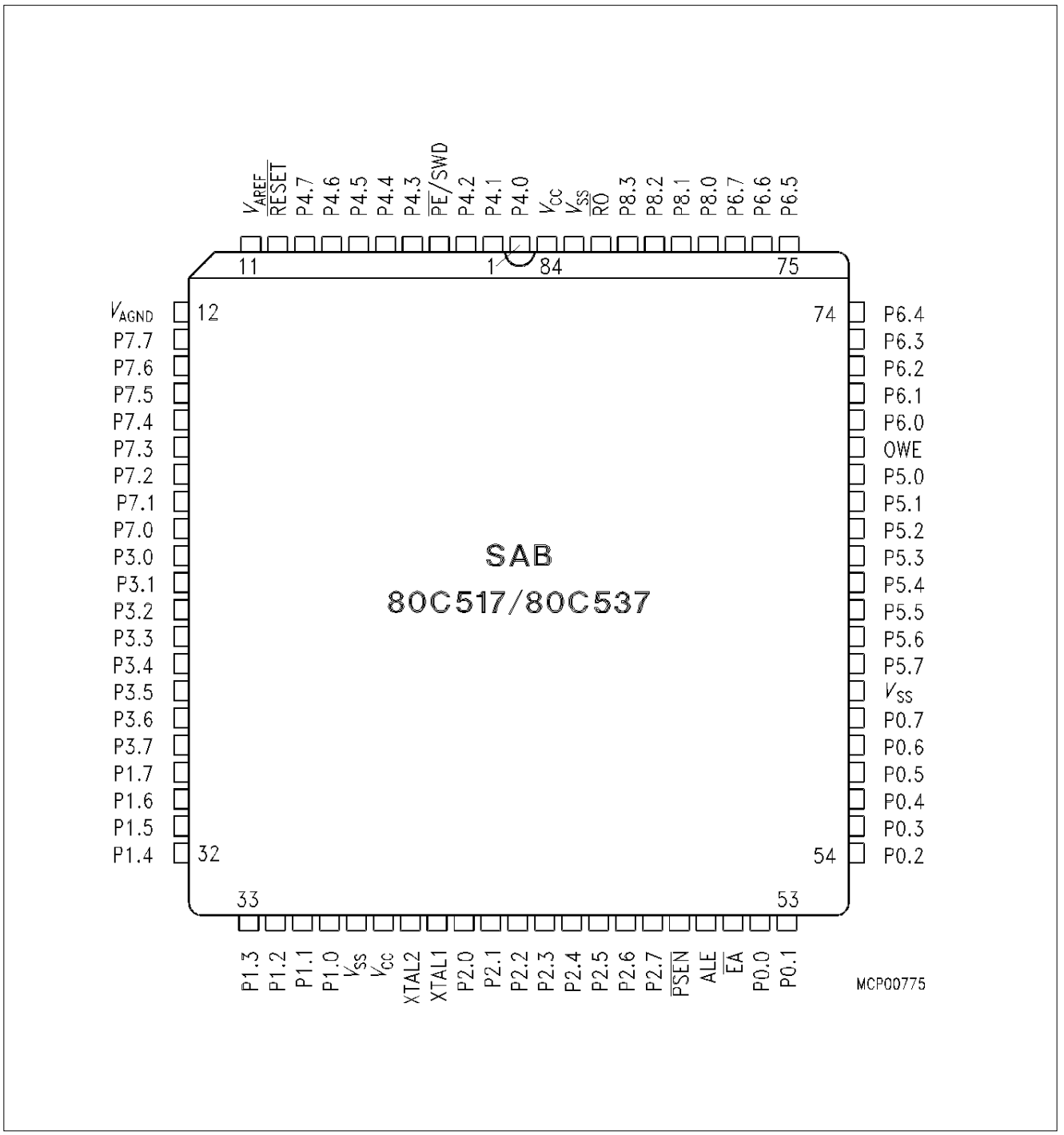
While maintaining all the SAB 80C515 features and operating characteristics the SAB 80C517 is expanded in its arithmetic capabilities, "fail-safe" characteristics, analog signal processing and timer capabilities. The SAB 80C537 is identical with the SAB 80C517 except that it lacks the on-chip program memory. The SAB 80C517/SAB 80C537 is supplied in a 84 pin plastic leaded chip carrier package (P-LCC-84) and in a 100-pin plastic quad metric flat package (P-MQFP-100-2).

Ordering Information

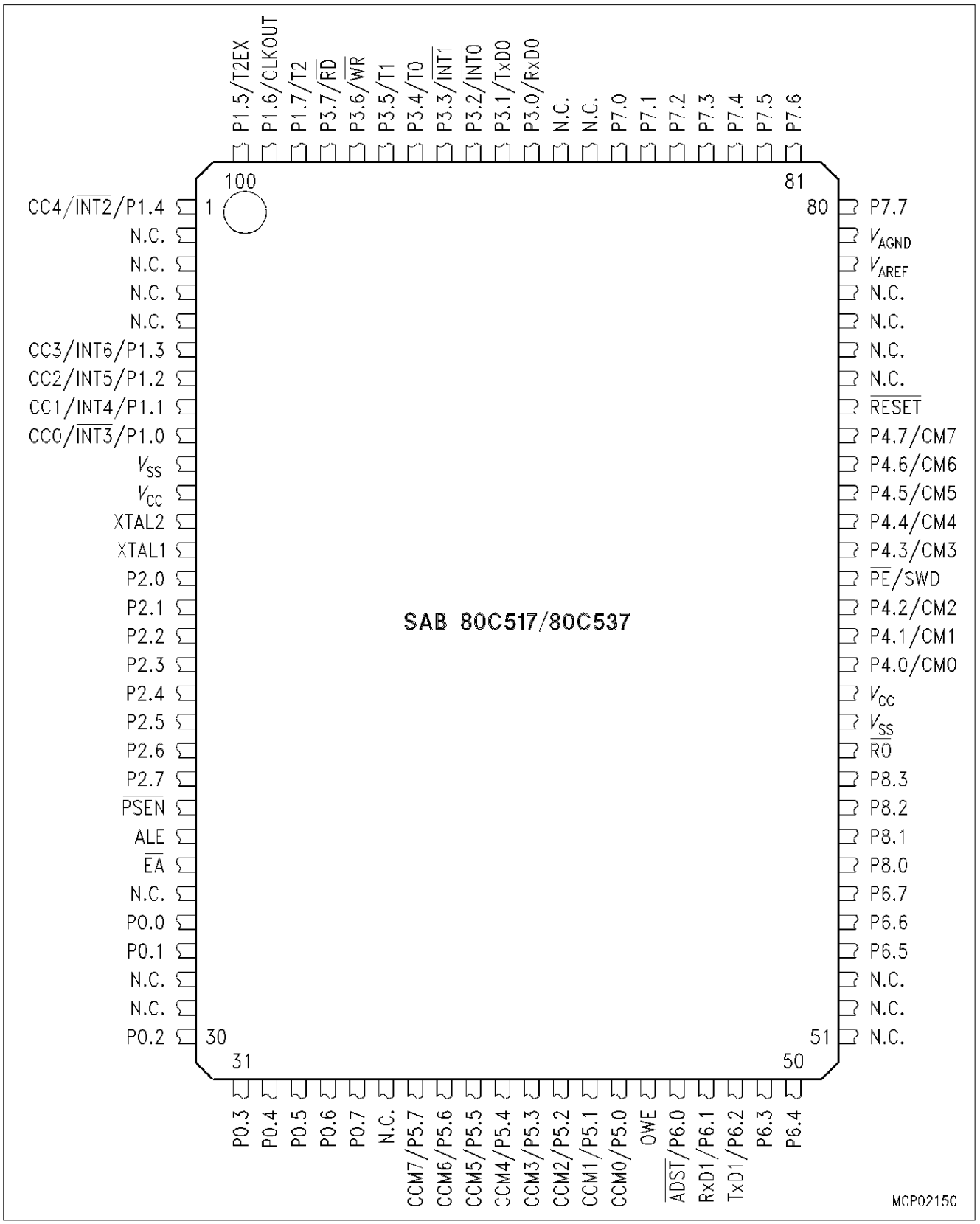
Type	Ordering code	Package	Description 8-bit CMOS microcontroller
SAB 80C517-N	Q67120-C397	P-LCC-84	with factory mask-programmable ROM,12 MHz
SAB 80C517-M	TBD	P-MQFP-100-2	
SAB 80C537-N	Q67120-C452	P-LCC-84	for external memory, 12 MHz
SAB 80C537-M	TBD	P-MQFP-100-2	
SAB 80C517-N-T40/85	Q67120-C483	P-LCC-84	with factory mask-programmable ROM, 12 MHz, ext. temperature – 40 to 85 ^{o}C
SAB 80C517-M-T40/85	TBD	P-MQFP-100-2	
SAB 80C537-N-T40/85	Q67120-C484	P-LCC-84	for external ROM, 12 MHz, ext. temperature – 40 to 85 ^{o}C
SAB 80C537-M-T40/85	TBD	P-MQFP-100-2	
SAB 80C517-N16	Q67120-C723	P-LCC-84	with mask-programmable ROM,16 MHz ext. temperature – 40 to 110 ^{o}C
SAB 80C517-M16	TBD	P-MQFP-100-2	
SAB 80C537-N16	Q67120-C722	P-LCC-84	for external memory, 16 MHz
SAB 80C537-M16	TBD	P-MQFP-100-2	
SAB 80C517-N16-T40/85	Q67120-C724	P-LCC-84	with mask-programmable ROM, 16 MHz ext. temperature – 40 to 85 ^{o}C
SAB 80C517-16-N-T40/85	Q67120-C725	P-LCC-84	with factory mask-programmable ROM,12 MHz



Logic Symbol



Pin Configuration
(P-LCC-84)



Pin Configuration
(P-MQFP-100-2)

Pin Definitions and Functions

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P4.0 – P4.7	1– 3, 5 – 9	64 - 66, 68 - 72	I/O	**Port 4** is a bidirectional I/O port with internal pull-up resistors. Port 4 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current ($I_{IL,}$ in the DC characteristics) because of the internal pull-up resistors. This port also serves alternate compare functions. The secondary functions are assigned to the pins of port 4 as follows: – CM0 (P4.0): Compare Channel 0 – CM1 (P4.1): Compare Channel 1 – CM2 (P4.2): Compare Channel 2 – CM3 (P4.3): Compare Channel 3 – CM4 (P4.4): Compare Channel 4 – CM5 (P4.5): Compare Channel 5 – CM6 (P4.6): Compare Channel 6 – CM7 (P4.7): Compare Channel 7
$\overline{PE}$/SWD	4	67	I	**$\overline{\text{Power saving modes enable}}$/Start Watchdog Timer** A low level on this pin allows the software to enter the power down, idle and slow down mode. In case the low level is also seen during reset, the watchdog timer function is off on default. Use of the software controlled power saving modes is blocked, when this pin is held on high level. A high level during reset performs an automatic start of the watchdog timer immediately after reset. When left unconnected this pin is pulled high by a weak internal pull-up resistor.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
$\overline{\text{RESET}}$	10	73	I	$\overline{\text{RESET}}$ A low level on this pin for the duration of one machine cycle while the oscillator is running resets the SAB 80C517. A small internal pull-up resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11	78		**Reference voltage** for the A/D converter.
V_{AGND}	12	79		**Reference ground** for the A/D converter.
P7.7 -P7.0	13 - 20	80 - 87	I	**Port 7** is an 8-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high/low voltages, and for the lower 8-bit of the multiplexed analog inputs of the A/D converter, simultaneously.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P3.0 - P3.7	21 - 28	90 - 97	I/O	**Port 3** is a bidirectional I/O port with internal pull-up resistors. Port 3 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current ($I_{IL,}$ in the DC characteristics) because of the internal pull-up resistors. Port 3 also contains the interrupt, timer, serial port 0 and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – R × D0 (P3.0): receiver data input (asynchronous) or data input/output (synchronous) of serial interface – T × D0 (P3.1): transmitter data output (asynchronous) or clock output (synchronous) of serial interface 0 – $\overline{INT0}$ (P3.2): $\overline{\text{interrupt 0 input}}$/timer 0 gate control – $\overline{INT1}$ (P3.3): $\overline{\text{interrupt 1 input}}$/timer 1 gate control – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{WR}$ (P3.6): the $\overline{\text{write control signal}}$ latches the data byte from port 0 into the external data memory – $\overline{RD}$ (P3.7): the $\overline{\text{read control signal}}$ enables the external data memory to port 0

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P1.7 - P1.0	29 - 36	98 - 100, 1, 6 - 9	I/O	**Port 1** is a bidirectional I/O port with inter-nal pull-up resistors. Port 1 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC character-istics) because of the internal pull-up resistors. It is used for the low order address byte during program verifi-cation. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows: – $\overline{\text{INT3}}$/CC0 (P1.0): $\overline{\text{interrupt 3 input}}$/ compare 0 output / capture 0 input – INT4/CC1 (P1.1): interrupt 4 input / compare 1 output /capture 1 input – INT5/CC2 (P1.2): interrupt 5 input / compare 2 output /capture 2 input – INT6/CC3 (P1.3): interrupt 6 input / compare 3 output /capture 3 input – $\overline{\text{INT2}}$/CC4 (P1.4): $\overline{\text{interrupt 2 input}}$ / compare 4 output /capture 4 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
XTAL2	39	12	–	**XTAL2** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL1	40	13	–	**XTAL1** Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is devided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.
P2.0 - P2.7	41 - 48	14 - 21	I/O	**Port 2** is a bidirectional I/O port with internal pull-up resistors. Port 2 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as in-puts. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pull-up resistors when issuing1 s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
$\overline{\text{PSEN}}$	49	22	O	The **Program Store Enable** output is a control signal that en-ables the external program memory to the bus during external fetch operations. It is activated every six oscillator periodes except during external data memory accesses. Remains high during internal pro-gram execution.
ALE	50	23	O	The **Address Latch Enable** output is used for latching the address into external memory during normal operation. It is activated every six oscil-lator periodes except during an exter-nal data memory access
$\overline{\text{EA}}$	51	24	I	**External Access Enable** When held at high level, instructions are fetched from the internal ROM when the PC is less than 8192. When held at low level, the SAB 80C517 fet-ches all instructions from external pro-gram memory. For the SAB 80C537 this pin must be tied low
P0.0 - P0.7	52 - 59	26 - 27, 30 - 35	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1 s written to them float, and in that state can be used as high-impe-dance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-up resistors when issuing 1 s. Port 0 also out-puts the code bytes during program verifica-tion in the SAB 83C517. External pull-up resistors are required during program verification.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P5.7 - P5.0	61 - 68	37 - 44	I/O	**Port 5** is a bidirectional I/O port with internal pull-up resistors. Port 5 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. This port also serves the alternate function "Concurrent Compare". The secondary functions are assigned to the port 5 pins as follows: – CCM0 (P5.0): concurrent compare 0 – CCM1 (P5.1): concurrent compare 1 – CCM2 (P5.2): concurrent compare 2 – CCM3 (P5.3): concurrent compare 3 – CCM4(P5.4): concurrent compare 4 – CCM5 (P5.5): concurrent compare 5 – CCM6 (P5.6): concurrent compare 6 – CCM7(P5.7): concurrent compare 7
OWE	69	45	I	**Oscillator Watchdog Enable** A high level on this pin enables the oscillator watchdog. When left unconnected this pin is pulled high by a weak internal pull-up resistor. When held at low level the oscillator watchdog function is off.

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
P6.0 - P6.7	70 - 77	46 - 50, 54 - 56	I/O	**Port 6** is a bidirectional I/O port with internal pull-up resistors. Port 6 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 6 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 6 also contains the external A/D converter control pin and the transmit and receive pins for serial channel 1. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 6, as follows: – $\overline{ADST}$ (P6.0): external A/D converter start pin – R × D1 (P6.1): receiver data input of serial interface 1 – T × D1 (P6.2): transmitter data output of serial interface 1
P8.0 - P8.3	78 - 81	57 - 60	I	**Port 8** is a 4-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high/low voltages, and for the higher 4-bit of the multiplexed analog inputs of the A/D converter, simultaneously

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O *)	Function
	P-LCC-84	P-MQFP-100-2		
$\overline{RO}$	82	61	O	**$\overline{\text{Reset Output}}$** This pin outputs the internally synchronized reset request signal. This signal may be generated by an external hardware reset, a watchdog timer reset or an oscillator watch-dog reset. The reset output is active low.
V_{SS}	37,60, 83	10, 62	–	**Circuit ground potential**
V_{CC}	38,84	11, 63	–	**Supply Terminal** for all operating modes
N.C.	–	2 - 5, 25, 28 - 29, 36, 51 - 53, 74 - 77; 88 - 89	–	Not connected

* I = Input
O = Output

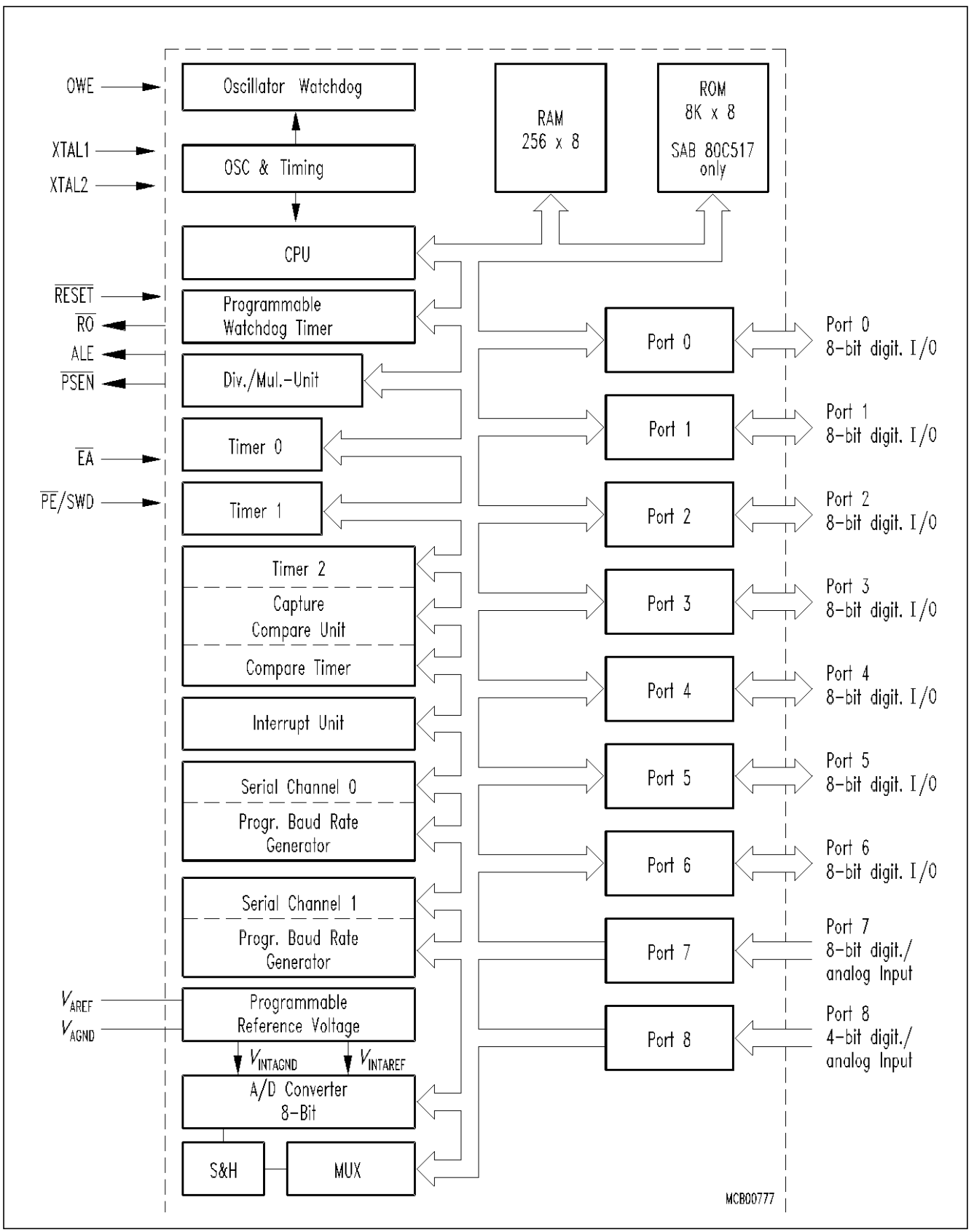


Figure 1
Block Diagram

Functional Description

The SAB 80C517 is based on 8051 architecture. It is a fully compatible member of the Siemens SAB 8051/80C51 microcontroller family being a significantly enhanced SAB 80C515. The SAB 80C517 is therefore 100 % compatible with code written for the SAB 80C515.

CPU

Having an 8-bit CPU with extensive facilities for bit-handling and binary BCD arithmetics the SAB 80C517 is optimized for control applications. With a 12 MHz crystal, 58 % of the instructions execute in 1 µs.

Being designed to close the performance gap to the 16-bit microcontroller world, the SAB 80C517's CPU is supported by a powerful 32-/16-bit arithmetic unit and a more flexible addressing of external memory by eight 16-bit datapointers.

Memory Organisation

According to the SAB 8051 architecture, the SAB 80C517 has separate address spaces for program and data memory. Figure 2 illustrates the mapping of address spaces.

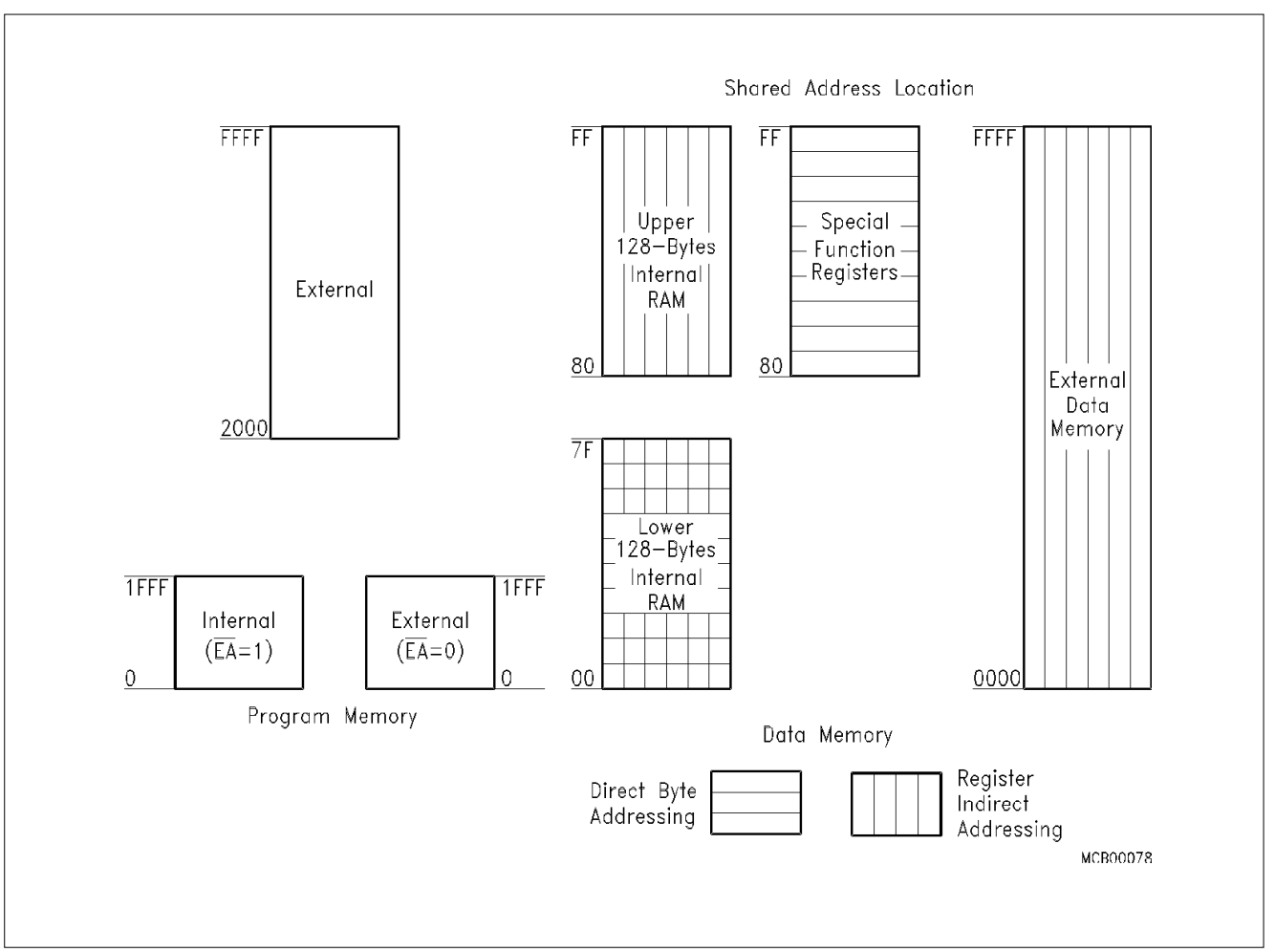


Figure 2
Memory Mapping

Program Memory

The SAB 80C517 has 8 KByte of on-chip ROM, while the SAB 80C537 has no internal ROM. The program memory can externally be expanded up to 64 Kbyte. Pin $\overline{EA}$ controls whether program fetches below address 2000H are done from internal or external memory.

Data Memory

The data memory space consists of an internal and an external memory space.

External Data Memory

Up to 64 KByte external data memory can be addressed by instructions that use 8-bit or 16-bit indirect addressing. For 8-bit addressing MOVX instructions utilizing registers R0 and R1 can be used. A 16-bit external memory addressing is supported by eight 16-bit datapointers.

Multiple Datapointers

As a functional enhancement to standard 8051 controllers, the SAB 80C517 contains eight 16-bit datapointers. The instruction set uses just one of these datapointers at a time. The selection of the actual datapointers is done in special function register DPSEL (data pointer select,
addr. 92H). Figure 3 illustrates the addressing mechanism.

Internal Data Memory

The internal data memory is divided into three physically distinct blocks:

– the lower 128 bytes of RAM including four banks of eight registers each

– the upper 128 byte of RAM

– the 128 byte special function register area.

A mapping of the internal data memory is also shown in figure 2. The overlapping address spaces are accessed by different addressing modes. The stack can be located anywhere in the internal data memory.

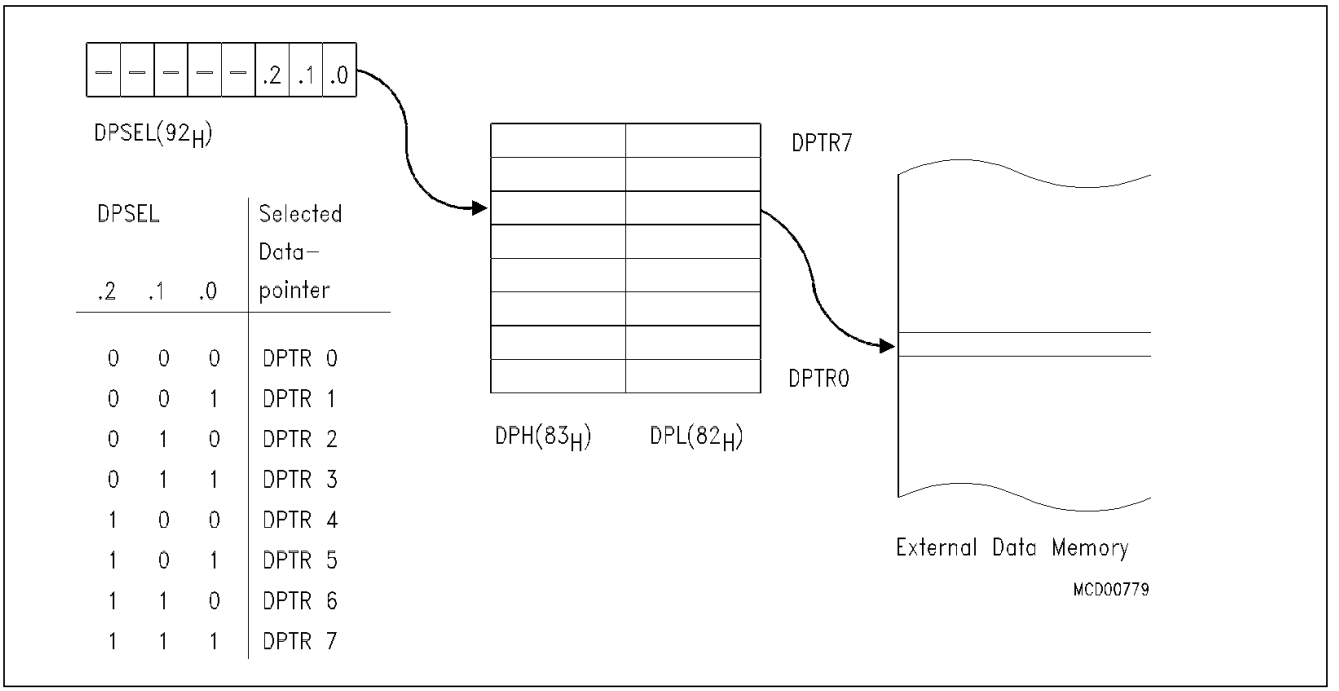


Figure 3
Addressing of External Data Memory

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area. The 81 special function registers include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripherals. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in table 1. In this table they are organized in groups which refer to the functional blocks of the SAB 80C517. Block names and symbols are listed in alphabetical order.

Table 1
Special Function Register

Address	Register	Name	Register	Contents after Reset
CPU	**ACC**	**Accumulator**	**0E0H** [1]	**00H**
	B	**B-Register**	**0F0H** [1]	**00H**
	DPH	Data Pointer, High Byte	83H	**00H**
	DPL	Data Pointer, Low Byte	82H	**00H**
	DPSEL	Data Pointer Select Register	92H	XXXX.X000B [3]
	PSW	**Program Status Word**	**0D0H** [1]	**00H**
	SP	**Register** Stack Pointer	81H	07H
A/D-Converter	**ADCON0**	**A/D Converter Control**	**0D8H** [1]	**00H**
	ADCON1	**Register 0**	0DCH	XXXX.0000B [3]
	ADDAT	A/D Converter Control Register 1	0D9H	00H
	DAPR	A/D Converter Data Register D/AConverter Program Register	0DAH	00H
Interrupt System	**IEN0**	**Interrupt Enable Register 0**	**0A8H** [1]	**00H**
	CTCON [2]	Com. Timer Control Register	0E1H	0XXX.0000B
	IEN1	**Interrupt Enable Register 1**	**0B8H** [1]	**00H**
	IEN2	Interrupt Enable Register 2	9AH	XXXX.00X0B [3]
	IP0	Interrupt Priority Register 0	0A9H	00H
	IP1	Interrupt Priority Register 1	0B9H	XX00 0000B
	IRCON	**Interrupt Request Control**	**0C0H** [1]	**00H**
	TCON [2]	**Register**	**88H** [1]	**00H**
	T2CON [2]	**Timer Control Register** **Timer 2 Control Register**	**0C8H**	**00H**

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

Table 1
Special Function Register (cont'd)

Address	Register	Name	Register	Contents after Reset
MUL/DIV Unit	ARCON	Arithmetic Control Register	0EFH	0XXX.XXXXB[3]
	MD0	Multiplication/Division	0E9H	XXH[3]
	MD1	Register 0	0EAH	XXH[3]
	MD2	Multiplication/Division	0EBH	XXH[3]
	MD3	Register 1	0ECH	XXH[3]
	MD4	Multiplication/Division R	0EDH	XXH[3]
	MD5	egister 2	0EEH	XXH[3]
		Multiplication/Division Register 3		
		Multiplication/Division Register 4		
		Multiplication/Division Register 5		

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) X means that the value is indeterminate and the location is reserved

Table 1
Special Function Register (cont'd)

Address	Register	Name	Register	Contents after Reset
Compare/ Capture- Unit (CCU)	CCEN	Comp./Capture Enable Reg.	0C1H	00H
	CC4EN	Comp./Capture Enable 4 Reg.	0C9H	X000.0000B[3]
	CCH1	Comp./Capture Reg. 1, High Byte	0C3H	00H
	CCH2	Comp./Capture Reg. 2, High Byte	0C5H	00H
	CCH3	Comp./Capture Reg. 3, High Byte	0C7H	00H
	CCH4	Comp./Capture Reg. 4, High Byte	0CFH	00H
	CCL1	Comp./Capture Reg. 1, Low Byte	0C2H	00H
	CCL2	Comp./Capture Reg. 2, Low Byte	0C4H	00H
	CCL3	Comp./Capture Reg. 3, Low Byte	0C6H	00H
	CCL4	Comp./Capture Reg. 4, Low Byte	0CEH	00H
	CMEN	Compare Enable Register	0F6H	00H
	CMH0	Compare Register 0, High Byte	0D3H	00H
	CMH1	Compare Register 1, High Byte	0D5H	00H
	CMH2	Compare Register 2, High Byte	0D7H	00H
	CMH3	Compare Register 3, High Byte	0E3H	00H
	CMH4	Compare Register 4, High Byte	0E5H	00H
	CMH5	Compare Register 5, High Byte	0E7H	00H
	CMH6	Compare Register 6, High Byte	0F3H	00H
	CMH7	Compare Register 7, High Byte	0F5H	00H
	CML0	Compare Register 0, Low Byte	0D2H	00H
	CML1	Compare Register 1, Low Byte	0D4H	00H
	CML2	Compare Register 2, Low Byte	0D6H	00H
	CML3	Compare Register 3, Low Byte	0E2H	00H
	CML4	Compare Register 4, Low Byte	0E4H	00H
	CML5	Compare Register 5, Low Byte	0E6H	00H
	CML6	Compare Register 6, Low Byte	0F2H	00H
	CML7	Compare Register 7, Low Byte	0F4H	00H
	CMSEL	Compare Input Select	0F7H	00H
	CRCH	Com./Rel./Capt. Reg. High Byte	0CBH	00H
	CRCL	Com./Rel./Capt. Reg. Low Byte	0CAH	00H
	CTCON	Com. Timer Control Reg.	0E1H	0XXX.0000B[3]
	CTRELH	Com. Timer Rel. Reg., High Byte	0DFH	00H
	CTRELL	Com. Timer Rel. Reg., Low Byte	0DEH	00H
	TH2	Timer 2, High Byte	0CDH	00H
	TL2	Timer 2, Low Byte	0CCH	00H
	T2CON	**Timer 2 Control Register**	**0C8H** [1]	**00H**

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) X means that the value is indeterminate and the location is reserved

Table 1
Special Function Register (cont'd)

Address	Register	Name	Register	Contents after Reset
Ports	**P0**	**Port 0**	**80H** [1]	**FFH**
	P1	**Port 1**	**90H** [1]	**FFH**
	P2	**Port 2**	**0A0H** [1]	**FFH**
	P3	**Port 3**	**0B0H** [1]	**FFH**
	P4	**Port 4**	**0E8H** [1]	**FFH**
	P5	**Port 5**	**0F8H** [1]	**FFH**
	P6	Port 6,	0FAH	FFH
	P7	Port 7, Analog/Digital Input	0DBH	XXH [3]
	P8	Port 8, Analog/Digital Input, 4-bit	0DDH	XXH [3]
Pow.Sav. Modes	PCON	Power Control Register	87H	00H
Serial Channels	**ADCON0** [2]	**A/D Converter Control Reg.**	**0D8H** [1]	**00H**
	PCON [2]	Power Control Register	87H	00H
	S0BUF	Serial Channel 0 Buffer Reg.	99H	XXH [3]
	S0CON	**Serial Channel 0 Control Reg**.	**98H** [1]	**00H**
	S1BUF	Serial Channel 1 Buffer Reg.,	9CH	0XXH [3]
	S1CON	Serial Channel 1 Control Reg.	9BH	0X00.000B [3]
	S1REL	Serial Channel 1 Reload Reg.	9DH	00H
Timer 0/ Timer 1	**TCON**	**Timer Control Register**	**88H** [1]	**00H**
	TH0	Timer 0, High Byte	8CH	00H
	TH1	Timer 1, High Byte	8DH	00H
	TL0	Timer 0, Low Byte	8AH	00H
	TL1	Timer 1, Low Byte	8BH	00H
	TMOD	Timer Mode Register	89H	00H
Watchdog	**IEN0** [2]	**Interrupt Enable Register 0**	**0A8H** [1]	**00H**
	IEN1 [2]	**Interrupt Enable Register 1**	**0B8H** [1]	**00H**
	IP0 [2]	Interrupt Priority Register 0	0A9H	00H
	IP1 [2]	Interrupt Priority Register 1	0B9H	XX00.0000B [3]
	WDTREL	Watchdog Timer Reload Reg.	86H	00H

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

A/D Converter

The SAB 80C517 contains an 8-bit A/D Converter with 12 multiplexed input channels which uses the successive approximation method. It takes 7 machine cycles to sample an analog signal (during this sample time the input signal should be held constant); the total conversion time (including sample time) is 13 machine cycles (13 µs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous; at the end of a conversion an interrupt can be generated.

A unique feature is the capability of internal reference voltage programming. The internal reference voltages V_{IntAREF} and V_{IntAGND} for the A/D converter are both programmable to one of 16 steps with respect to the external reference voltages. This feature permits a conversion with a smaller internal reference voltage range to gain a higher resolution. In addition, the internal reference voltages can easily be adapted by software to the desired analog input voltage range (see table 2).

Table 2
djustable Internal Reference Voltages

Step	DAPR (.3-.0) DAPR (.7-.4)	V_{IntAGND}	V_{IntAREF}
0	0000	0.0	5.0
1	0001	0.3125	–
2	0010	0.625	–
3	0011	0.9375	–
4	0100	1.25	1.25
5	0101	1.5625	1.5625
6	0110	1.875	1.875
7	0111	2.1875	2.1875
8	1000	2.5	2.5
9	1001	2.8125	2.8125
10	1010	3.125	3.125
11	1011	3.4375	3.4375
12	1100	3.75	3.75
13	1101	–	4.0625
14	1110	–	4.375
15	1111	–	4.68754

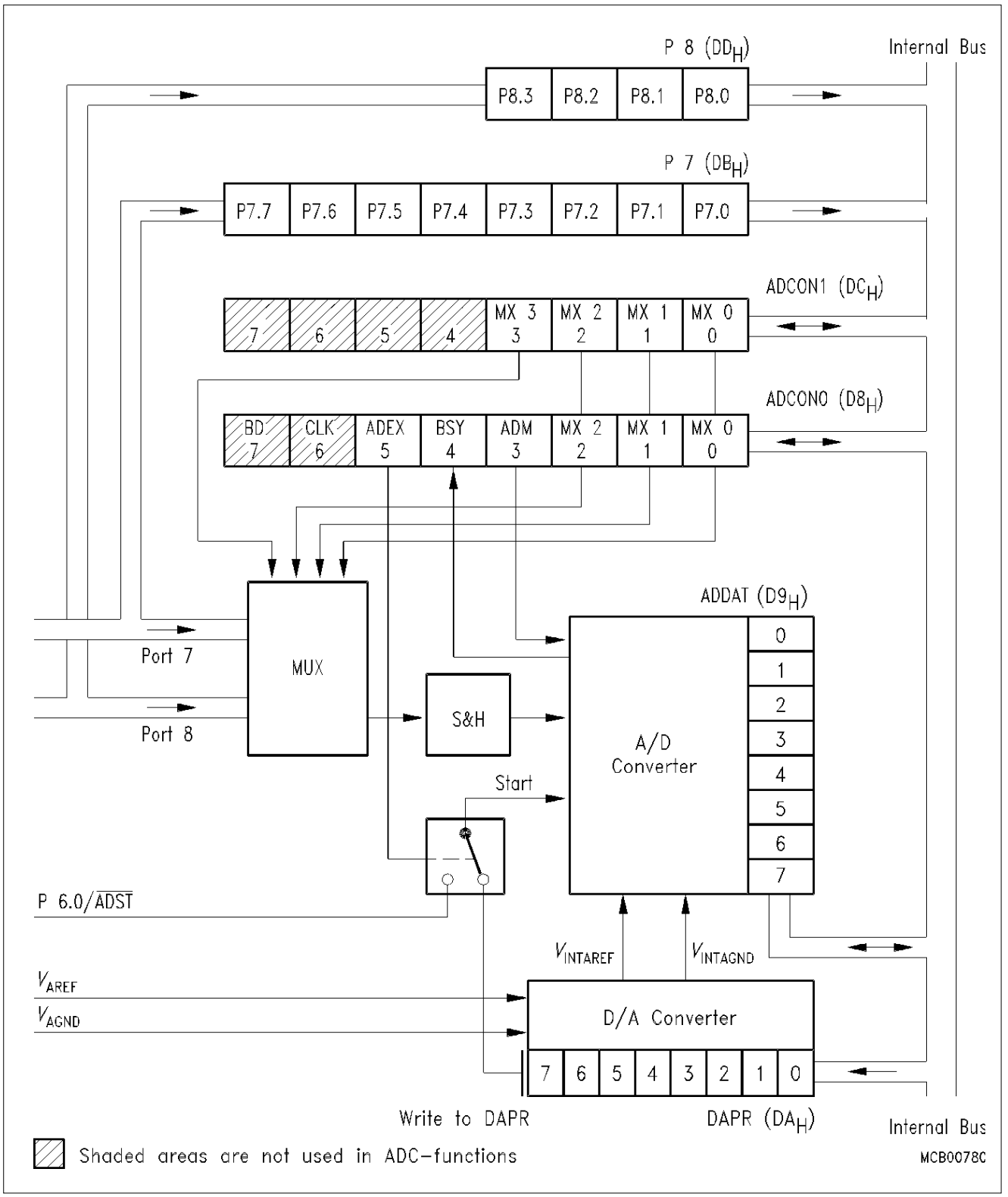


Figure 4
Block Diagram A/D Converter

Compare/Capture Unit (CCU)

The compare capture unit is a complex timer/register array for applications that require high speed I/O, pulse width modulation and more timer/counter capabilities. The CCU contains

- one 16-bit timer/counter **(timer 2)** with 2-bit prescaler, reload capability and a max.clock frequency of f_{OSC}/12 (1 MHz with a 12 MHz crystal).
- one 16-bit timer **(compare timer)** with 8-bit prescaler, reload capability and a max. clock frequency of f_{OSC}/2 (6 MHz with a 12 MHz crystal).
- thirteen 16-bit compare registers.
- five of which can be used as 16-bit capture registers.
- up to 21 output lines controlled by the CCU.
- seven interrupts which can be generated by CCU-events.

Figure 5 shows a block diagram of the CCU. Eight compare registers (CM0 to CM7) can individually be assigned to either timer 2 or the compare timer. Diagrams of the two timers are shown in figures 6 and 7. The four compare/capture registers and the compare/reload/capture register are always connected to timer 2. Dependent on the register type and the assigned timer two compare modes can be selected. Table 3 illustrates possible combinations and the corresponding output lines.

Table 3
CU Compare Configuration

Assigned Timer	DAPR (.3-.0) DAPR (.7-.4)	$V_{IntAGND}$	$V_{IntAREF}$
Timer 2	CRCH/CRCL	P1.0/$\overline{INT3}$/CC0	Comp. mode 0, 1 + Reload
	CC1H/CC1L	P1.1/INT4/CC1	Comp. mode 0, 1
	CC2H/CC2L	P1.2/INT5/CC2	Comp. mode 0, 1
	CC3H/CC3L	P1.3/INT6/CC3	Comp. mode 0, 1
	CC4H/CC4L	P1.4/$\overline{INT2}$/CC4	Comp. mode 0, 1
	CC4H/CC4L	P5.0/CCM0	Comp. mode 1
	:	:	:
	CC4H/CC4L	P5.7/CCM7	Comp. mode 1
	CM0H/CM0L	P4.0/CM0	Comp. mode 1
	:	:	:
	CM7H/CM7L	P4.7/CM7	Comp. mode 1
Compare timer	CM0H/CM0L	P4.0/CM0	Comp. mode 0 (with add. latches)
	:	:	:
	:	:	:
	CM7H/CM7L	P4.7/CM7	Comp. mode 0 (with add. latches)

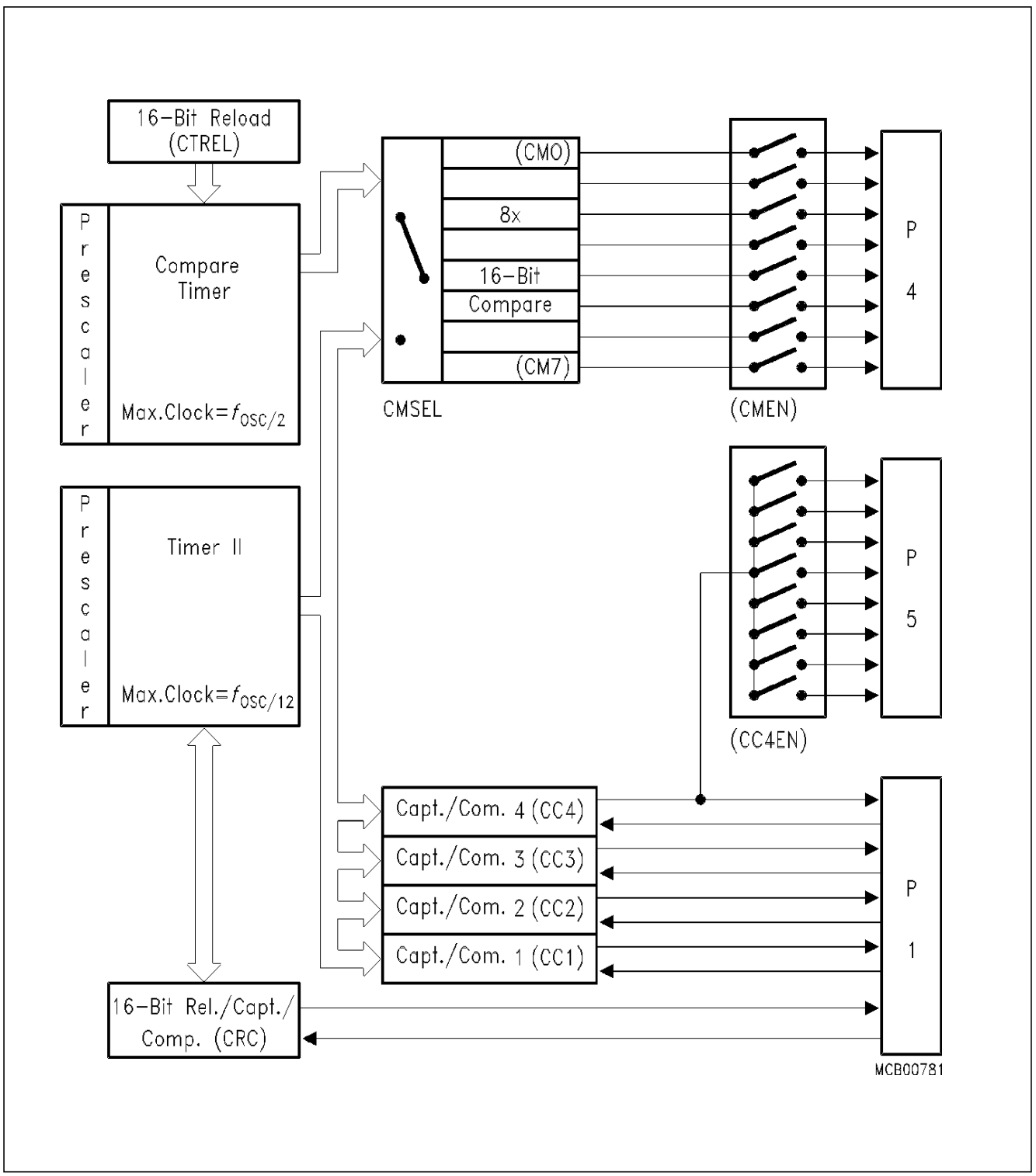


Figure 5
Block Diagram of the Compare/Capture Unit

Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 register or the compare timer register. If the count value in the timer registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to low level when the timer overflows.

Mode 1: The transition of the output signal can be determined by software. A timer overflow signal doesn't affect the compare-output.

Compare registers CM0 to CM7 use additional compare latches when operated in mode 0. Figure 8 shows the function of these latches. The latches are implemented to prevent from loss of compare matches which may occur when loading of the compare values is not correlated with the timer count. The compare latches are automatically loaded from the compare registers at every timer overflow.

Capture

This feature permits saving of the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value of timer 2 registers into a dedicated capture register.

Mode 0: Capture is performed in response to a transition at the corresponding port pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

Reload of Timer 2

A 16-bit reload can be performed with the 16-bit CRC register, which is a concatenation of the 8-bit registers CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which also can request an interrupt.

Timer/Counters 0 and 1

These timer/counters are fully compatible with timer/counter 0 or 1 of the SAB 8051 and can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer; timer/counter 1 in this mode holds its count.

External inputs $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

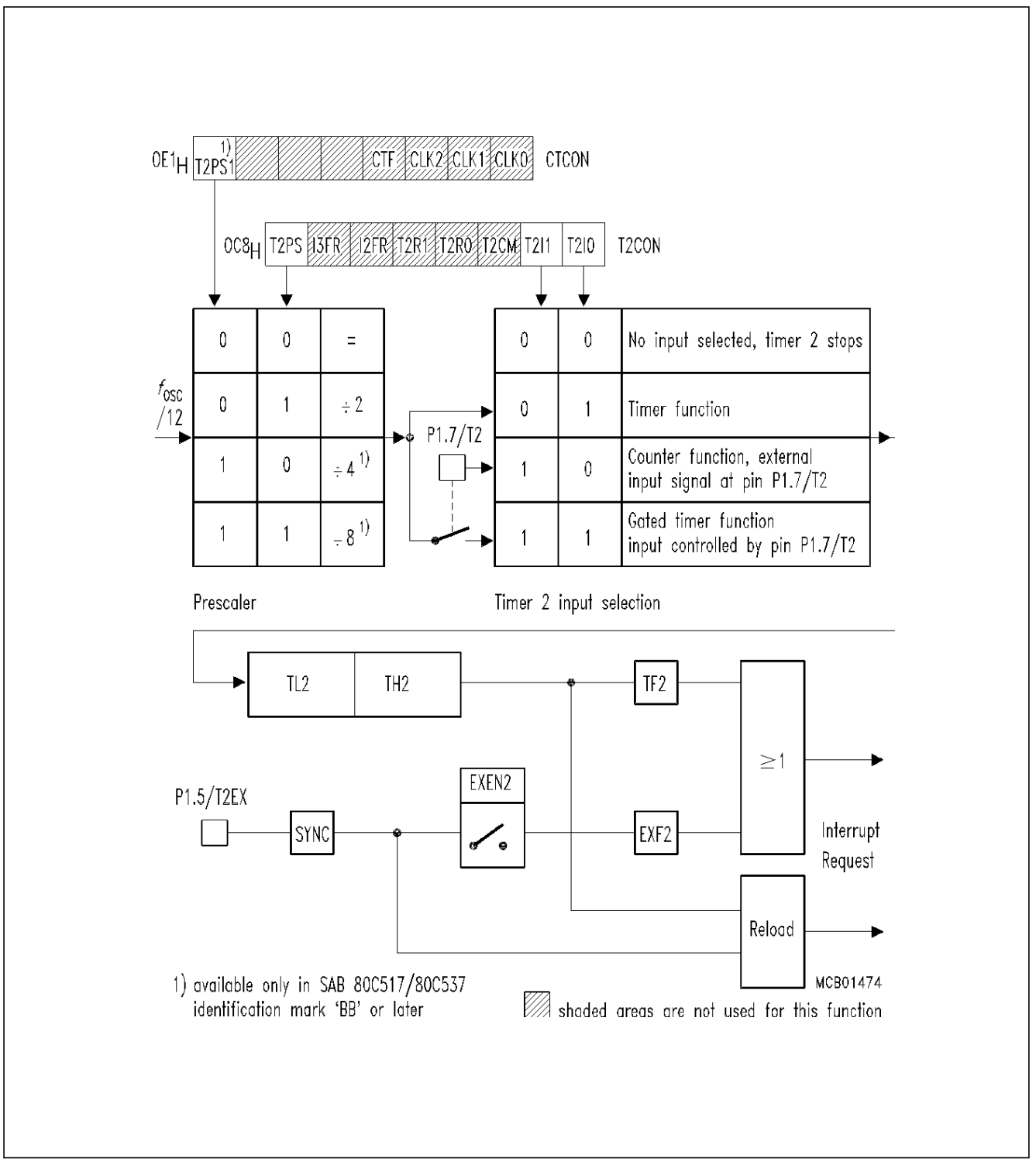


Figure 6
Block Diagram of Timer 2

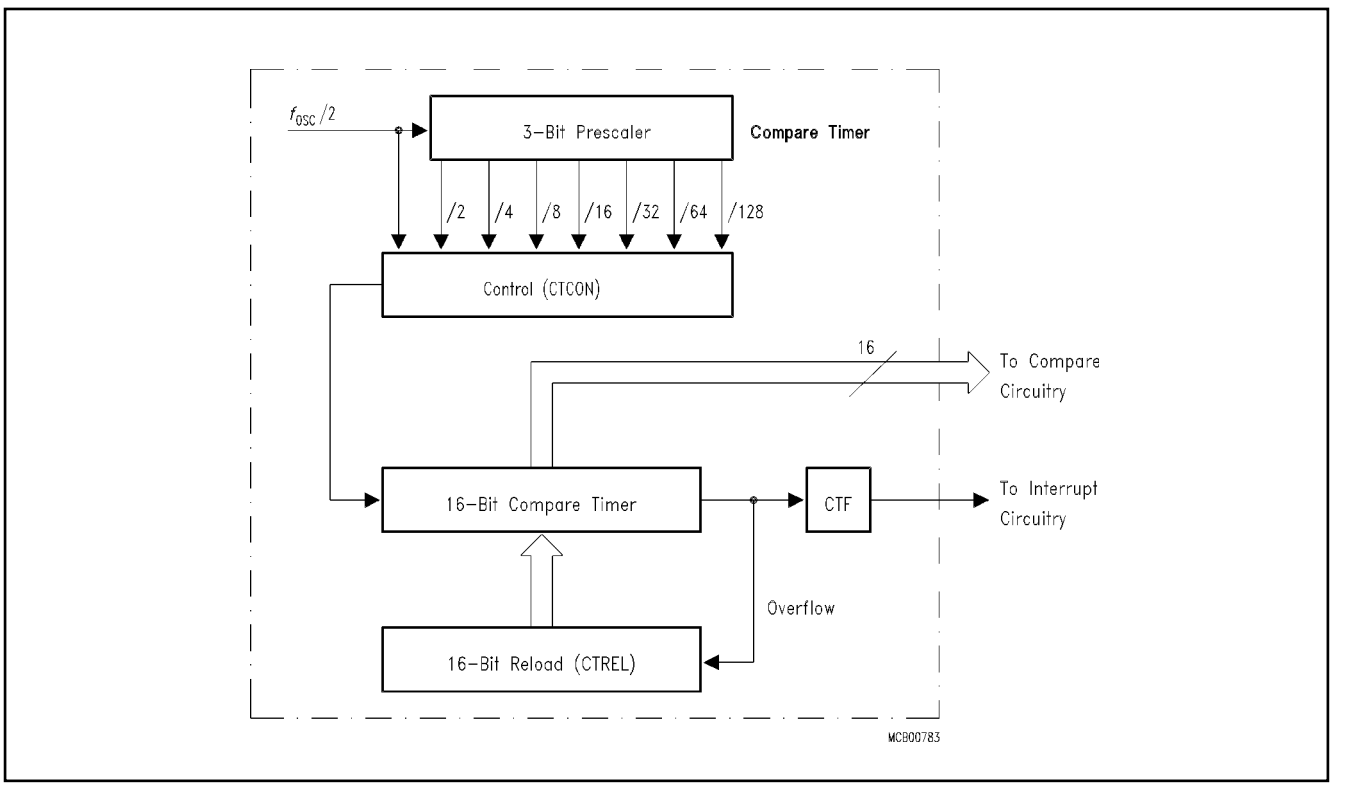


Figure 7
Block Diagram of the Compare Timer

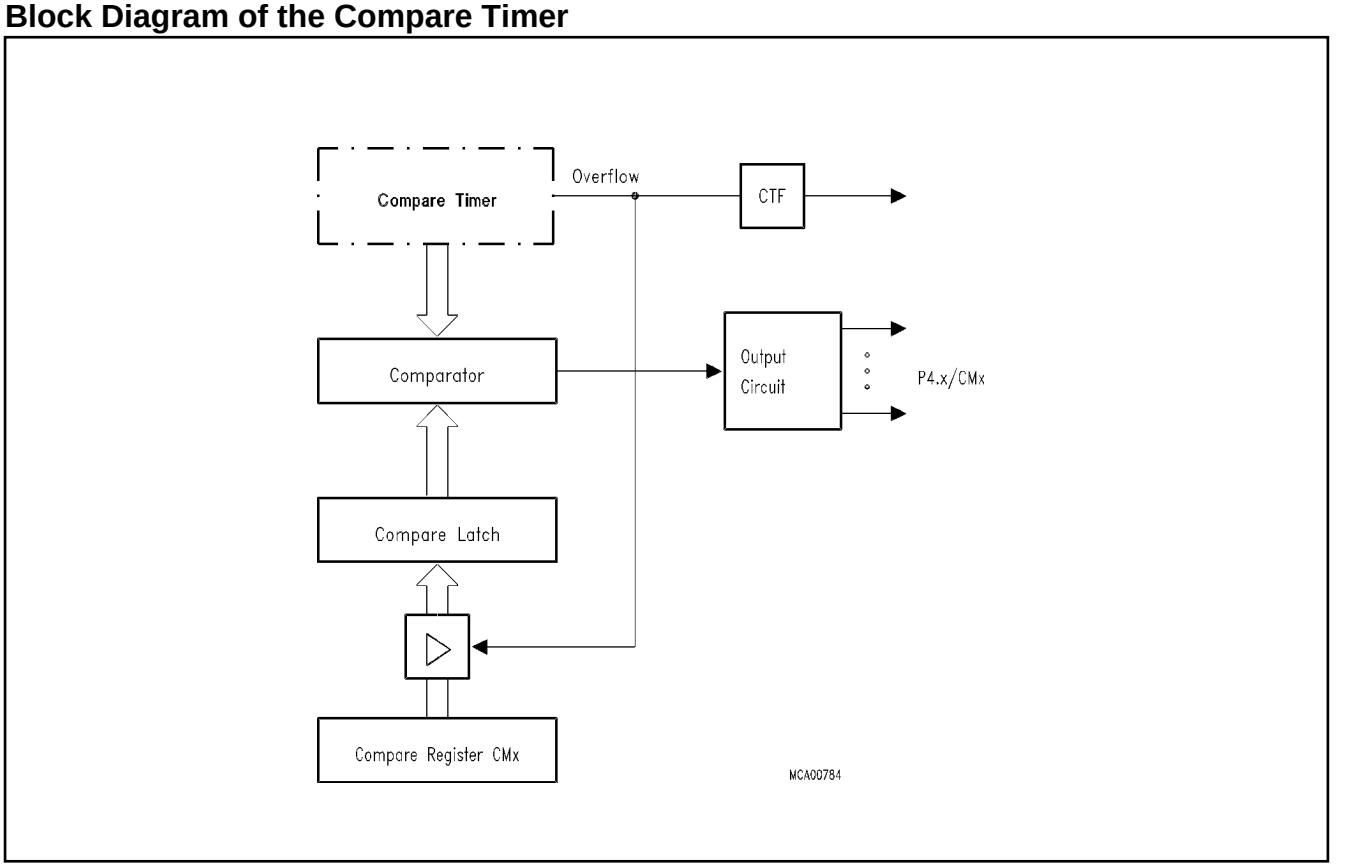


Figure 8
Compare-Mode 0 with Registers CM0 to CM7

Interrupt Structure

The SAB 80C517 has 14 interrupt vectors with the following vector addresses and request flags.

Table 4
Interrupt Sources and Vectors

Source (Request Flags)	Vector Address	Vector
IE0	0003H	External interrupt 0
TF0	000BH	Timer 0 overflow
IE1	0013H	External interrupt 1
TF1	001BH	Timer 1 overflow
RI0/TI0	0023H	Serial channel 0
TF2 + EXF2	002BH	Timer 2 overflow/ext. reload
IADC	0043H	A/D converter
IEX2	004BH	External interrupt 2
IEX3	0053H	External interrupt 3
IEX4	005BH	External interrupt 4
IEX5	0063H	External interrupt 5
IEX6	006BH	External interrupt 6
RI1/TI1	0083H	Serial channel 1
CTF	009BH	Compare timer overflow

Each interrupt vector can be individually enabled/disabled. The response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 2 to 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs or triples. Each pair or triple can be programmed individually to one of four priority levels by setting or clearing one bit in special function register IP0 and one in IP1. Figure 9 shows the interrupt request sources, the enabling and the priority level structure.

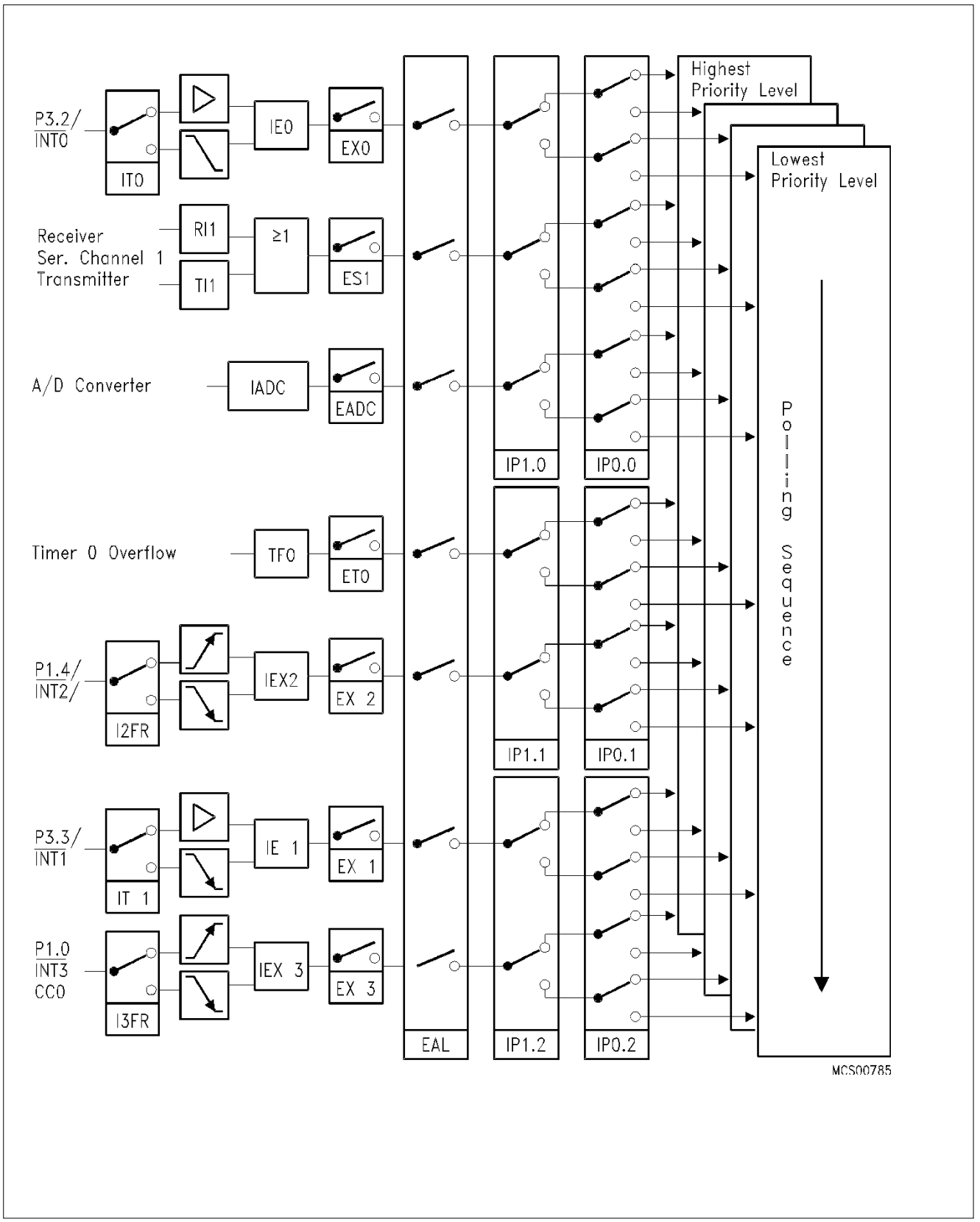


Figure 9
Interrupt Structure

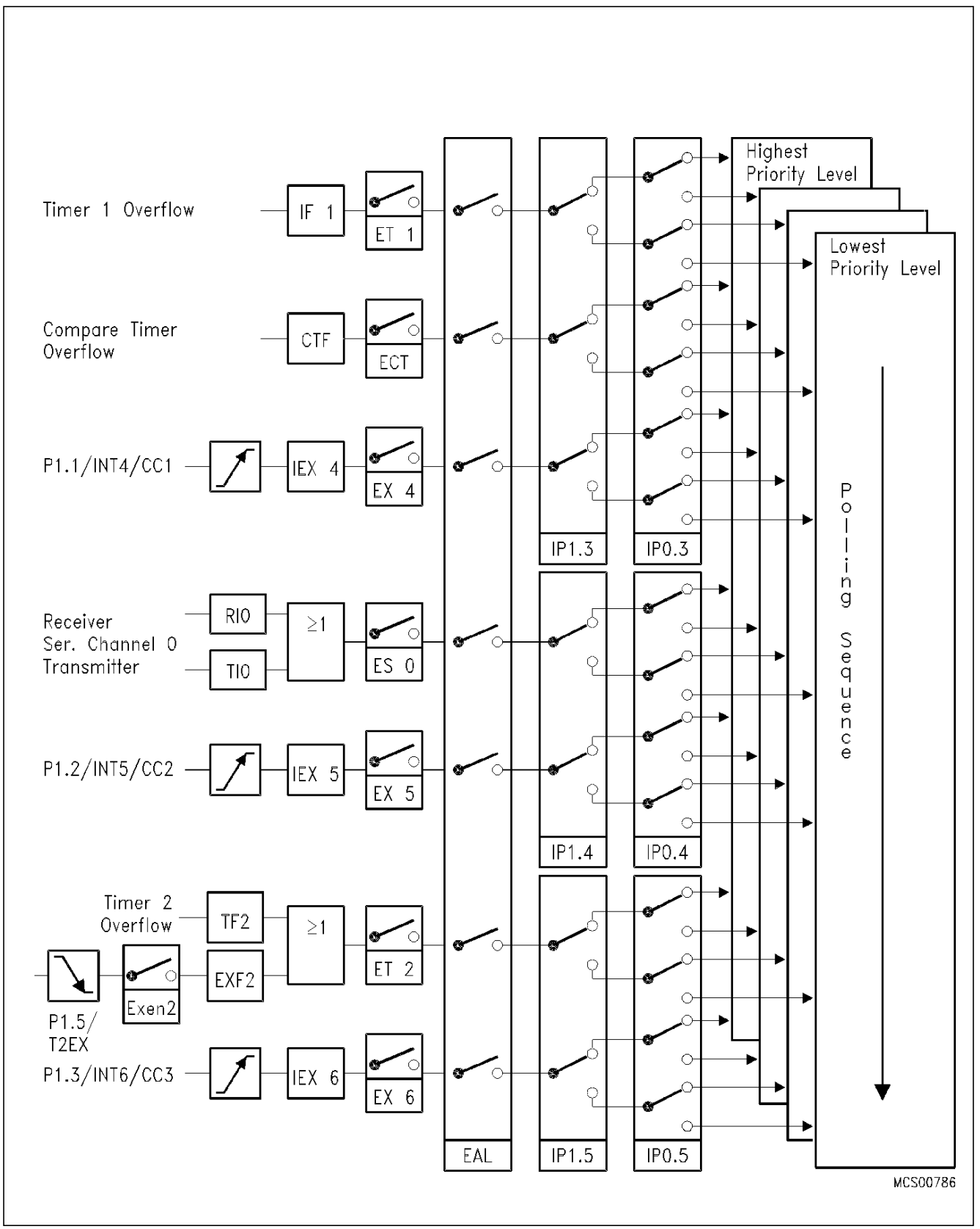


Figure 9 (cont'd)
Interrupt Structure

Multiplication/Division Unit

This on-chip arithmetic unit provides fast 32-bit division, 16-bit multiplication as well as shift and normalize features. All operations are integer operations.

Operation	Result	Remainder	Execution Time
32-bit/16-bit 16-bit/16-bit	32-bit 16-bit	16-bit 16-bit	6 t_{cy} [1]) 4 t_{cy}
16-bit * 16-bit	32-bit	–	4 t_{cy}
32-bit normalize	–	–	6 t_{cy} [2])
32-bit shift left/right	–	–	6 t_{cy} [2])

1) 1 t_{cy} = 1 µs @ 12 MHz oscillator frequency.
2) The maximal shift speed is 6 shifts/cycle.

The MDU consists of six registers used for operands and results and one control register. Operation of the MDU can be divided in three phases:

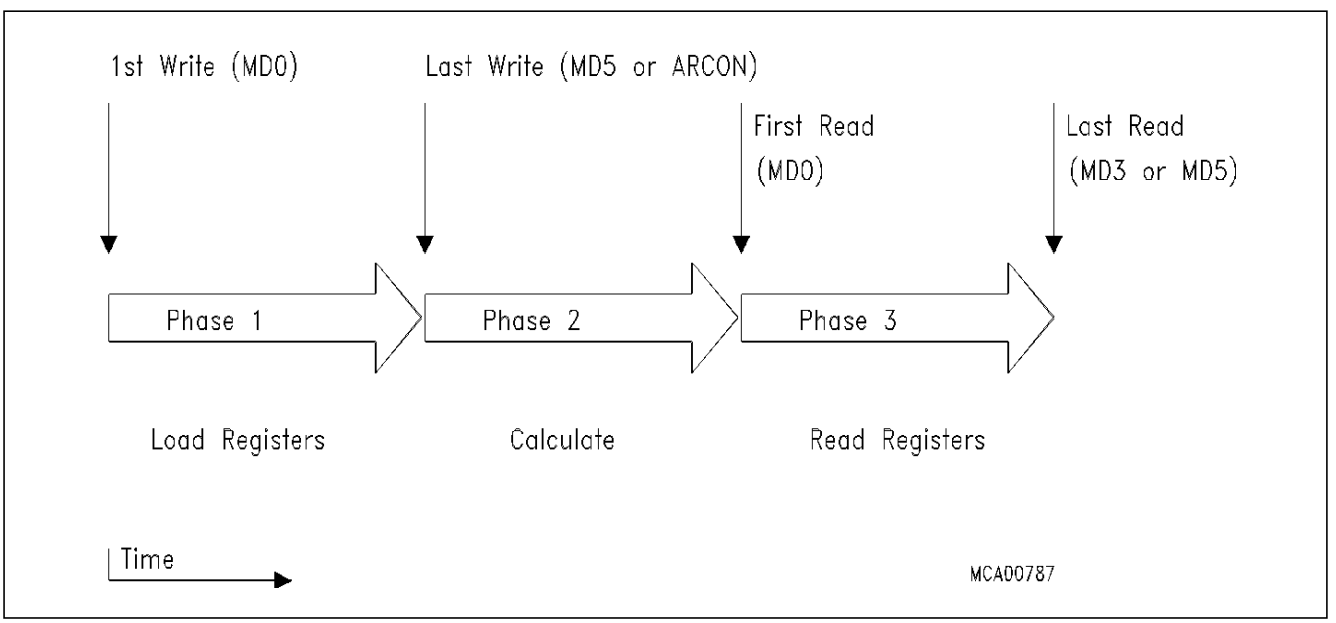


Figure 10
Operation of the MDU

To start an operation, register MD0 to MD5 (or ARCON) must be written to in a certain sequence according to table 5 or 6. The order the registers are accessed determines the type of the operation. A shift operation is started by a final write operation to register ARCON (see also the register description).

Table 5
Performing a MDU-Calculation

Operation	32-Bit/16-Bit		16-Bit/16-Bit		16-Bit * 16-Bit	
First Write	MD0	D'endL	MD0	D'endL	MD0	M'andL
	MD1	D'end	MD1	D'end	MD4	M'orL
	MD2	D'end	MD2	D'end	MD1	M'andH
	MD3	D'endH	MD3	D'endH	MD5	M'orH
	MD4	D'orL	MD4	D'orL		
Last Write	MD5	D'orH	MD5	D'orH		
First Read	MD0	QuoL	MD0	QuoL	MD0	PrL
	MD1	Quo	MD1	Quo	MD1	Pr
	MD2	Quo	MD2	Quo	MD2	Pr
	MD3	QuoH	MD3	QuoH	MD3	PrH
	MD4	RemL	MD4	RemL		
Last Read	MD5	RemH	MD5	RemH		

Table 6
Shift Operation with the CCU

Operation	Normalize, Shift Left, Shift Right	
First Write	MD0	least significant byte
	MD1	
	MD2	
	MD3	most significant byte
Last Write	ARCON	start of conversion
First Read	MD0	least significant byte
	MD1	
	MD2	
Last Read	MD3	most significant byte

Abbreviations

D'end : Dividend, 1st operand of division
D'or : Divisor, 2nd operand of division
M'and : Multiplicand, 1st operand of multiplication
M'or : Multiplicator, 2nd operand of multiplication
Pr : Product, result of multiplication
Rem : Remainder
Quo : Quotient, result of division
...L : means, that this byte is the least significant of the 16-bit or 32-bit operand
...H : means, that this byte is the most significant of the 16-bit or 32-bit operand

I/O Ports

The SAB 80C517 has seven 8-bit I/O ports and two input ports (8-bit and 4-bit wide).

Port 0 is an open-drain bidirectional I/O port, while ports 1 to 6 are quasi-bidirectional I/O ports with internal pull-up resistors. That means, when configured as inputs, ports 1 to 6 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET. Port 1, 3, 4, 5 and port 6 provide several alternate functions. Please see the "Pin Description" for details.

Port pins show the information written to the port latches, when used as general purpose port. When an alternate function is used, the port pin is controlled by the respective peripheral unit. Therefore the port latch must contain a "one" for that function to operate. The same applies when the port pins are used as inputs. Ports 1, 3, 4 and 5 are bit- addressable.

The SAB 80C517 has two dual-purpose input ports. The twelve port lines at port 7 and port 8 can be used as analog inputs for the A/D converter. If input voltages at P7 and P8 meet the specified digital input levels (V_{IL} and V_{IH}) the port can also be used as digital input port.

Power Saving Modes

The SAB 80C517 provides – due to Siemens ACMOS technology – three modes in which power consumption can be significantly reduced.

– The **Slow Down Mode**
  The controller keeps up the full operating functionality, but is driven with the eighth part of its normal operating frequency. Slowing down the frequency greatly reduces power consumption.

– The **Idle Mode**
  The CPU is gated off from the oscillator, but all peripherals are still supplied by the clock and able to work.

– The **Power Down Mode**
  Operation of the SAB 80C517 is stopped, the oscillator is turned off. This mode is used to save the contents of the internal RAM with a very low standby current.

All of these modes are entered by software. Special function register PCON (power control register, address is 87H) is used to select one of these modes.

Hardware Enable for Power Saving Modes

A dedicated Pin ($\overline{PE}$/SWD) of the SAB 80C517 allows to block the power saving modes. Since this pin is mostly used in noise-critical application it is combined with an automatic start of the Watchdog Timer (see there for further description).

$\overline{PE}$/SWD = V_{IH} (logic high level):	Using of the power saving modes is not possible. The instruction sequences used for entering of these modes will not affect the normal operation of the device.
$\overline{PE}$/SWD = V_{IL} (logic low level):	All power saving modes can be activated by software. When left unconnected, Pin $\overline{PE}$/SWD is pulled to high level by a weak internal pullup. This is done to provide system protection on default.

The logic-level applied to pin $\overline{PE}$/SWD can be changed during program execution to allow or to block the use of the power saving modes without any effect on the on-chip watchdog circuitry.

Power Down Mode

The power down mode is entered by two consecutive instructions directly following each other. The first instruction has to set the flag PDE (power down enable) and must not set PDS (power down set). The following instruction has to set the start bit PDS. Bits PDE and PDS will automatically be cleared after having been set.

The instruction that sets bit PDS is the last instruction executed before going into power down mode. The only exit from power down mode is a hardware reset.

The status of all output lines of the controller can be looked up in table 7.

Table 7
Status of External Pins During Idle and Power Down

Outputs	Last instruction executed from internal code memory		Last instruction executed from external code memory	
	Idle	**Power down**	**Idle**	**Power Down**
ALE	High	Low	High	Low
PSEN	High	Low	High	Low
Port 0	Data	Data	Float	Float
Port 1	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output
Port 2	Data	Data	Address	Data
Port 3	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output
Port 4	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output
Port 5	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output
Port 6	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output

Idle Mode

During idle mode all peripherals of the SAB 80C517 are still supplied by the oscillator clock. Thus the user has to take care which peripheral should continue to run and which has to be stopped during Idle.

The procedure to enter the Idle mode is similar to entering the power down mode.
The two bits IDLE and IDLS must be set by to consecutive instructions to minimize the chance of unintentional activating of the idle mode.

There are two ways to terminate the idle mode:

– The idle mode can be terminated by activating any enabled interrupt. This interrupt will be serviced and normally the instruction to be executed following the RETI instruction will be the one following the instruction that sets the bit IDLS.

– The other way to terminate the idle mode, is a hardware reset. Since the oscillator is still running, the hardware reset must be held active only for two machine cycles for a complete reset.

Normally the port pins hold the logical state they had at the time idle mode was activated. If some pins are programmed to serve their alternate functions they still continue to output during idle mode if the assigned function is on. The control signals ALE and $\overline{\text{PSEN}}$ hold at logic high levels (see table 7).

Table 8
Baud Rate Generation

Function		Serial Interface 0		Serial Interface 1
8-Bit synchronous channel	**Mode**	**Mode 0**		–
	Baud rate *)	1 MHz @ f_{OSC} = 12 MHz		–
	Baud rate derived from	f_{OSC}		–
8-Bit UART	**Mode**	**Mode 1**		**Mode B**
	Baud rate *)	1 – 62.5 K	4800, 9600	1.5 – 375 K
	Baud rate derived from	Timer 1	BD	8-bit baud rate generator
9-Bit UART	**Mode**	**Mode 2**	**Mode 3**	**Mode A**
	Baud rate *)	187.5 K/ 375 K	1 – 62.5 K	1.5 – 375 K
	Baud rate derived from	$f_{OSC}/2$	Timer 1	8-bit baud rate generator

*) Baud rate values are given for 12 MHz oscillator frequency.

Serial Interface 0

Serial Interface 0 can operate in 4 modes:

Mode 0: Shift register mode:
Serial data enters and exits through R × D0. T × D0 outputs the shift clock 8 data bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 8-bit UART, variable baud rate:
10-bit are transmitted (through R × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On reception, the stop bit goes into RB80 in special function register S0CON. The baud rate is variable.

Mode 2: 9-bit UART, fixed baud rate:
11-bit are transmitted (through T × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). On transmission, the 9th data bit (TB80 in S0CON) can be assigned to the value of 0 or 1. For example, the parity bit (P in the PSW) could be moved into TB80 or a second stop bit by setting TB80 to 1. On reception the 9th data bit goes into RB80 in special function register S0CON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 9-bit UART, variable baud rate:
11-bit are transmitted (through T × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). In fact, mode 3 is the same as mode 2 in all respects except the baud rate. The baud rate in mode 3 is variable.

Variable Baud Rates for Serial Interface 0

Variable baud rates for modes 1 and 3 of serial interface 0 can be derived from either timer 1 or from the oscillator via a special prescaler ("BD").

Timer 1 may be operated in mode 1 (to generate slow baud rates) or mode 2. The dedicated baud rate generator "BD" provides the two standard baud rates 4800 or 9600 baud. Table 8 shows possible configurations and the according baud rates.

Serial Interface 1

Serial interface 1 can operate in two asynchronous modes:

Mode A: 9-bit UART, variable baud rate.
11 bits are transmitted (through T×D0) or received (through R×D0): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). On trans- mission, the 9th data bit (TB81 in S1CON) can be assigned to the value of 0 or 1. For example, the parity bit (P in the PSW) could be moved into TB81 or a second stop bit by setting TB81 to 1. On reception the 9th data bit goes into RB81 in special function register S1CON, while the stop bit is ignored.

Mode B: 8-bit UART, variable baud rate.
10 bits are transmitted (through T×D1) or received (through R×D1): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On reception, the stop bit goes into RB81 in special function register S1CON.

Variable Baud Rates for Serial Interface 1

Variable baud rates for modes A and B of serial interface 1 can be derived from a dedicated baud rate generator.

The baud rate clock (baud rate = $\frac{\text{baud rate clock}}{16}$) is generated by a 8-bit free running timer with programmable reload register.

Watchdog Units

The SAB 80C517 offers two enhanced fail safe mechanisms, which allow an automatic recovery from hardware failure or software upset:

– programmable watchdog timer (WDT), variable from 512 µs up to about 1.1 s time out period @12 MHz. Upward compatible to SAB 80515 watchdog.

– oscillator watchdog (OWD), monitors the on-chip oscillator and forces the micro-controller to go into reset state, in case the on-chip oscillator fails.

Programmable Watchdog Timer

The WDT can be activated by hardware or software.

Hardware initialization is done when pin $\overline{\text{PE}}$/SWD (Pin 4) is held high during RESET. The SAB 80C517 then starts program execution with the WDT running. Pin $\overline{\text{PE}}$/SWD doesn't allow dynamic switching of the WDT.

Software initialization is done by setting bit SWDT. A refresh of the watchdog timer is done by setting bits WDT and SWDT consecutively.

A block diagram of the watchdog timer is shown in figure 11.

When a watchdog timer reset occurs, the watchdog timer keeps on running, but a status flag WDTS is set. This flag can also be manipulated by software.

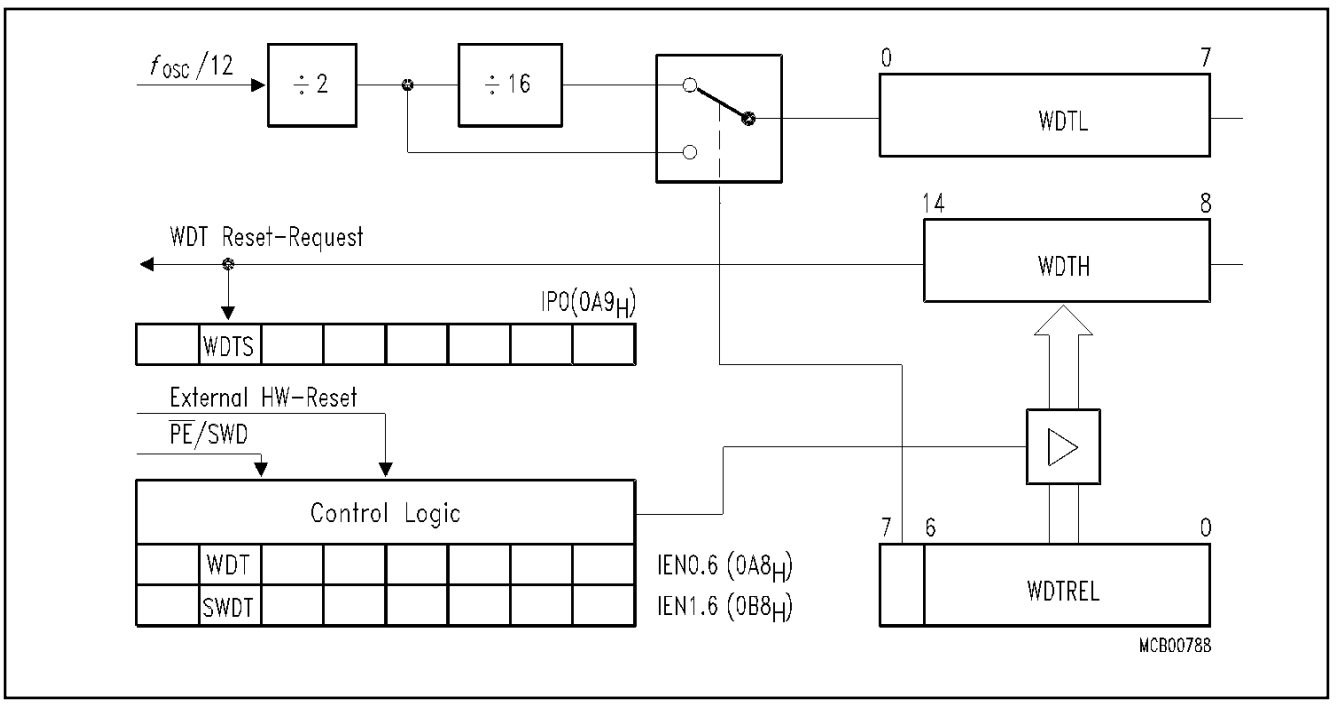


Figure 11
Block Diagram of the Programmable Watchdog Timer

Oscillator Watchdog

The oscillator watchdog monitors the on-chip quartz oscillator. A detected oscillator failure (f_{OSC} < appr. 300 kHz) causes a hardware reset. The reset state is held until the on-chip oscillator is working again. The oscillator watchdog feature is enabled by a high level at pin OWE (pin 69). An oscillator watchdog reset sets status flag OWDS which can be examined and modified by software. Figure 12 shows a block diagram of the oscillator watchdog.

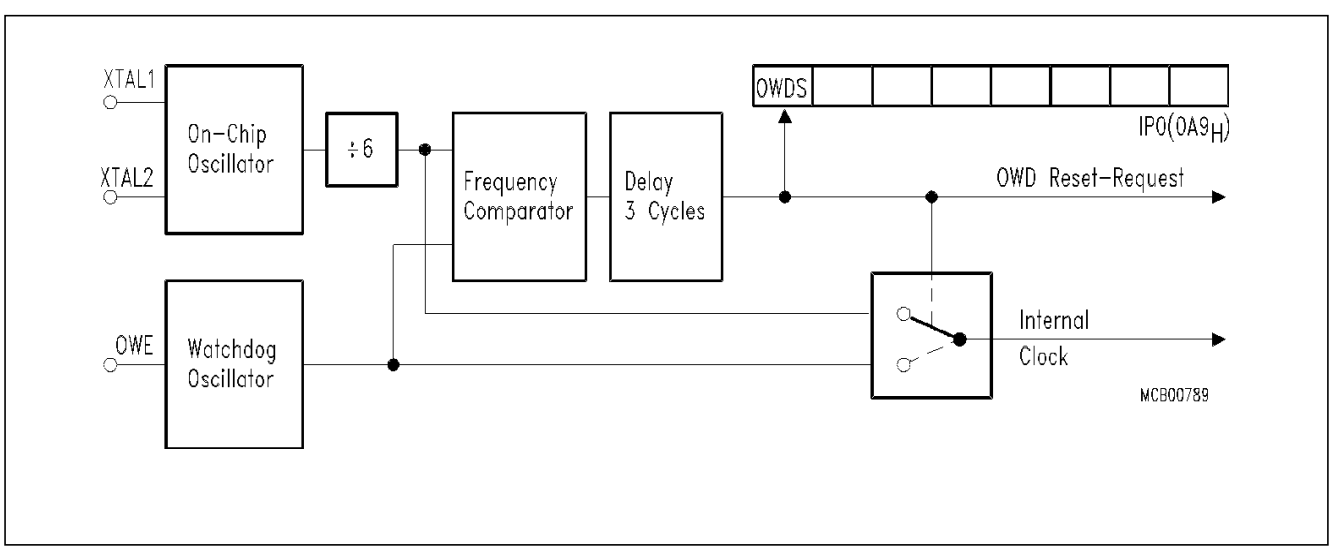


Figure 12
Functional Block Diagram of the Oscillator Watchdog

Instruction Set Summary

The SAB 80C517/80C537 has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function Registers, Interrupt Vectors and Assembler Directives.

Literature Information

Title	Ordering No.
Microcontroller Family SAB 8051 Pocket Guide	B158-H6497-X-X-7600

Absolute Maximum Ratings

Ambient temperature under bias
SAB 80C517/83C537 ..... 0 to 70 °C
SAB 80C517/83C537-T40/85 ..... – 40 to 85 °C
Storage temperature T_{ST} ..... – 65 to 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS}) ..... – 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}) ..... – 0.5 to V_{CC} +0.5 V
Input current on any pin during overload condition ..... – 10mA to +10mA
Absolute sum of all input currents during overload condition ..... |100mA|
Power dissipation ..... 2 W

Note *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) theVoltage on V_{CC} pins with respect to ground (V_{SS}) must not exeed the values definded by the absolute maximum ratings.*

DC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V;
T_A = 0 to 70 °C for the SAB 80C517/83C537
T_A = – 40 to 85 °C for the SAB 80C517-/83C537-T40/85

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Input low voltage (except $\overline{EA}$)	V_{IL}	– 0.5	0.2 V_{CC} – – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – – 0.3	V	–
Input high voltage	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL2	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage to $\overline{RESET}$	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage (ports 1, 2, 3, 4, 5, 6)	V_{OL}	–	0.45	V	I_{OL}=1.6 mA[1)]

Notes see page 341.

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Output low voltage (ports ALE, $\overline{PSEN}$, $\overline{RO}$)	V_{OL1}	–	0.45	V	I_{OL}=3.2mA [1]
Output high voltage (ports 1, 2, 3, 4, 5, 6)	V_{OH}	2.4 0.9 V_{CC}	– –	V V	I_{OH}=–80 µA I_{OH}=–10 µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$, $\overline{RO}$)	V_{OH1}	2.4 0.9 V_{CC}	– –	V V	I_{OH}=–800 µA[2] I_{OH}=–80 µA[2]
Logic 0 input current (ports 1, 2, 3, 4, 5, 6)	I_{IL}	– 10	– 70	µA	V_{IN} = 0.45 V
Input low current to $\overline{RESET}$ for reset	I_{IL2}	– 10	–100	µA	V_{IN} = 0.45 V
Input low current (XTAL2)	I_{IL3}	–	– 15	µA	V_{IN} = 0.45 V
Input low current (OWE, $\overline{PE}$/SWD)	I_{IL4}	–	– 20	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 1, 2, 3, 4, 5, 6)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$, ports 7, 8)	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}[10]
Pin capacitance	C_{IO}	–	10	pF	f_C= 1 MHz T_A= 25 °C
Power supply current:					
Active mode, 12 MHz [6]	I_{CC}	–	40	mA	V_{CC} = 5 V,[4]
Idle mode, 12 MHz [6]		–	15	mA	V_{CC} = 5 V,[5]
Slow down mode, 12 MHz [6]		–	15	mA	V_{CC} = 5 V,[5]
Active mode, 16 MHz [6]	I_{CC}	–	52.3	mA	V_{CC} = 5 V,[4]
Idle mode, 16 MHz [6]		–	19	mA	V_{CC} = 5 V,[5]
Slow down mode, 16MHz[6]		–	19	mA	V_{CC} = 5 V,[5]
Power down Mode	I_{PD}	–	50	µA	V_{CC} = 2...5.5 V [3]

Notes see page 341.

A/D Converter Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
V_{AREF} = V_{CC} ± 5%; V_{AGND} = V_{SS} ± 0.2 V; $V_{IntAREF}$ - $V_{IntAGND}$ ≥ 1V
T_A = 0 to 70 °C for the SAB 80C517/83C537
T_A = – 40 to 85 °C for the SAB 80C517/83C537-T40/875

Parameter	Symbol	Limit values			Unit	Test condition
		min.	typ.	max.		
Analog input voltage	V_{AINPUT}	V_{AGND} – 0.2	–	V_{AREF} + 0.2	V	9)
Analog input capacitance	C_I	–	25	60	pF	7)
Load time	t_L	–	–	2 t_{CY}	µs	7)
Sample time (incl. load time)	t_S	–	–	7t_{CY}	µs	7)
Conversion time (incl. sample time)	t_C	–	–	13 t_{CY}	µs	7)
Differential non-linearity Integral non-linearity Offset error Gain error Total unadjusted error	DNLE INLE TUE	– – 	± 1/2 ± 1/2 ± 1/2 ± 1/2 ± 1	± 1 ± 1 ± 1 ± 1 ± 2	LSB LSB LSB LSB LSB	$V_{IntAREF}$ = V_{AREF} = V_{CC} $V_{IntAGND}$ = V_{AGND} = V_{SS} 7)
Internal reference error	$V_{IntREFERR}$	–		± 30	mV	8)
V_{AREF} supply current	I_{REF}	–	–	5	mA	8)

Notes see page 341.

Notes for pages 338, 339 and 340:

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1, 3, 4, 5 and 6. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation.
In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt- trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) Power down I_{PD} is measured with all output pins disconnected;
$\overline{EA}$ = $\overline{RESET}$ = V_{CC}; Port 0 = Port 7 = Port 8 = V_{CC}; XTAL1 = N.C.; XTAL2 = V_{SS};
V_{AGND}= N.C.; V_{AREF} = V_{CC}; $\overline{PE}$/SWD = OWE = V_{SS}.

4) I_{CC} (active mode) is measured with all output pins disconnected; XTAL2 driven with clock signal according to the figure below; XTAL1 = N.C.;
$\overline{EA}$ = OWE = $\overline{PE}$/SWD = V_{CC}; Port 0 = Port 7 = Port 8 = V_{CC};
$\overline{RESET}$ = V_{SS}. I_{CC} would be slightly higher if a crystal oscillator is used.

5) I_{CC} (idle mode,) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with clock signal according to the figure below; XTAL1 = N.C.;
$\overline{RESET}$ = OWE = V_{CC}; Port 0 = Port 7 = Port 8 = V_{CC}; $\overline{EA}$ = $\overline{PE}$/SWD = V_{SS}.
I_{CC} (slow down mode) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with clock signal according to the figure below; XTAL = N.C.; Port 7 = Port 8 = V_{CC}; $\overline{EA}$ = $\overline{PE}$/SWD = V_{SS}.

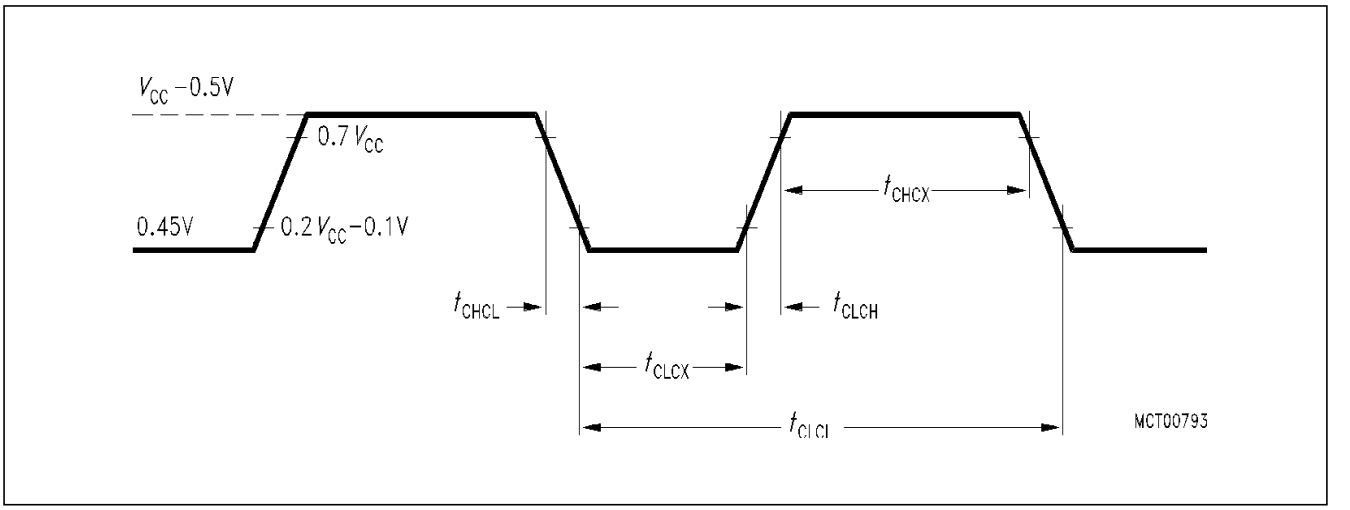
6) I_{CC} (max.) at other frequencies is given by: active mode: I_{CC} max = 3.1 $*$ f_{OSC} + 3.0
idle mode: I_{CC} max = 1.0 $*$ f_{OSC} + 3.0
Where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V (see also notes 4 and 5).

7) The output impedance of the analog source must be low enough to assure full loading of the sample capacitance (C_I) during load time (T_L). After charging of the internal capacitance (C_I) in the load time (T_L) the analog input must be held constant for the rest of the sample time (T_S).

8) The differential impedance R_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

9) Exceeding the limit values at one or more input channels will cause additional current which is sinked sourced at these channels. This may also affect the accuracy of other channels which are operated within the specification.

10) Only valid for not selected analog inputs.



Clock of Waveform for I_{CC} Tests in Active, Idle Mode and Slow Down Mode

AC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V T_A = 0 to 70 °C for the SAB 80C517/83C537
T_A = – 40 to 85 °C for the SAB 80C517/83C537-T40/85
(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF))

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min	max.	min.	max.	
Program Memory Characteristics						
ALE pulse width	t_{LHLL}	127	–	2 t_{CLCL} – 40	–	ns
Address setup to ALE	t_{AVLL}	53	–	t_{CLCL} – 30	–	ns
Address hold after ALE	t_{LLAX}	48	–	t_{CLCL} – 35	–	ns
ALE to valid instruction in	t_{LLIV}	–	233	–	$4t_{CLCL}$ – 100	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	58	–	t_{CLCL} – 25	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	215	–	3 t_{CLCL} – 35	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	t_{PLIV}	–	150	–	$3t_{CLCL}$ – 100	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0		ns
Input instruction float after $\overline{\text{PSEN}}$ *)	t_{PXIX}*)	–	63	–	t_{CLCL} – 20	ns
Address valid after $\overline{\text{PSEN}}$ *)	t_{PXAV}*)	75	–	t_{CLCL} – 8	–	ns
Address to valid instruction in	t_{AVIV}	–	302	0	$5t_{CLCL}$ – 115	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	–	–	–		ns

*) Interfacing the SAB 80C517 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	400	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	132	–	2 t_{CLCL} – 30	–	ns
$\overline{RD}$ to valid instr in	t_{RLDV}	–	252	–	5 t_{CLCL} – 165	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	2 t_{CLCL} – 70	ns
ALE to valid data in	t_{LLDV}	–	517	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	585	–	9 t_{CLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	3 t_{CLCL} – 50	3 t_{CLCL} +50	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	t_{CLCL} – 40	t_{CLCL} +40	ns
Address valid to $\overline{WR}$	t_{AVWL}	203	–	4 t_{CLCL} – 130	–	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	t_{CLCL} – 50	–	ns
Data setup before $\overline{WR}$	t_{QVWX}	433	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	t_{CLCL} – 50	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

AC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB 80C517-16/83C537-16

T_A = – 40 to 85 °C for the SAB 80C517-16/83C537-16-T40/85

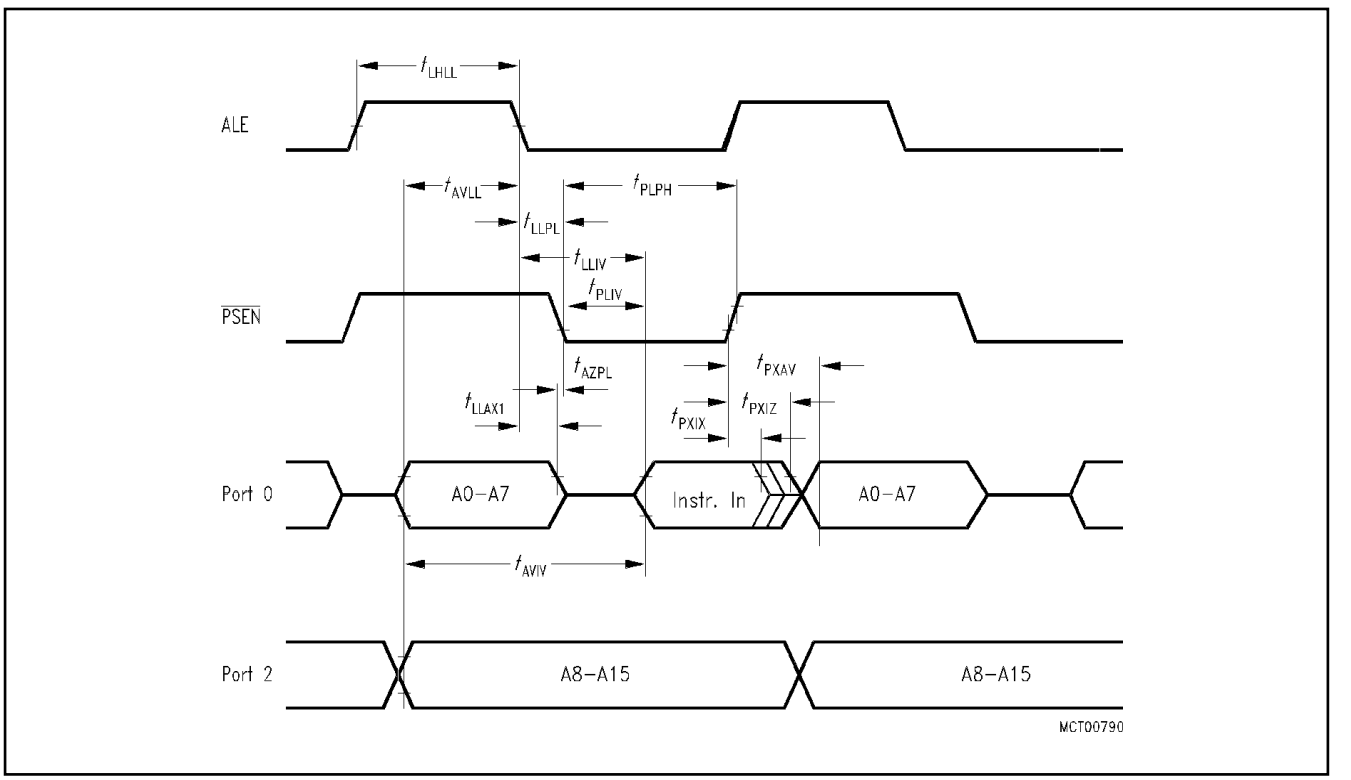
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100pF; C_L for all outputs = 80 pF)

Parameter	Symbol	Limit values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 16 MHz		
		min	max.	min.	max.	
Program Memory Characteristics						
ALE pulse width	t_{LHLL}	85	–	2 t_{CLCL} – 40	–	ns
Address setup to ALE	t_{AVLL}	33	–	t_{CLCL} – 30	–	ns
Address hold after ALE	t_{LLAX}	28	–	t_{CLCL} – 35	–	ns
ALE to valid instr. in	t_{LLIV}	–	150	–	4t_{CLCL} – 100	ns
ALE to $\overline{PSEN}$	t_{LLPL}	38	–	t_{CLCL} – 25	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	153	–	3 t_{CLCL} – 35	–	ns
$\overline{PSEN}$ to valid instr. in	t_{PLIV}	–	88	–	3t_{CLCL} – 100	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float *) after $\overline{PSEN}$	t_{PXIZ}	–	43	–	t_{CLCL} – 20	ns
Address valid after $\overline{PSEN}$ *)	t_{PXAV}	55	–	t_{CLCL} – 8	–	ns
Address to valid instr. in	t_{AVIV}	–	198	0–	5t_{CLCL} – 115	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

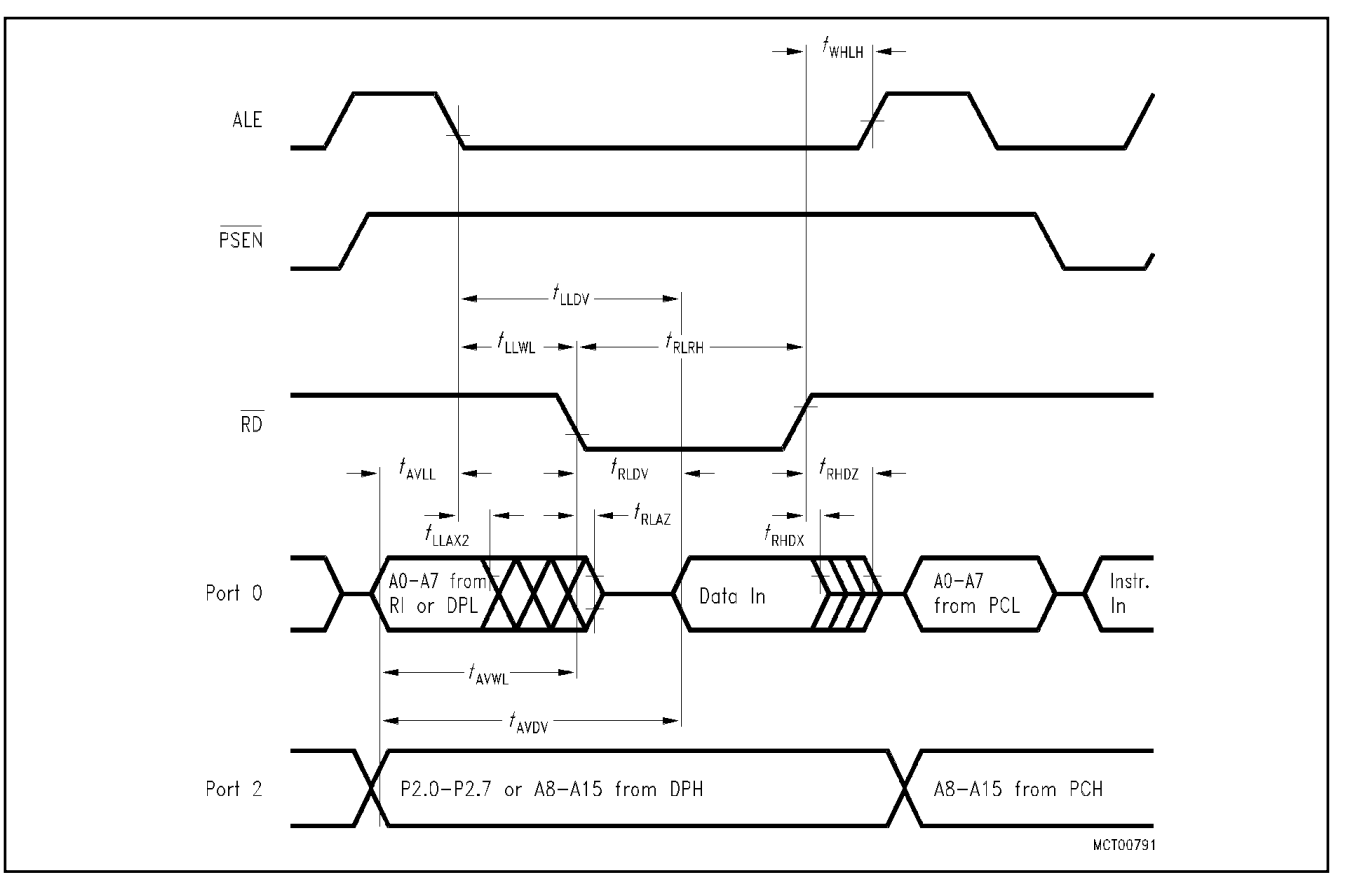
*) Interfacing the SAB 80C517 to devices with float times up to 55 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

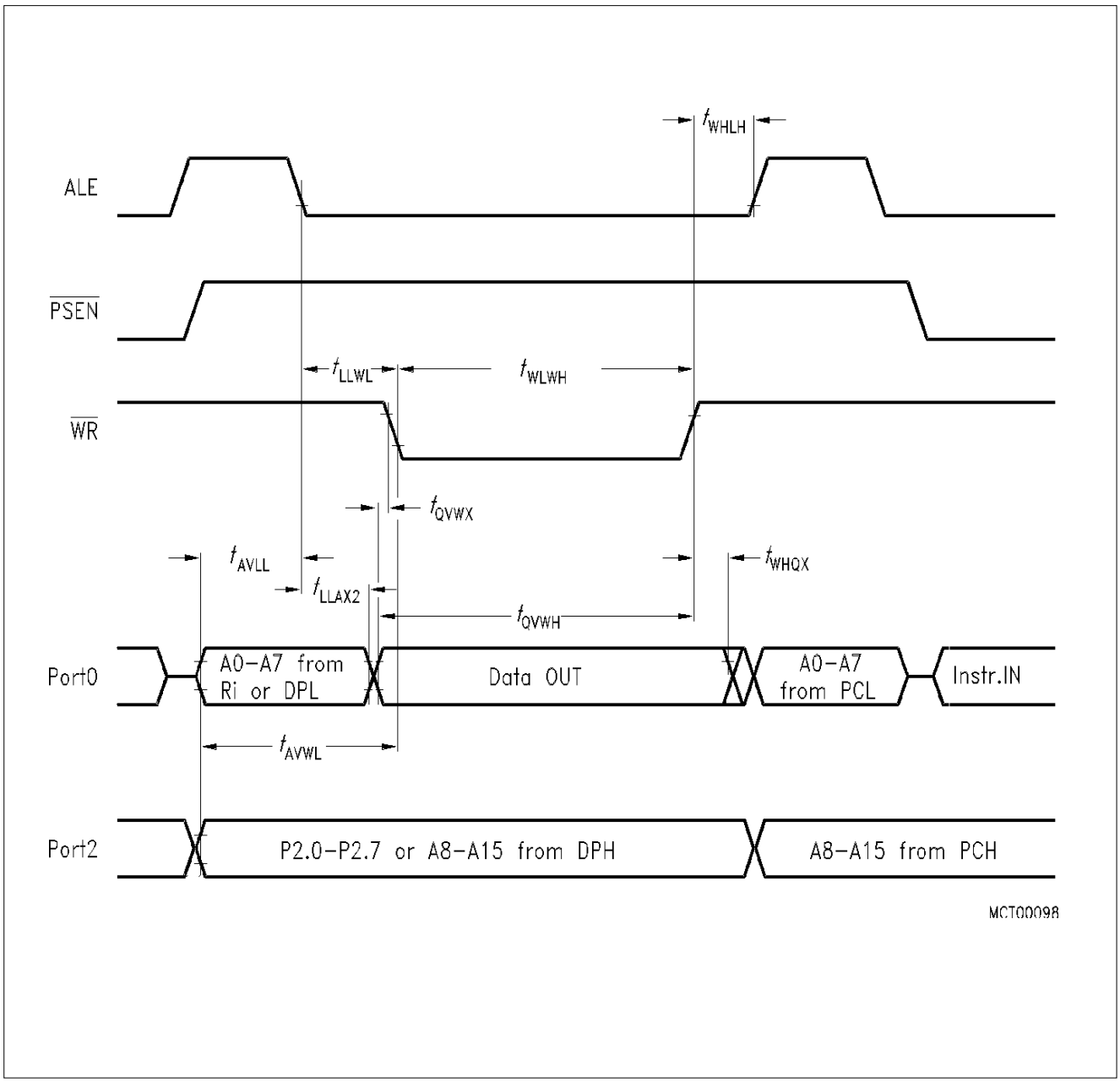
Parameter	Symbol	Limit values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 16 MHz		
		min	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	275	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	275	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	90	–	2 t_{CLCL} – 35	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	148	–	5 t_{CLCL} – 165	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	55	–	2 t_{CLCL} – 70	ns
ALE to valid data in	t_{LLDV}	–	350	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	398	–	9 t_{CLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	138	238	3 t_{CLCL} – 50	3 t_{CLCL} +50	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	23	103	t_{CLCL} – 40	t_{CLCL} +40	ns
Address valid to $\overline{WR}$	t_{AVWL}	120	–	4 t_{CLCL} – 130	–	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	13	–	t_{CLCL} – 50	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	288	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	13	–	t_{CLCL} – 50	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns



Program Memory Read Cycle



Data Memory Read Cycle



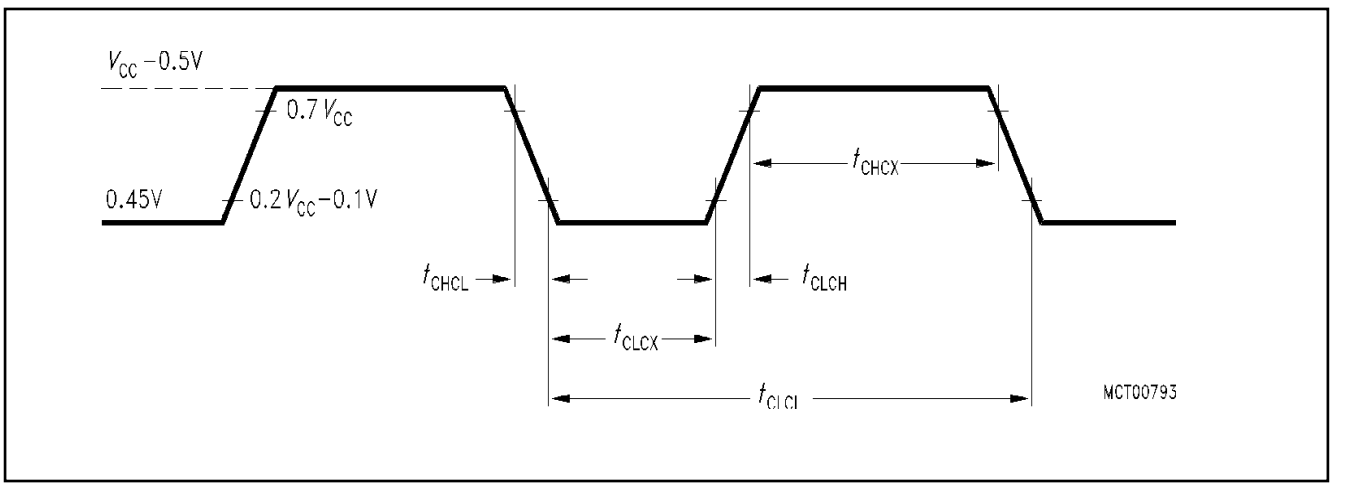
Data Memory Write Cycle

AC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 3.5 MHz to 12 MHz		
		min	max.	
External Clock Drive				
Oscillator period	t_{CLCL}	83.3	285	ns
Oscillator frequency	$1/t_{CLCL}$	3.5	12	MHz
High time	t_{CHCX}	20	–	ns
Low time	t_{CLCX}	20	–	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns

AC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 1 MHz to 16 MHz		
		min	max.	
External Clock Drive				
Oscillator period	t_{CLCL}	62.5	285	ns
Oscillator frequency	$1/t_{CLCL}$	3.5	16	MHz
High time	t_{CHCX}	25	–	ns
Low time	t_{CLCX}	25	–	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns



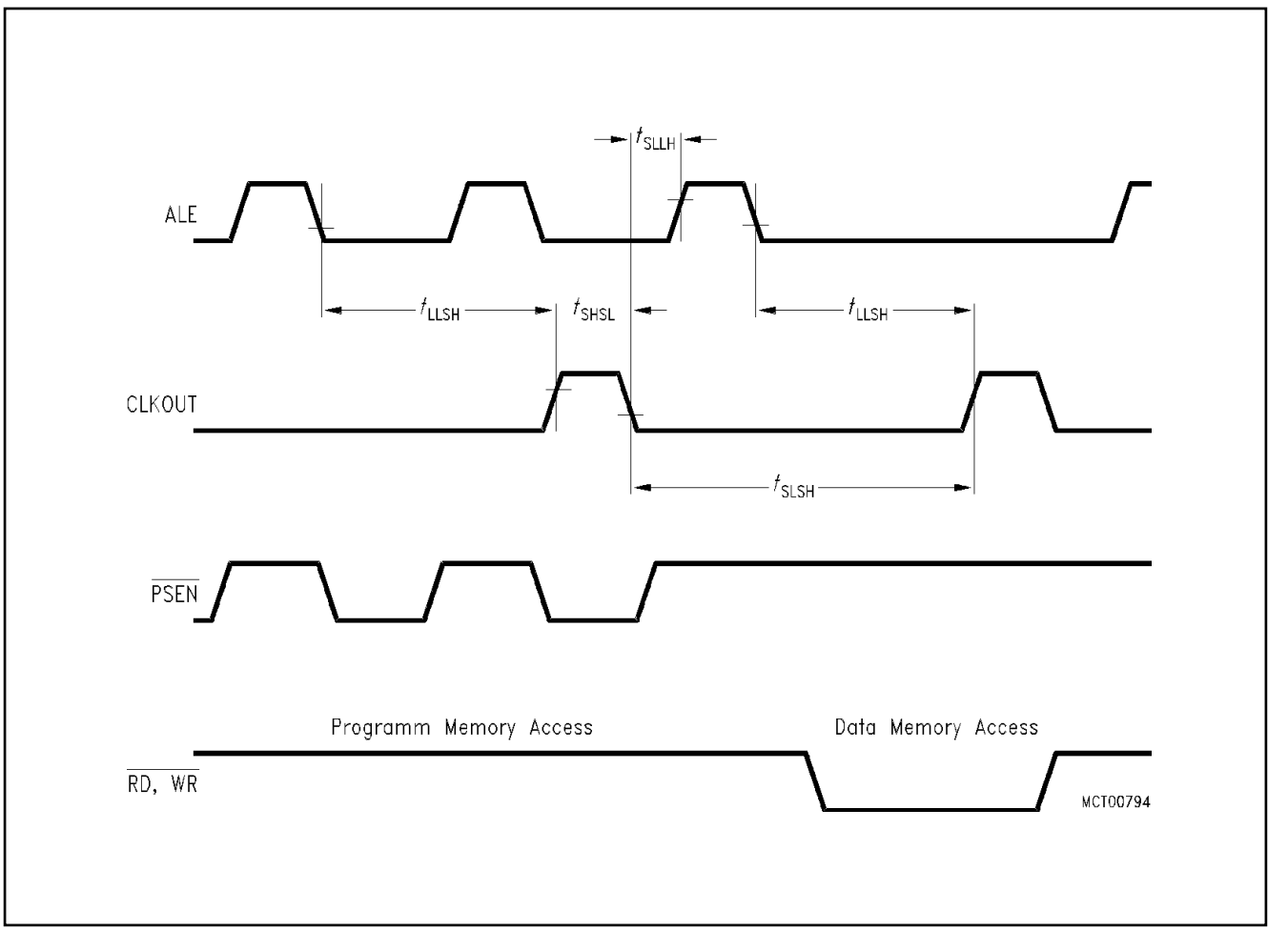
External Clock Cycle

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
System Clock Timing						
ALE to CLKOUT	t_{LLSH}	543	–	$7t_{CLCL} - 40$	–	ns
CLKOUT high time	t_{SHSL}	127	–	$2t_{CLCL} - 40$	–	ns
CLKOUT low time	t_{SLSH}	793	–	$10t_{CLCL} - 40$	–	ns
CLKOUT low to ALE high	t_{SLLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 3.5 MHz to 16 MHz		
		min.	max.	min.	max.	
System Clock Timing						
ALE to CLKOUT	t_{LLSH}	398	–	$7t_{CLCL} - 40$	–	ns
CLKOUT high time	t_{SHSL}	85	–	$2t_{CLCL} - 40$	–	ns
CLKOUT low time	t_{SLSH}	585	–	$10t_{CLCL} - 40$	–	ns
CLKOUT low to ALE high	t_{SLLH}	23	103	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns



System Clock Timing

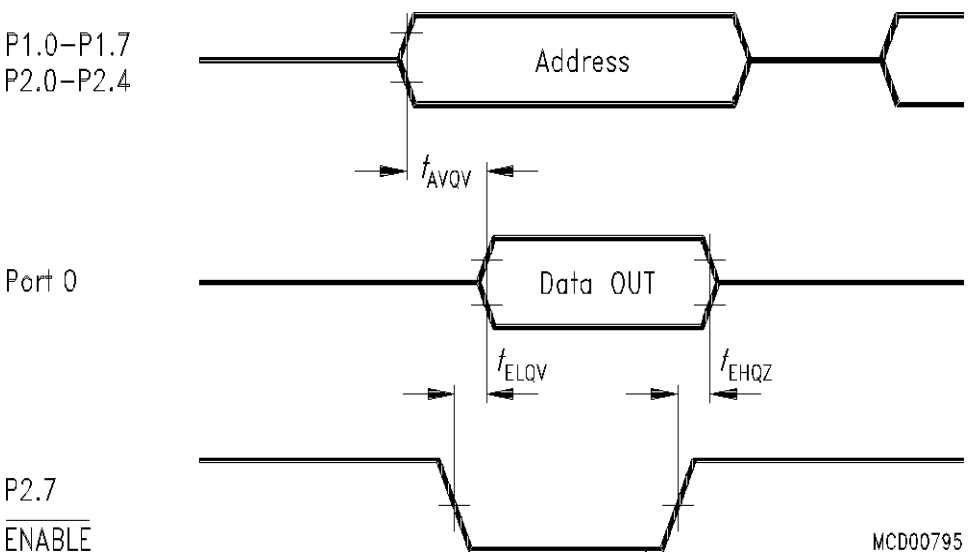
ROM Verification Characteristics

T_A = 25°C ± 5°C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Parameter	Symbol	Limit values		Unit
		min	max.	

ROM Verification

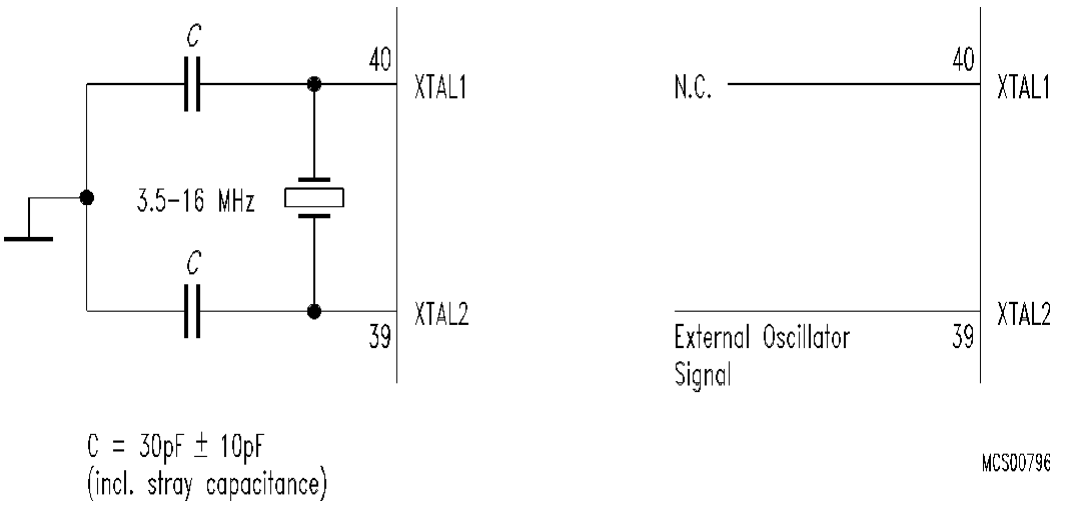
Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns
ENABLE to valid data	t_{ELQV}	–	48 t_{CLCL}	ns
Data float after ENABLE	t_{EHQZ}	0	48 t_{CLCL}	ns
Oscillator frequency	1/t_{CLCL}	4	6	MHz



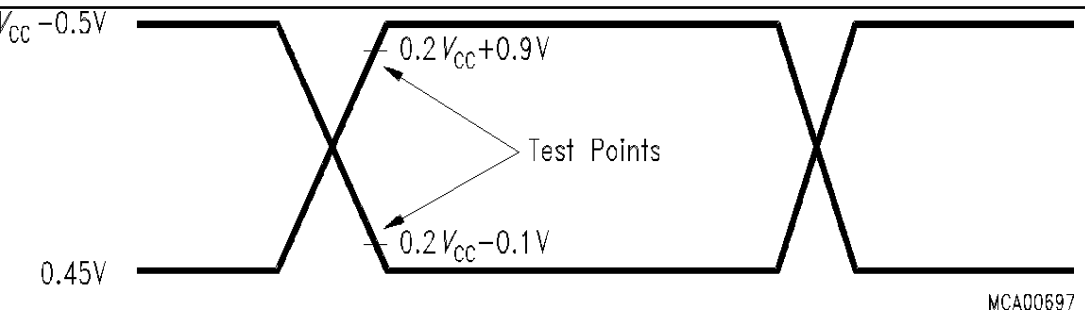
ROM Verification

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA

Recommended Oscillator Circuits

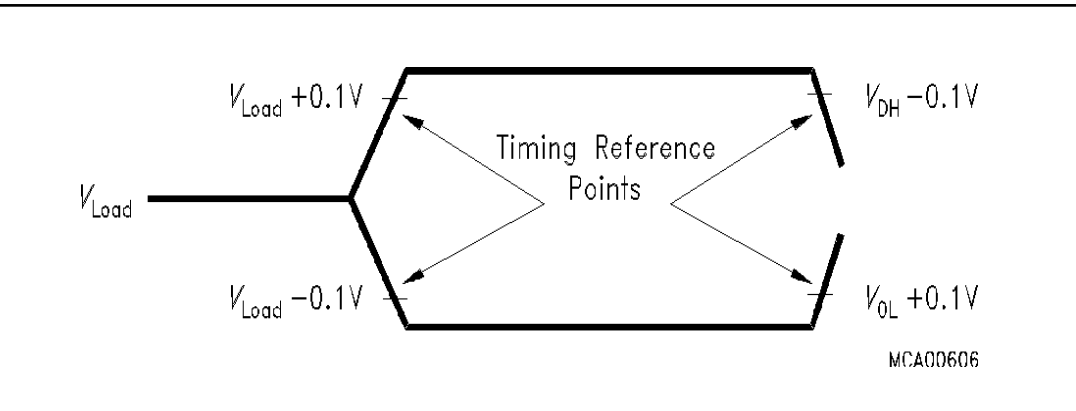


AC Testing



AC Inputs during testing are driven at V_{CC} – 0.5 V for a logic 1 and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Input, Output Waveforms

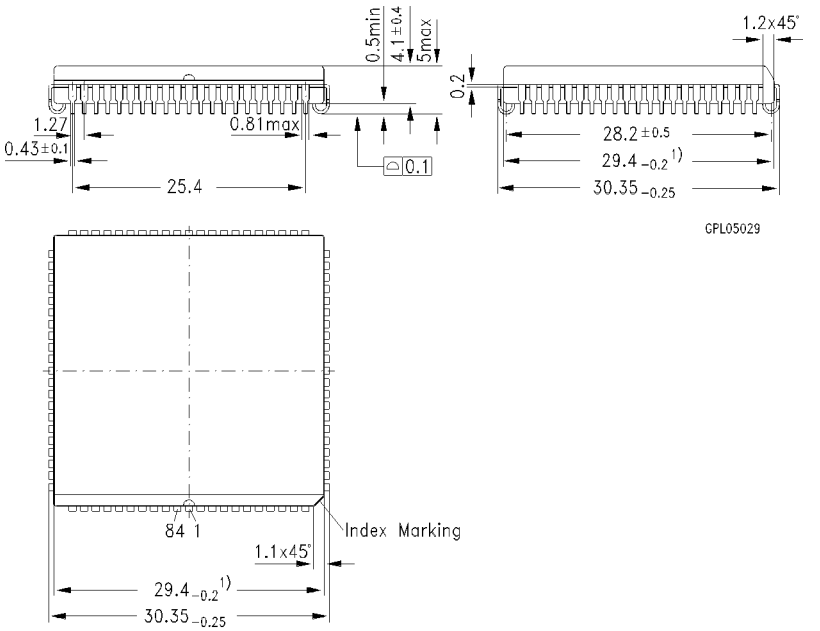


Float Waveforms

SMD = Surface Mounted Device

Package Outlines

Plastic Package, P-LCC-84 – SMD
(Plastic Leaded Chip-Carrier)

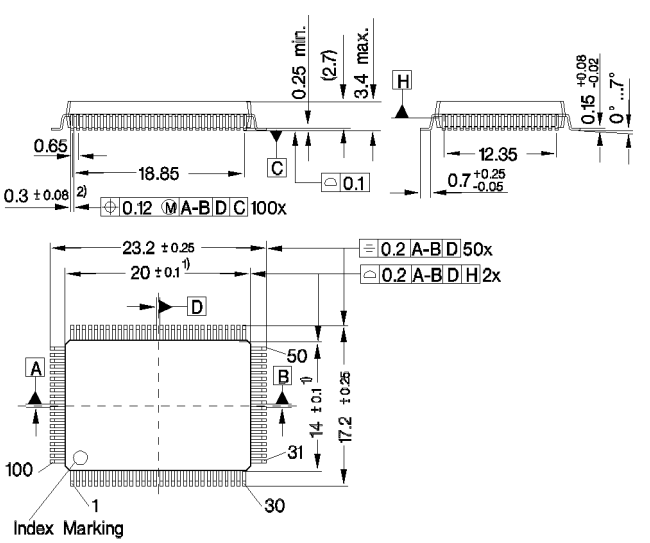


1) Does not include plastic or metal protrusions of 0.15max per side

SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, P-MQFP-100– 2 – SMD
(Plastic Metric Rectangular-Flat-Package)



2) Does not include dambar protrusion of 0.08 max. per side
1) Does not include plastic or metal protrusion of 0.25 max. per side

SMD = Surface Mounted Device

Dimensions in mm

SIEMENS

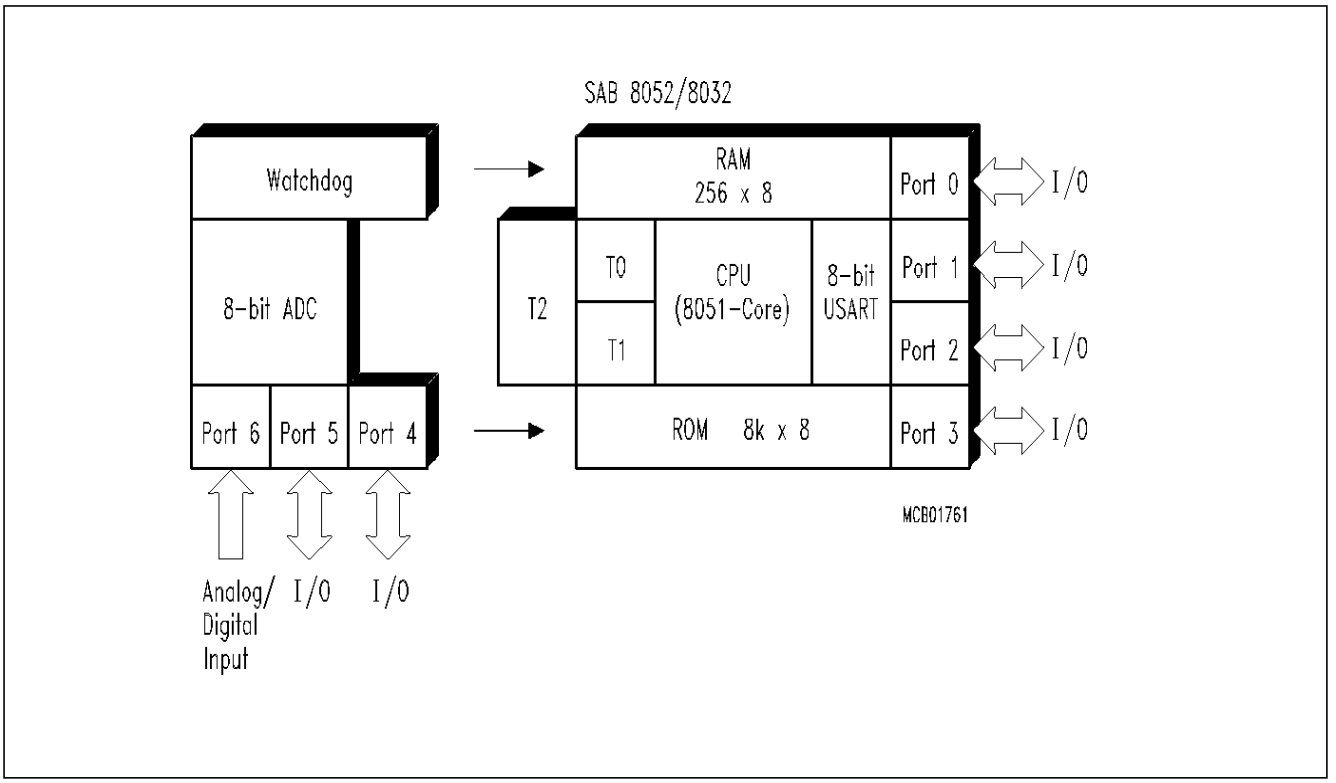
High-Performance
8-Bit Single Chip Microcontroller SAB 80515/80535

Preliminary

SAB 80515 Microcontroller with factory mask-programmable ROM
SAB 80535 Microcontroller for external ROM

- 8 K × 8 ROM (SAB 80C515 only)
- 256 × 8 RAM
- Six 8-bit I/O ports, one 8-bit input port for analog signals
- Three 16-bit timer/counters
- Highly flexible reload, capture, compare capabilities
- Full-duplex serial channel
- Twelve interrupt vectors, four priority levels
- 8-bit A/D converter with 8 multiplexed inputs and programmable internal reference voltages
- 16-bit watchdog timer
- V_{PD} provides standby current for 40 bytes of RAM
- Boolean processo
- 256-bit-addressable locations
- Most instructions execute in 1 µs (750 ns)
- 4 µs (3 µs) multiply and divide
- External memory expandable up to 128 Kbytes
- Backwardly compatible with SAB 8051
- Two temperature ranges available:
  0 to 70 °C
  – 40 to 85 °C (T40/85)

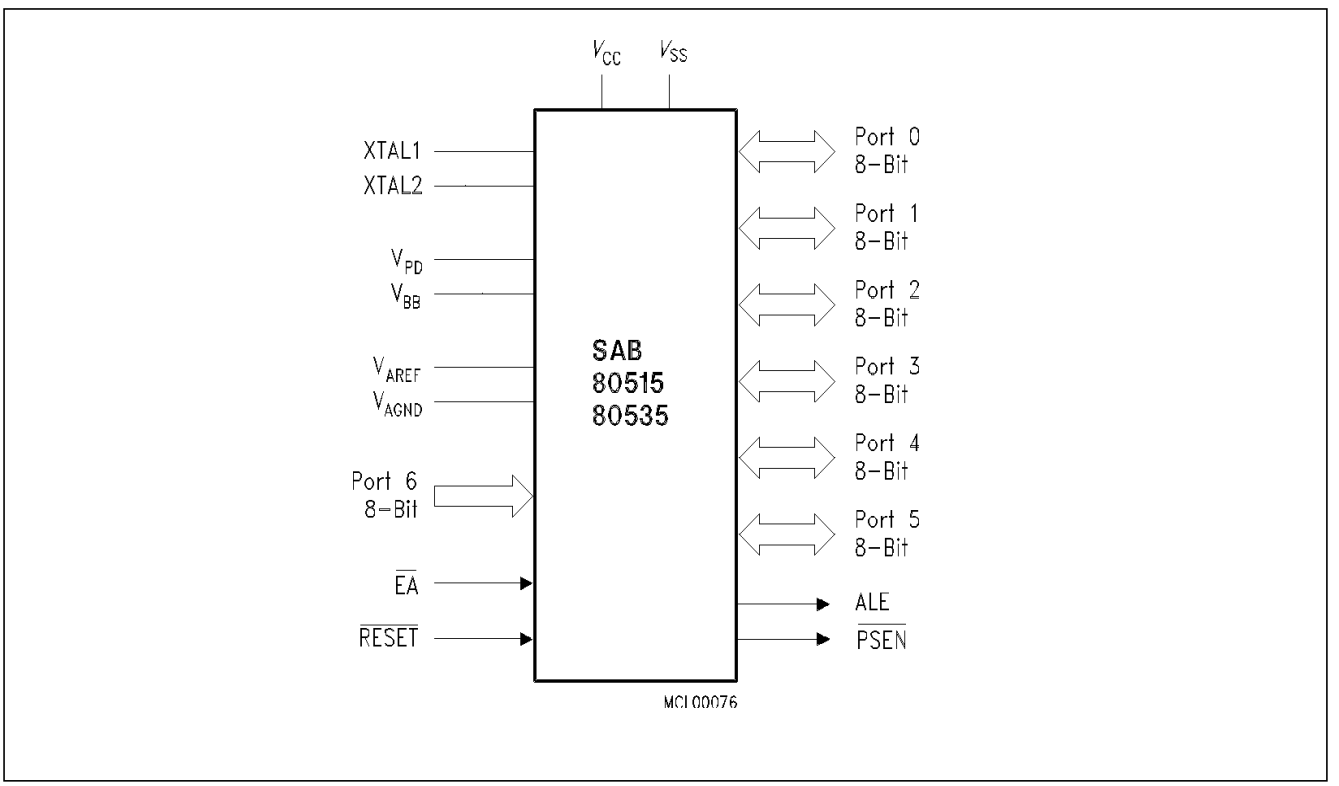
The SAB 80515/80535 is a powerful member of the Siemens SAB 8051 family of 8-bit microcontrollers. It is fabricated in + 5 V N-channel, silicon-gate Siemens MYMOS technology. The SAB 80515/80535 is a stand-alone, high-performance single-chip microcontroller based on the SAB 8051 architecture. While maintaining all the SAB 8051 operating characteristics, the SAB 80515/80535 incorporates several enhancements which significantly increase design flexibility and overall system performance.
The SAB 80535 is identical with the SAB 80515 except that it lacks the on-chip program memory. The SAB 80515/80535 is supplied in a 68-pin plastic leaded chip carrier package (P-LCC-68).



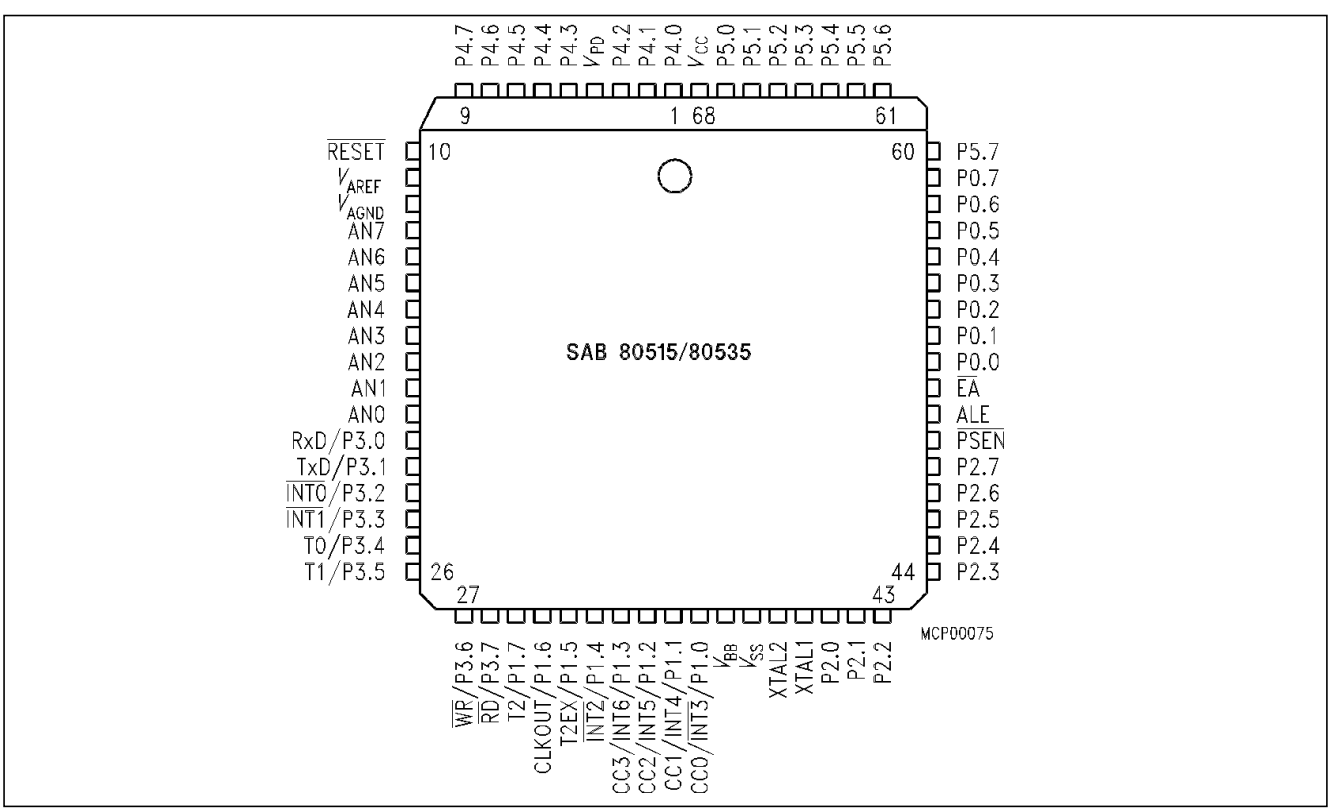
Ordering Information

Type	Ordering code	Package	Description 8-bit CMOS microcontroller
SAB 80515-N	Q 67120-C211	P-LCC-68	with mask-programmable ROM
SAB 80535-N	Q 67120-C241	P-LCC-68	for external memory
SAB 80515-N-T40/85	Q 67120-C210	P-LCC-68	with mask-programmable ROM
SAB 80535-N-40/85	Q 67120-C240	P-LCC-68	for external memory

Note: Extended temperature range – 40 to 110 °C on request



Logic Symbol



Pin Configuration
(P-LCC-68)

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	I/O	**Port 4** is an 8-bit quasi-bidirectional I/O port . Port 4 can sink/source 4 LS-TTL loads.
V_{PD}	4	I	Power down supply. If V_{PD} is held within its specs while V_{CC} drops below specs, V_{PD} will provide standby power to 40 byte of the internal RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
$\overline{\text{RESET}}$	10	I	A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80C515. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}
V_{AREF}	11		Reference voltage for the A/D converter
V_{AGND}	12		Reference ground for the A/D converter
AN7-AN0	13-20	I	Multiplexed analog inputs

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P3.0-P3.7	21-28	I/O	Port 3 is an 8-bit bidirectional I/O. It also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source 4 LS-TTL loads.The secondary functions are assigned to the pins of port 3, as follows: – R × D (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – T × D (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{\text{INT0}}$(P3.2): interrupt 0 input/timer 0 gate control input – $\overline{\text{INT1}}$(P3.3): interrupt 1 input/timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{\text{WR}}$(P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{\text{RD}}$ (P3.7): the read control signal enables the external data memory to port 0

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P1.7 - P1.0	29 - 36	I/O	Port 1 is an 8-bit bidirectional I/O port .It is used for the low-order address byte during program verification. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows: – $\overline{\text{INT3}}$/CC0 (P1.0): interrupt 3 input / compare 0 output / capture 0 input – INT4/CC1 (P1.1): interrupt 4 input / compare 1 output / capture 1 input – INT5/CC2 (P1.2): interrupt 5 input / compare 2 output / capture 2 input – INT6/CC3 (P1.3): interrupt 6 input / compare 3 output / capture 3 input – $\overline{\text{INT2}}$(P1.4): interrupt 2 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input
V_{BB}	37		Substrate pin. Must be connected to V_{SS} through a capacitor (47 to 100 nF) for proper operation of the A/D converter.
XTAL2	39	–	XTAL2 is the output from the oscillator's amplifier.Input to the internal timing circuitry. A crystal, ceramic resonator, or external source can be used.
XTAL1	40	–	XTAL1 is the input to the oscillator's high gain amplifier. Required when a crystal or ceramic resonator is used. Connect to V_{SS} when external source is used on XTAL2.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P2.0-P2.7	41- 48	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source 4 LS-TTL loads.
$\overline{\text{PSEN}}$	49	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution.
ALE	50	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{\text{EA}}$	51	I	When held at a TTL high level, the SAB 80515 executes instructions from the internal ROM when the PC is less than 8192. When held at a TTL low level, the SAB 80515 fetches all instructions from external program memory. For the SAB 80535 this pin must be tied low.
P0.0-P0.7	52-59	I/O	Port 0 is an 8-bit open-drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source 8 LS-TTL loads.
P5.7-P5.0	60-67	I/O	Port 5 is an 8-bit quasi-bidirectional I/O port. Port 5 can sink/source 4 LS-TTL loads.
V_{CC}	68		POWER SUPPLY (+ 5 V power supply during normal operation and program verification)
V_{SS}	38		GROUND (0 V)

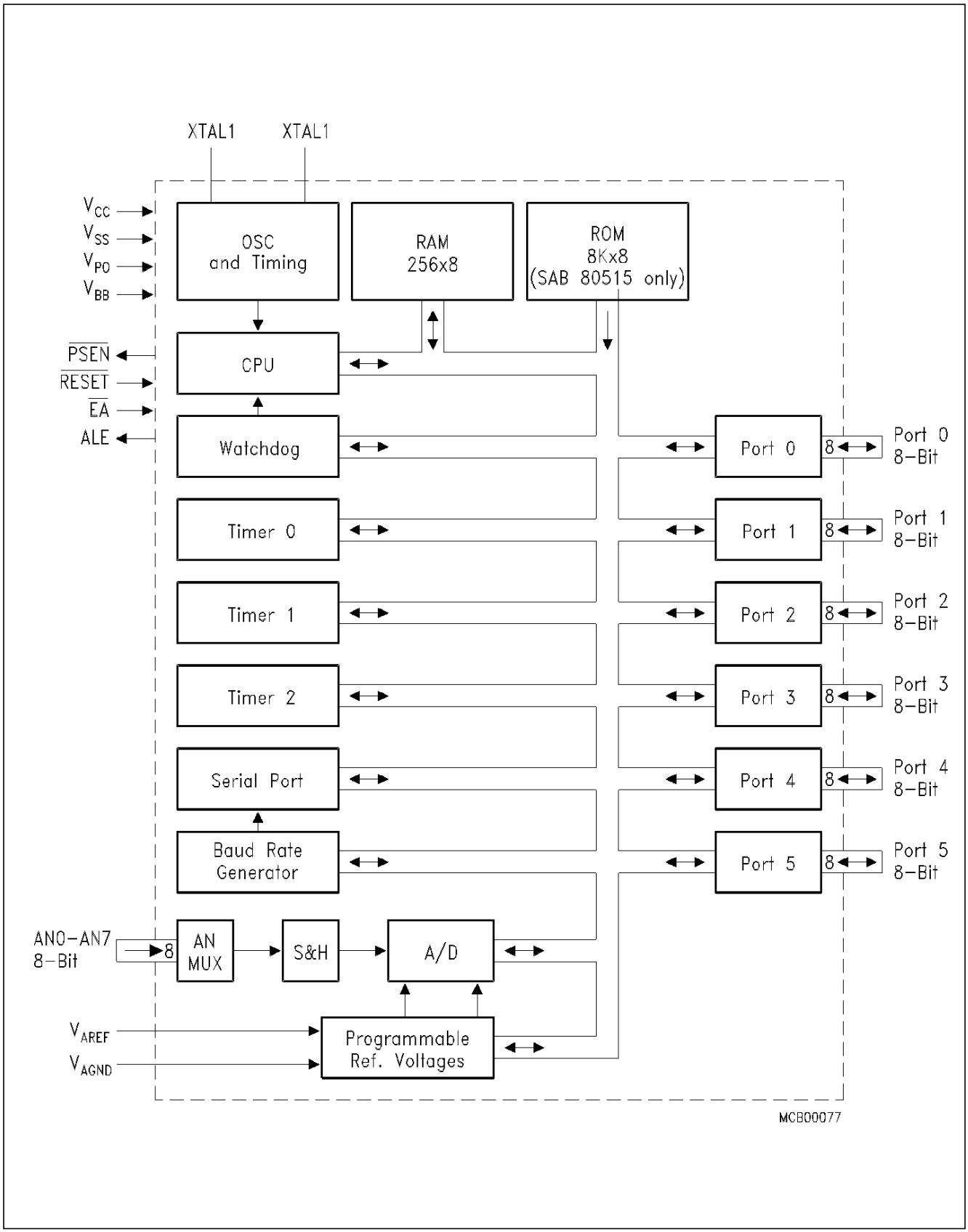


Figure 1
Block Diagram

Functional Description

The architecture of the SAB 80515 is based on the SAB 8051 microcontroller family. The following features of the SAB 80515 are fully compatible with the SAB 8051 features:

- Instruction set
- External memory expansion interface (port 0 and port 2)
- Full-duplex serial port
- Timer/counter 0 and 1
- Alternate functions on port 3
- The lower 128 bytes of internal RAM and the lower 4 Kbytes of internal ROM

The SAB 80515 additionally contains 128 bytes of internal RAM and 4 Kbytes of internal ROM, which results in a total of 256 bytes of RAM and 8 Kbytes of ROM on chip. The SAB 80515 has a new 16-bit timer/counter with a 2:1 prescaler, reload mode, compare and capture capability. It also contains a 16-bit watchdog timer, an 8-bit A/D converter with programmable reference voltages, two additional quasi-bidirectional 8-bit ports, one 8-bit input port for analog signals, and a programmable clock output ($f_{OSC}/12$).
Furthermore, the SAB 80515 has a powerful interrupt structure with 12 vectors and 4 programmable priority levels.
Figure 1 shows a block diagram of the SAB 80515.

CPU

The SAB 80515 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1.0 µs.

Memory Organization

The SAB 80515 manipulates operands in the four memory address spaces described in the following. (Figure 2 illustrates the memory address spaces of the SAB 80515).

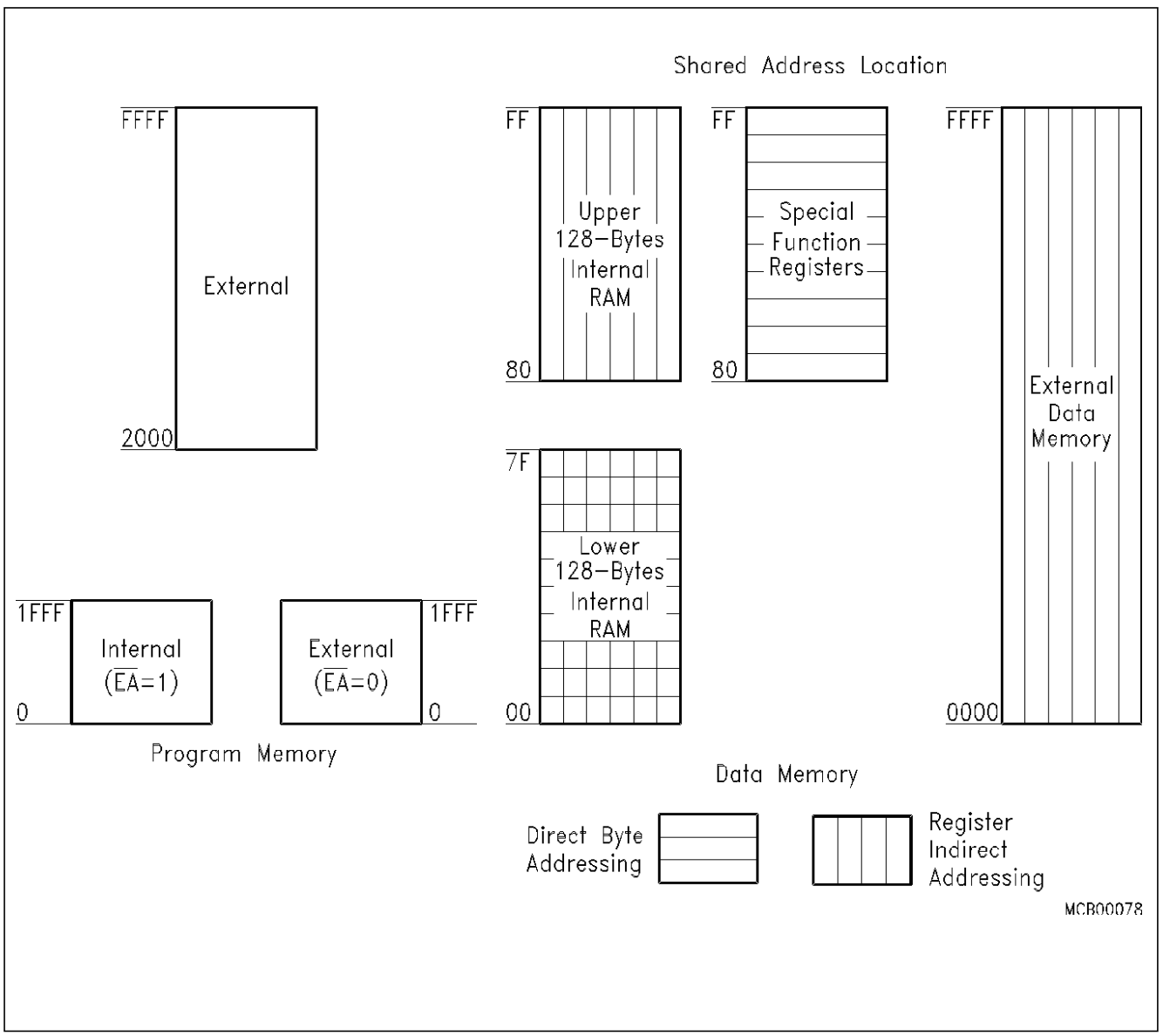


Figure 2
Memory Address Spaces

Program memory

The SAB 80515 has 8 Kbyte of on-chip ROM, while the SAB 80535 has no internal ROM. The program memory can be externally expanded up to 64 Kbytes. If the $\overline{EA}$ pin is held high, the SAB 80515 executes out of internal ROM unless the address exceeds 1FFFH. Locations 2000H through 0FFFFH are then fetched from the external program memory. If the $\overline{EA}$ pin is held low, the SAB 80515 fetches all instructions from the external program memory. Since the SAB 80535 has no internal ROM, pin $\overline{EA}$ must be tied low when using this component.

Data Memory

The data memory address space consists of an internal and an external memory space. The internal data memory is divided into three physically separate and distinct blocks: the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128-byte special function register (SFR) area. While the upper 128 bytes of data memory and the SFR area share the same address locations, they are accessed through different addressing modes. The lower 128 bytes of data memory can be accessed through direct or register indirect addressing; the upper 128 bytes of RAM can be accessed through register indirect addressing; the special function registers are accessible through direct addressing.
Four 8-register banks, each bank consisting of eight 8-bit multi-purpose registers, occupy locations 0 through 1FH in the lower RAM area. The next 16 bytes, locations 20H through 2FH, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal data memory address space, and the stack depth can be expanded up to 256 bytes.
The external data memory can be expanded up to 64 Kbytes and can be accessed by instructions that use a 16-bit or an 8-bit address.

Special Function Registers

All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 41 special function registers (SFR's) include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in the following table:

In table 1 they are organized in numeric order of their addresses. In table 2 they are organized in groups which refer to the functional blocks of the SAB 80515/80535.

Table 1
Special Function Register

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80H	**P0** [1]	**0FFH**	**98H**	**SCON** [1]	**00H**
81H	SP	07H	99H	SBUF	XXXX XXXX B
82H	DPL	00H	9AH	reserved	XXH [2]
83H	DPH	00H	9BH	reserved	XXH [2]
84H	reserved	XXH [2]	9CH	reserved	XXH [2]
85H	reserved	XXH [2]	9DH	reserved	XXH [2]
86H	reserved	XXH [2]	9EH	reserved	XXH [2]
87H	PCON	000X 0000B [2]	9FH	reserved	XXH [2]
88H	**TCON** [1]	**00H**	**A0H**	**P2** [1]	**0FFH**
89H	TMOD	00H	A1H	reserved	XXH [2]
8AH	TL0	00H	A2H	reserved	XXH [2]
8BH	TL1	00H	A3H	reserved	XXH [2]
8CH	TH0	00H	A4H	reserved	XXH [2]
8DH	TH1	00H	A5H	reserved	XXH [2]
8EH	reserved	XXH [2]	A6H	reserved	XXH [2]
8FH	reserved	XXH [2]	A7H	reserved	XXH [2]
90H	**P1** [1]	**0FFH**	**A8H**	**IEN0** [1]	**00H**
91H	reserved	XXH [2]	A9H	IP0	X000 0000B [2]
92H	reserved	XXH [2]	AAH	reserved	XXH [2]
93H	reserved	XXH [2]	ABH	reserved	XXH [2]
94H	reserved	XXH [2]	ACH	reserved	XXH [2]
95H	reserved	XXH [2]	ADH	reserved	XXH [2]
96H	reserved	XXH [2]	AEH	reserved	XXH [2]
97H	reserved	XXH [2]	AFH	reserved	XXH [2]

[1] Bit-addressable Special Function Register
[2] X means that the value is indeterminate and the location is reserved

Table 1
Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
B0H	**P3**[1]	**0FFH**	**D0H**	**PSW** [1]	**00H**
B1H	reserved	XXH[2]	D1H	reserved	XXH [2]
B2H	reserved	XXH[2]	D2H	reserved	XXH [2]
B3H	reserved	XXH[2]	D3H	reserved	XXH [2]
B4H	reserved	XXH[2]	D4H	reserved	XXH [2]
B5H	reserved	XXH[2]	D5H	reserved	XXH [2]
B6H	reserved	XXH[2]	D6H	reserved	XXH [2]
B7H	reserved	XXH[2]	D7H	reserved	XXH [2]
B8H	**IEN1** [1]	**00H**	**D8H**	**ADCON**	**00X0 0000 B** [2]
B9H	IP1	XX00 0000B [2]	D9H	ADDAT	00H
BAH	reserved	XXH [2]	DAH	DAPR	00H
BBH	reserved	XXH [2]	DBH	P6	
BCH	reserved	XXH [2]	DCH	reserved	XXH [2]
BDH	reserved	XXH [2]	DDH	reserved	XXH [2]
BEH	reserved	XXH [2]	DEH	reserved	XXH [2]
BFH	reserved	XXH [2]	DFH	reserved	XXH [2]
C0H	**IRCON** [1]	**00H**	**E0H**	**ACC** [1]	**00H**
C1H	CCEN	00H	E1H	reserved	XXH [2]
C2H	CCL1	00H	E2H	reserved	XXH [2]
C3H	CCH1	00H	E3H	reserved	XXH [2]
C4H	CCL2	00H	E4H	reserved	XXH [2]
C5H	CCH2	00H	E5H	reserved	XXH [2]
C6H	CCL3	00H	E6H	reserved	XXH [2]
C7H	CCH3	00H	E7H	reserved	XXH [2]
C8H	**T2CON** [1]	**00H**	**E8H**	**P4** [1]	**0FFH**
C9H	reserved	XXH [2]	E9H	reserved	XXH [2]
CAH	CRCL	00H	EAH	reserved	XXH [2]
CBH	CRCH	00H	EBH	reserved	XXH [2]
CCH	TL2	00H	ECH	reserved	XXH [2]
CDH	TH2	00H	EDH	reserved	XXH [2]
CEH	reserved	XXH [2]	EEH	reserved	XXH [2]
CFH	reserved	XXH [2]	EFH	reserved	XXH [2]

[1] Bit-addressable Special Function Register
[2] X means that the value is indeterminate and the location is reserved

Table 1
Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
F0H	**B**[1)]	**00H**	**F8H**	**P5** [1)]	**0FFH**
F1H	reserved	XXH[2)]	F9H	reserved	XXH[2)]
F2H	reserved	XXH[2)]	FAH	reserved	XXH[2)]
F3H	reserved	XXH[2)]	FBH	reserved	XXH[2)]
F4H	reserved	XXH[2)]	FCH	reserved	XXH[2)]
F5H	reserved	XXH[2)]	FDH	reserved	XXH[2)]
F6H	reserved	XXH[2)]	FEH	reserved	XXH[2)]
F7H	reserved	XXH[2)]	FFH	reserved	XXH[2)]

[1)] Bit-addressable Special Function Register
[2)] X means that the value is indeterminate and the location is reserved

Table 2
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumululator	**0E0H** 1)	00H
	B	B-Register	**0F0H** 1)	00H
	DPH	Data Pointer, High Byte	083H	00H
	DPL	Data Pointer, Low Byte	082H	00H
	PSW	Program Status Word Register	**0D0H** 1)	00H
	SP	Stack Pointer	081H	07H
A/D-Converter	ADCON 2)	A/D Converter Control Register	**0D8H** 1)	00X0 0000 B 3)
	ADDAT	A/D Converter Data Register	09DH	00H
	DAPR	A/D Converter Program Register	0DAH	00H)
Interrupt System	IEN0 2)	Interrupt Enable Register 0	**0A8H** 1)	00H
	IEN1 2)	Interrupt Enable Register 1	**0B8H** 1)	00H
	IP0 2)	Interrupt Priority Register 0	0A9H	X000 0000 B 3)
	IP1	Interrupt Priority Register 1	0B9H	XX00 0000 B 3)
	IRCON	Interrupt Request Control Register	**0C0H** 1)	00H
	TCON 2)	Timer Control Register	**88H** 1)	00H
	T2CON 2)	Timer 2 Control Register	**0C8H** 1	00H
Compare/ Capture-Unit Compare/ Capture-Unit (CCU) (cont'd) (CCU)	CCEN	Comp./Capture Enable Reg.	0C1H	00H
	CCH1	Comp./Capture Reg. 1, High Byte	0C3H	00H
	CCH2	Comp./Capture Reg. 2, High Byte	0C5H	00H
	CCH3	Comp./Capture Reg. 3, High Byte	0C7H	00H
	CCL1	Comp./Capture Reg. 1, Low Byte	0C2H	00H
	CCL2	Comp./Capture Reg. 2. Low Byte	0C4H	00H
	CCL3	Comp./Capture Reg. 3, Low Byte	0C6H	00H
	CRCH	Com./Rel./Capt. Reg. High Byte	0CBH	00H
	CRCL	Com./Rel./Capt. Reg. Low Byte	0CAH	00H
	TH2	Timer 2, High Byte	0CDH	00H
	TL2	Timer 2, Low Byte	0CCH	00H
	T2CON 2)	Timer 2 Control Register 1)	**0C8H** 1)	00H

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks
3) X means that the value is indeterminate

Table 2
Special Function Registers- Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Ports	P0	Port 0	**80H** 1)	0FFH
	P1	Port 1	**90H** 1)	0FFH
	P2	Port 2	**0A0H** 1)	0FFH
	P3	Port 3	**0B0H** 1)	0FFH
	P4	Port 4	**0E8H** 1)	0FFH
	P5	Port 5	**0F8H** 1)	0FFH
	P6	Port 6, Analog/Digital Input	0DBH	
Pow. Sav. Modes	PCON 2)	Power Control Register	087H	000X 0000 B 2)
Serial Channels	ADCON 2)	A/D Converter Control Reg.	**0D8H** 1)	00X0 0000 B 3)
	PCON 2)	Power Control Register	087H	000X 0000 B 3)
	SBUF	Serial Channel Buffer Reg.	099H	XXXX XXXX B 3)
	SCON	Serial Channel Control Reg.	**098H** 1)	00H
Timer 0/ Timer 1	TCON 2)	Timer Control Register	0**88H**1)	00H
	TH0	Timer 0. High Byte	08CH	00H
	TH1	Timer 1, High Byte	08DH	00H
	TL0	Timer 0, Low Byte	08AH	00H
	TL1	Timer 1, Low Byte	08BH	00H
	TMOD	TImer Mode Register	089H	00H
Watchdog	IEN0 2)	Interrupt Enable Register 0	**0A8H** 1)	00H
	IEN1 2)	Interrupt Enable Register 1	**0B8H** 1)	00H
	IP0 2)	Interrupt Priority Register 0	0A9H	X000 0000 B 3)

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) X means that the value is indeterminate and the location is reserved

Serial Port

The serial port of the SAB 80515 enables full duplex communication between microcontrollers or between microcontroller and peripheral devices. The serial port can operate in 4 modes:

Mode 0: Shift register mode. Serial data enters and exits through R×D. T×D outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 10 bits are transmitted (through R×D) or received (through T×D): a start bit (0), 8 data bits (LSB first), and a stop bit (1). The baud rate is variable.

Mode 2: 11 bits are transmitted (through R×D) or received (through T×D): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 11 bits are transmitted (through T×D) or received (through R×D): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is identical to mode 2 except for the baud rate. The baud rate in mode 3 is variable.

The variable baud rates in modes 1 and 3 can be generated by timer 1 or an internal baud rate generator.

A/D Converter

The 8-bit A/D converter of the SAB 80515 has eight multiplexed analog inputs (Port 6) and uses the successive approximation method.
It takes 5 machine cycles to sample an analog signal (during this sample time the input signal should be held constant); the total conversion time (including sample time) is 15 machine cycles (15 µs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous; at the end of a conversion an interrupt can be generated.

A unique feature is the capability of internal reference voltage programming. The internal reference voltages V_{IntAREF} and V_{IntAGND} for the A/D converter both are programmable to one of 16 steps with respect to the external reference voltages. This feature permits a conversion with a smaller internal reference voltage range to gain a higher resolution. In addition, the internal reference voltages can easily be adapted by software to the desired analog input voltage range.

Figure 3 shows a block diagram of the A/D converter.

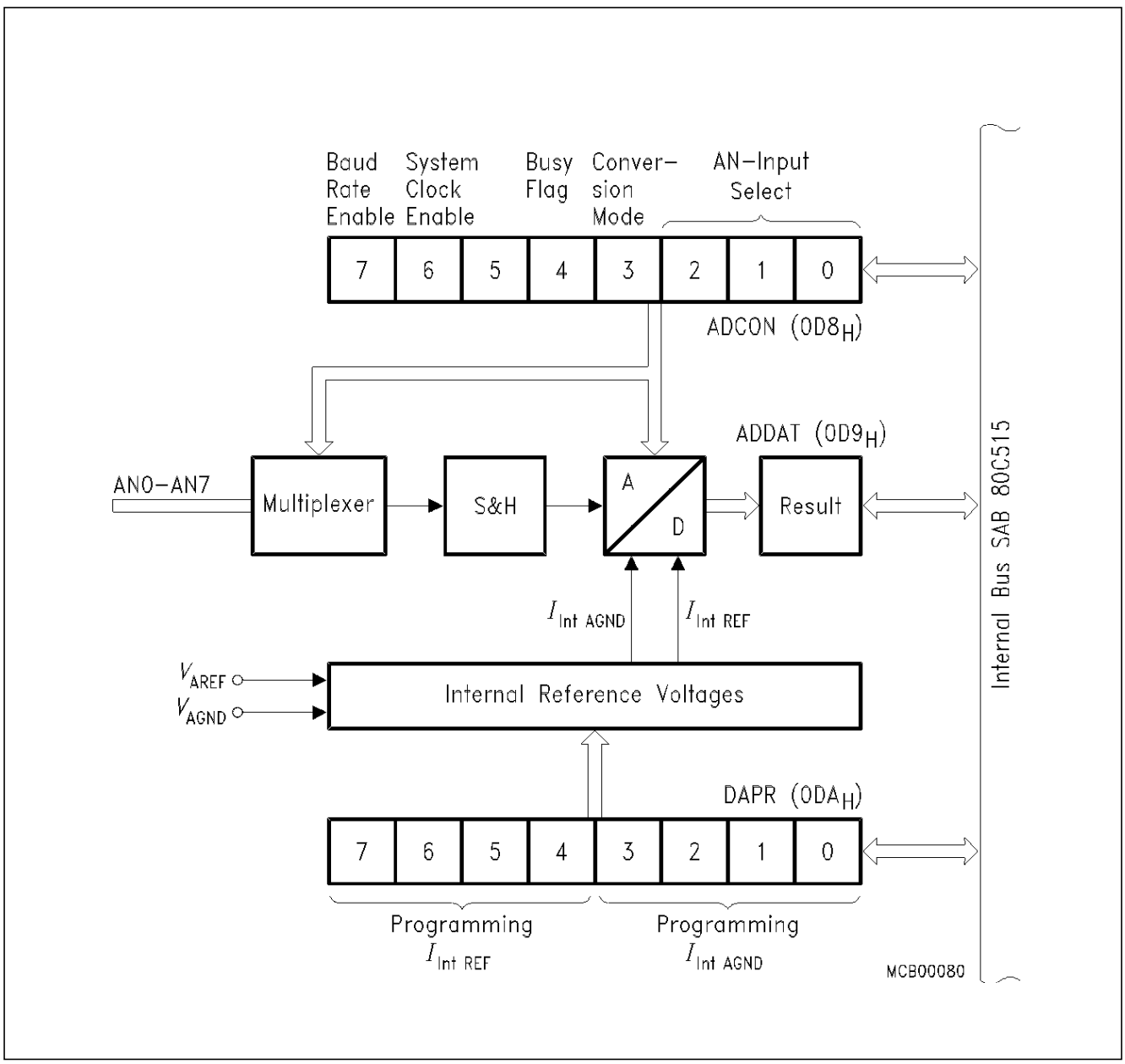


Figure 3
Block Diagram of the A/D Converter

Timer/Counters

The SAB 80515 contains three 16-bit timer/counters which are useful in many applications for timing and counting. The input clock for each timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

– Timer/counter 0 and 1

These timer/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto-reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; timer/counter 1 in this mode holds its count.

External inputs $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

– Timer/counter 2

Timer/counter 2 of the SAB 80515 is a 16-bit timer/counter with several additional features. It offers a 2:1 prescaler, a selectable gate function, and compare, capture and reload functions. Corresponding to the 16-bit timer register there are four 16-bit capture/compare registers, one of them can be used to perform a 16-bit reload on a timer overflow or external event. Each of these registers corresponds to a pin of port 1 for capture input/compare output.
Figure 4 shows a block diagram of the timer/counter 2.

Reload

A 16-bit reload can be performed with the 16-bit CRC register, which is a concatenation of the 8-bit registers CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer 2 overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

Capture

This feature permits saving the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value in timer 2 registers into a dedicated capture register:

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 registers. If the count value in the timer 2 registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to a low level when timer 2 overflows.

Mode 1: The transition of the output signal can be determined by software. A timer 2 overflow causes no output change.

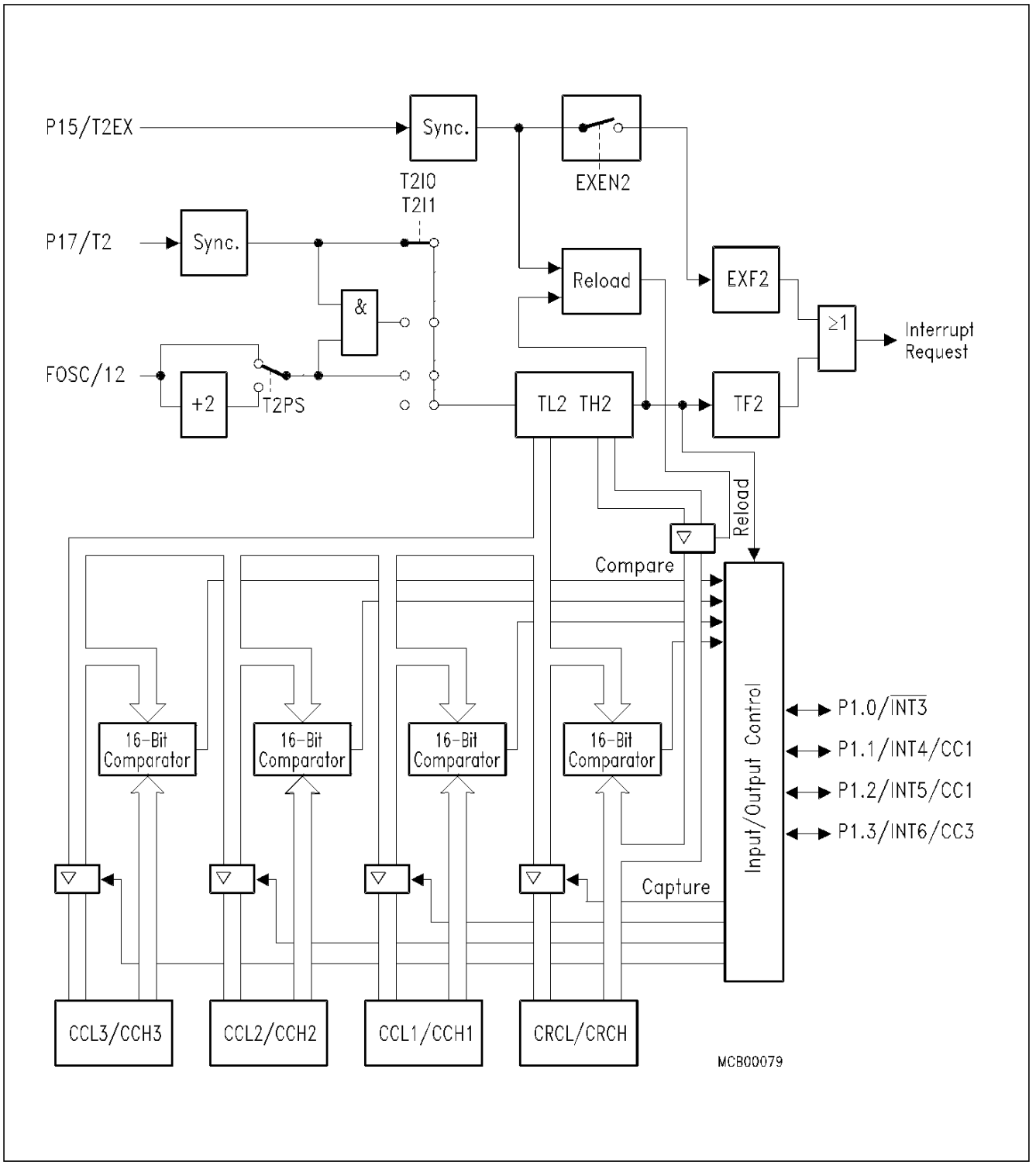


Figure 4
Block Diagram of Timer/Counter 2

Interrupt Structure

The SAB 80515 has 12 interrupt vectors with the following vector addresses and request flags:

Table 3
Interrupt Sources and Vectors

Source (Request Flags)	Vector Address	Vector
IE0	0003H	External interrupt 0
TF0	000BH	Timer 0 interrupt
IE1	0013H	External interrupt 1
TF1	001BH	Timer 1 interrupt
RI + TI	0023H	Serial port interrupt
TF2 + EXF2	002BH	Timer 2 interrupt
IADC	0043H	A/D converter interrupt
IEX2	004BH	External interrupt 2
IEX3	0053H	External interrupt 3
IEX4	005BH	External interrupt 4
IEX5	0063H	External interrupt 5
IEX6	006BH	External interrupt 6

Each interrupt vector can be individually enabled/disabled. The minimum response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

Figure 5 shows the interrupt request sources.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 3 to 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs. Each pair can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. Figure 6 shows the priority level structure.

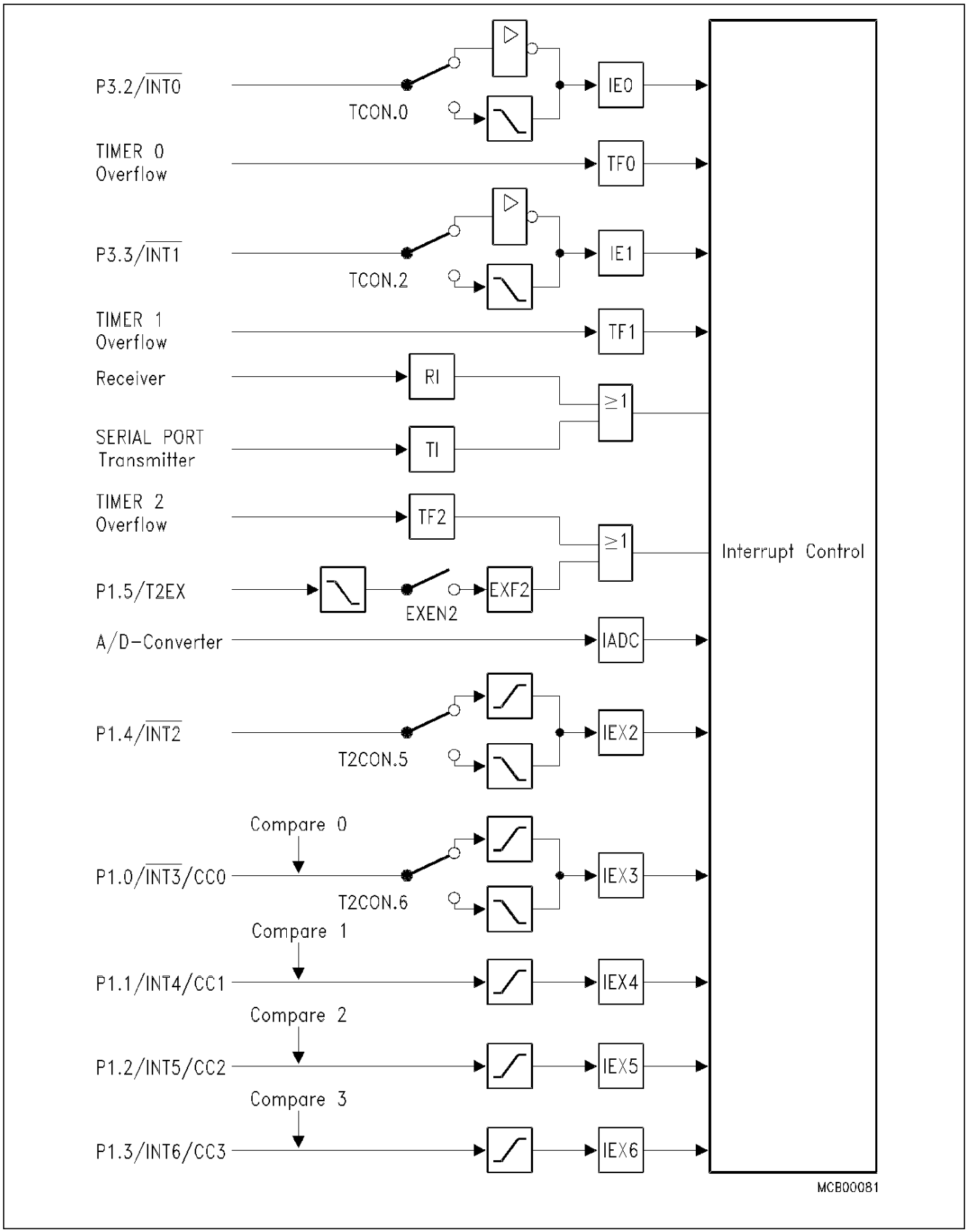


Figure 5
Interrupt Request Sources

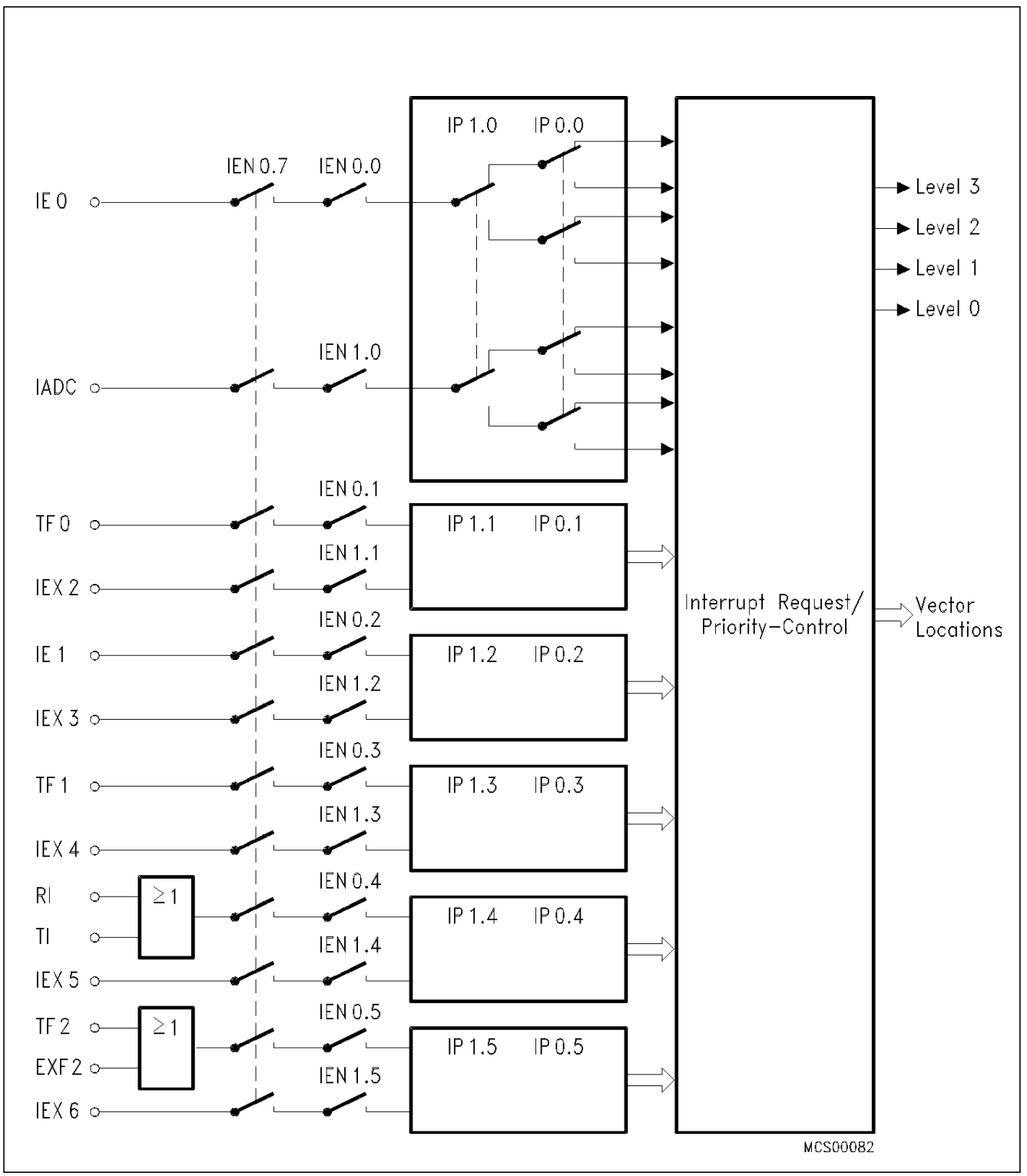


Figure 6
Priority Level Structure

I/O Ports

The SAB 80515 has six 8-bit I/O ports and one 8-bit input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pull-up resistors. That means, when configured as inputs, ports 1 to 5 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.
Ports 1 and 3 are provided for several alternate functions, as listed below:

Port	Symbol	Function
P1.0	$\overline{\text{INT3}}$/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	INT6/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	$\overline{\text{INT2}}$	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external counter input
P3.0	RXD	Serial port's receiver data input (asynchronous) or data input/output (synchronous)
P3.1	TXD	Serial port's transmitter data output (asynchronous) or clock output (synchronous)
P3.2	$\overline{\text{INT0}}$	External interrupt 0 input, timer 0 gate control
P3.3	$\overline{\text{INT1}}$	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	T1	Timer 1 external counter input
P3.6	$\overline{\text{WR}}$	External data memory write strobe
P3.7	$\overline{\text{RD}}$	External data memory read strobe

The input port AN0-AN7 is used for analog input signals to the A/D converter.

Watchdog Timer

This feature is provided as a means of graceful recovery from a software upset. After an external reset, the watchdog timer is cleared and stopped. It can be started and cleared by software, but it cannot be stopped. If the software fails to clear the watchdog timer at least every 65532 machine cycles (about 65 ms if a 12 MHz oscillator frequency is used), an internal hardware reset will be initiated.

The reset cause (external reset or reset caused by the watchdog) can be examined by software. To clear the watchdog, two bits in two different special function registers must be set by two consecutive instructions (bits IEN0.6 and IEN1.6). This is done to prevent the watchdog from being cleared by unexpected opcodes.

Instruction Set Summary

The SAB 80515/80535 has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function Registers, Interrupt Vectors and Assembler Directives.

Literature Information

Title	Ordering No.
Microcontroller Family SAB 8051 Pocket Guide	B158-B6599 - X - X - 7600

Absolute Maximum Ratings

Ambient temperature under bias
SAB 80515/80535 ..... 0 to 70 °C
SAB 80515/80535-T40/85 ..... – 40 to 85 °C
Storage temperature ..... – 65 to 150 °C
Voltage on any pins with respect to ground (V_{SS}) ..... – 0.5 V to 7 V
Power dissipation ..... 2 W

Note *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB 80515/80535
T_A = – 40 to 85 °C for the SAB 80515/80535-T40/85
T_A = – 40 to110 °C for the SAB 80515/80535-T40/110

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input low voltage	V_{IL}	– 0.5	0.8	V	–
Input high voltage) (except $\overline{\text{RESET}}$, XTAL2	V_{IH}	2.0	V_{CC} – 0.5	V	–
Input high voltage to XTAL2	V_{IH1}	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
Input high voltage to $\overline{\text{RESET}}$	V_{IH2}	3.0	–	V	–
Power down voltage	V_{PD}	3	5.5	V	V_{CC} = 0 V
Output low voltage ports 1, 2, 3, 4, 5	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA[1)]
Output low voltage port 0, ALE, $\overline{\text{PSEN}}$	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1)]
Output high voltage ports 1, 2, 3, 4, 5	V_{OH}	2.4	–	V	I_{OH} = – 80 µA
Output high voltage port 0, ALE, $\overline{\text{PSEN}}$	V_{OH1}	2.4	–	V	I_{OH} = – 400 µA

[1)] Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1,3,4,5. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-0 transitions during bus operation.

DC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Logic 0 input current ports 1, 2, 3, 4, 5	I_{IL}	–	– 800	µA	V_{IL} = 0.45 V
Logic 0 input current XTAL2	I_{IL2}	–	– 2.5	mA	XTAL1 = V_{SS} V_{IL} = 0.45 V
Input low current to $\overline{\text{RESET}}$ for reset	I_{IL3}	–	– 500	µA	V_{IL} = 0.45 V
Input leakage current to port 0, $\overline{\text{EA}}$ AN0 - AN7	I_{LI}	–	± 10	µA	0 V < V_{IN} < V_{CC}
Power supply current:[1] SAB 80515/80535 SAB 80515/80535-T40/85 SAB 80515/80535-T40/110	 I_{CC} I_{CC} I_{CC}	 – – –	 210 230 230	 mA mA mA	 all outputs disconnected
Power-down current	I_{PD}	–	3	mA	V_{CC} = 0 V
Capacitance of I/O buffer	C_{IO}	–	10	pF	f_C =1 MHz

[1] Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1,3,4,5. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-0 transitions during bus operation.

A/D Converter Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V; V_{AREF} = V_{CC} ± 5 %; V_{AGND} = V_{SS} ± 0.2 V;
$V_{IntAREF} - V_{IntAGND} \geq 1$ V; T_A = 0 to + 70 °C for SAB 80515/80535
T_A = – 40 to + 85 °C for SAB 80515/80535 - T40/85

Parameter	Symbol	Limit values			Unit	Test condition
		min.	typ.	max.		
Analog input voltage	V_{AINPUT}	V_{AGND}- 0.2	–	V_{AREF}+ 0.2	V	–
Analog input capacitance	C_I	–	25	–	pF	1)
Load time	t_L	–	–	2 t_{CY}	µs	–
Sample time (incl. load time)	t_S	–	–	5 t_{CY}	µs	–
Conversion time (including sample time)	t_C	–	–	13 t_{CY}	µs	–
Differential non-linearity Integral non-linearity Offset error Gain error Total unadjusted error	DNLE INLE TUE	–	± 1/2 ± 1/2 ± 1/2 ± 1/2 ± 1	± 1 ± 1 ± 1 ± 1 ± 2	LSB LSB LSB LSB LSB	$V_{IntAREF}$ = V_{AREF} = V_{CC} $V_{IntAGND}$ = V_{AGND} = V_{SS} 2)
V_{AREF} supply current	I_{REF}	–	–	5	mA	2)
Internal reference error	$V_{IntREFER}$	–	± 5	± 30	mV	2)

1) The internal resistance of the analog source must be low enough to assure full loading of the sample capacitance (C_I)during load time (t_L). After charging of the internal capacitance (C_I) in the load time (t_L) the analog input must be held constant for the rest of the sample time (t_S).

2) The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

AC Characteristics

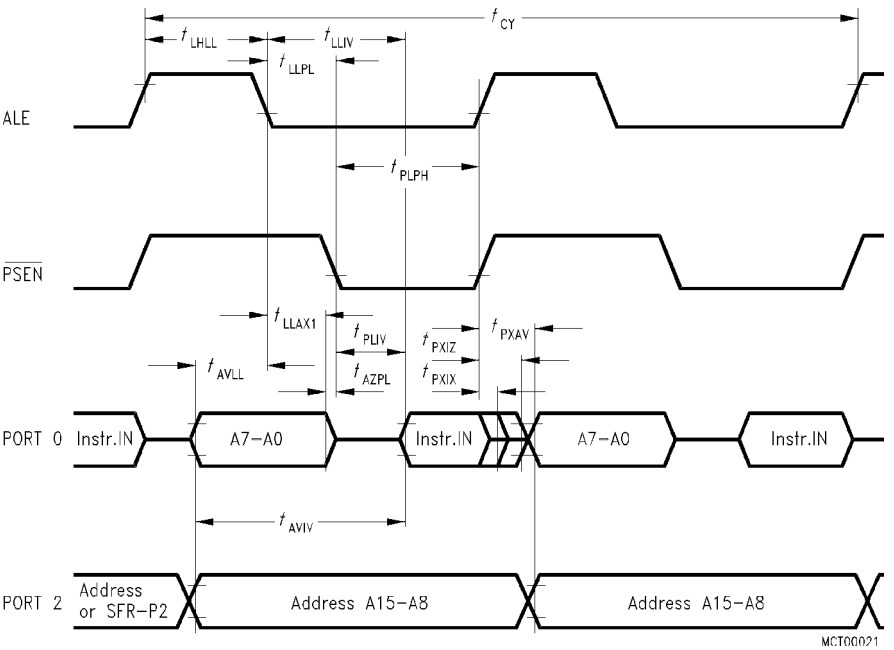
V_{CC} = 5 V ± 10 %; V_{SS} = 0 V; (C_L for port 0, ALE and PSEN outputs = 100 pF; C_L for all other outputs = 80 pF) T_A = 0 to + 70 °C; for SAB 80515/80535
T_A = – 40 to + 85 °C; for SAB 80515/80535 - 40/85

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min	max.	min.	max.	
Program Memory Characteristics						
Cycle Time	t_{CY}	1000	–	12 t_{CLCL}	–	ns
ALE pulse width	t_{LHLL}	127	–	2 t_{CLCL} – 40	–	ns
Address setup to ALE	t_{AVLL}	53	–	t_{CLCL} – 30	–	ns
Address hold after ALE	t_{LLAX1}	48	–	t_{CLCL} – 35	–	ns
ALE to valid instruction in	t_{LLIV}	–	233	–	4 t_{CLCL} – 100	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	58	–	t_{CLCL} – 25	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	215		3 t_{CLCL} – 35	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	t_{PLIV}	–	150	–	3 t_{CLCL} –100	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	63	–	t_{CLCL} – 20	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	75	–	t_{CLCL} – 8	–	ns
Address to valid instruction in	t_{AVIV}	–	302	–	5 t_{CLCL} – 115	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	–	0	–	ns

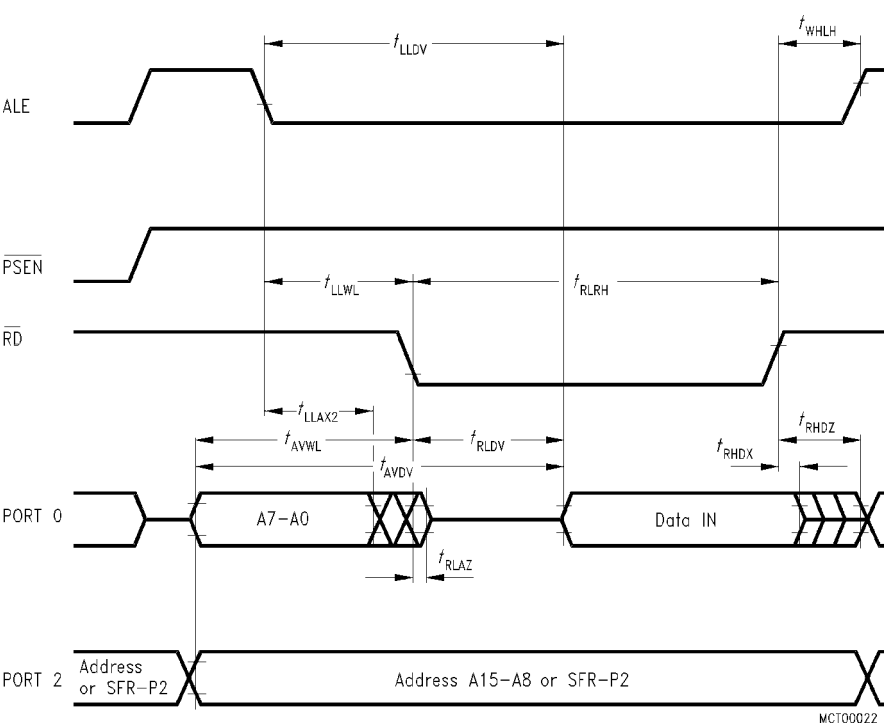
*) Interfacing the SAB 805156 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

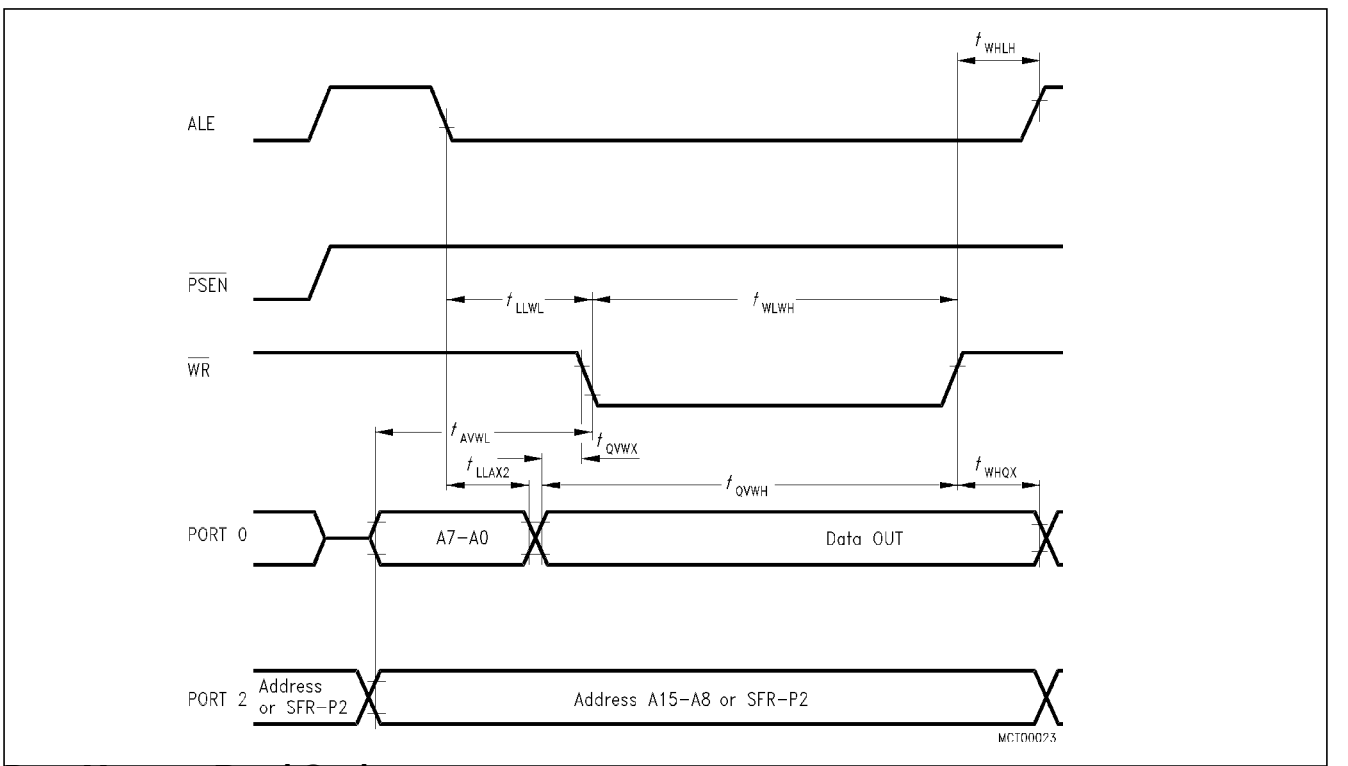
Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	400	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	132	–	2 t_{CLCL} – 35	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	5 t_{CLCL} – 165	ns
DATA hold after $\overline{RD}$	t_{RHDX}	0	–	0		ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	2 t_{CLCL} – 70	ns
ALE to valid data in	t_{LLDV}	–	517	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	585	–	9 t_{nCLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
Address to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	–	4 t_{CLCL} – 130	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	t_{CLCL} – 40	t_{CLCL} + 40	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	t_{CLCL} – 50	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	t_{CLCL} – 50	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

Waveforms

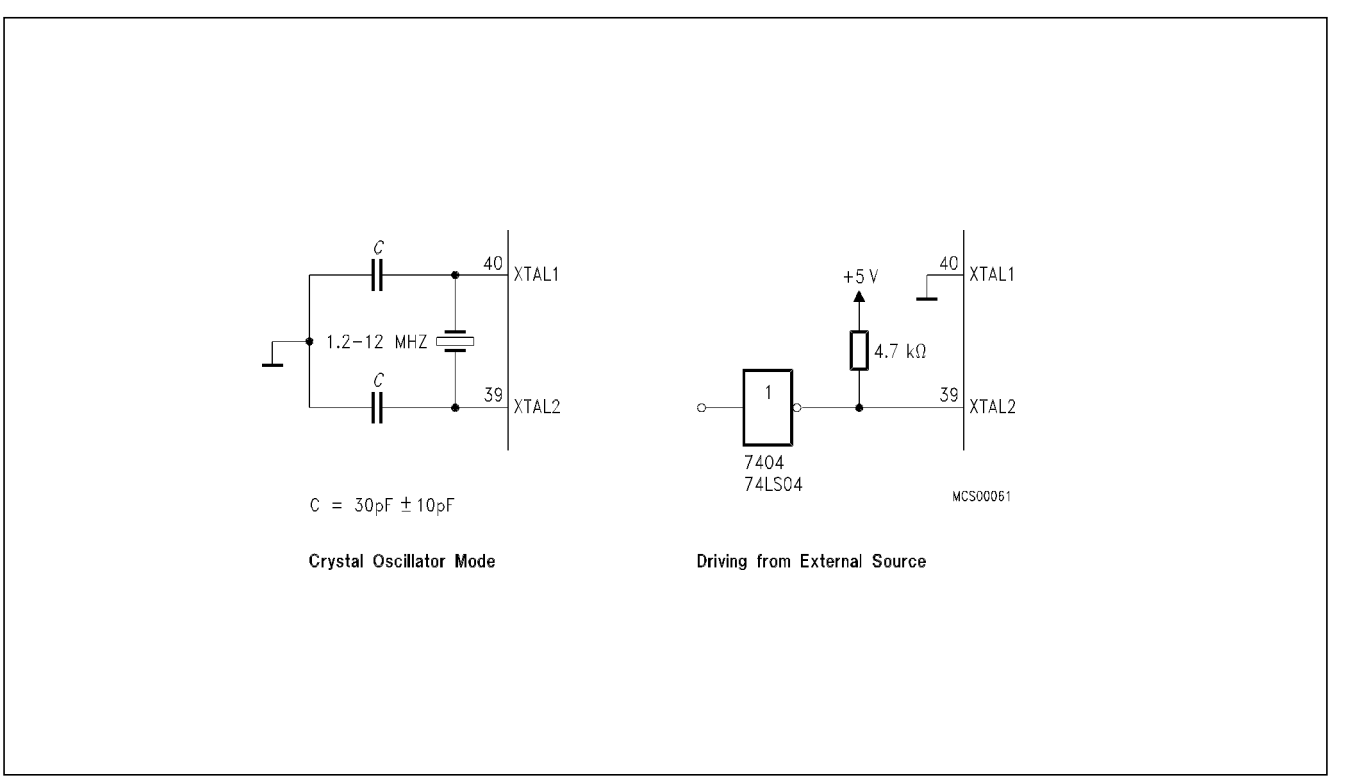


Program Memory Read Cycle





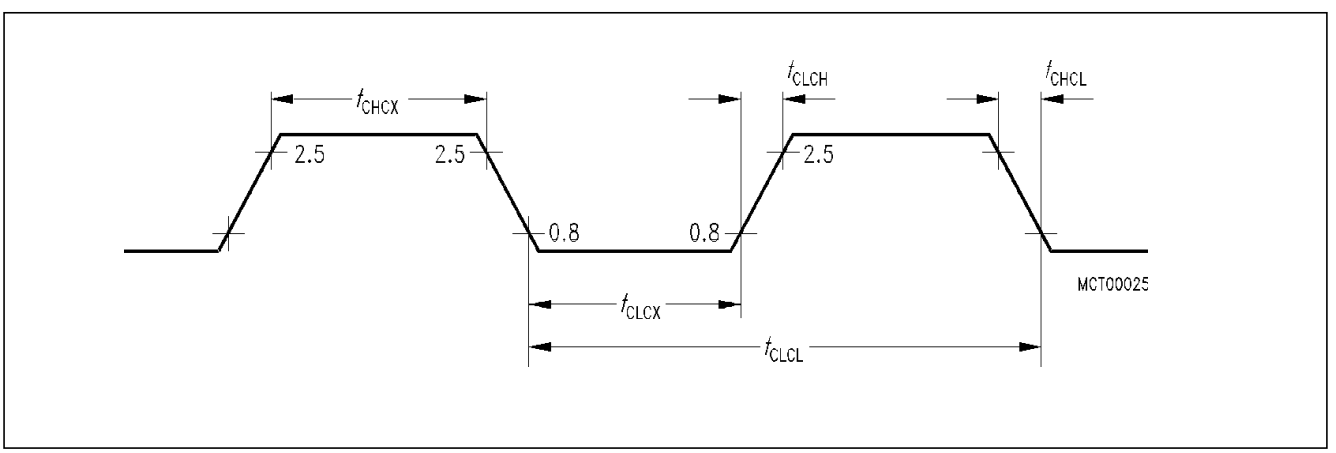
Data Memory Read Cycle



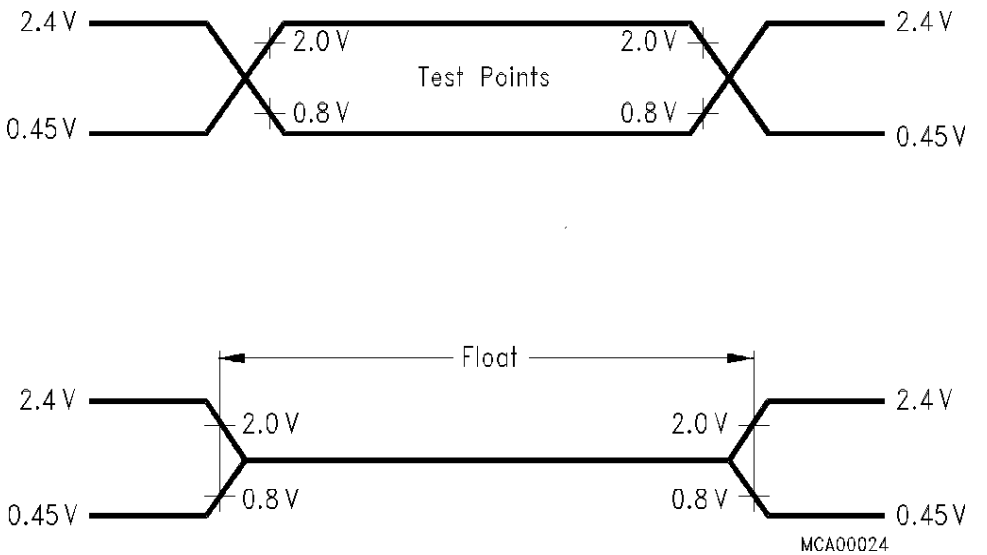
Recommended Oscillator Circuits

AC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 1.2 MHz to 12 MHz		
		min.	max.	
External Clock Drive XTAL2				
Oscillator period	t_{CLCL}	83.3	833.3	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns
Oscillator period	t_{CLCL}	83.3	833.3	ns



External Clock Cycle

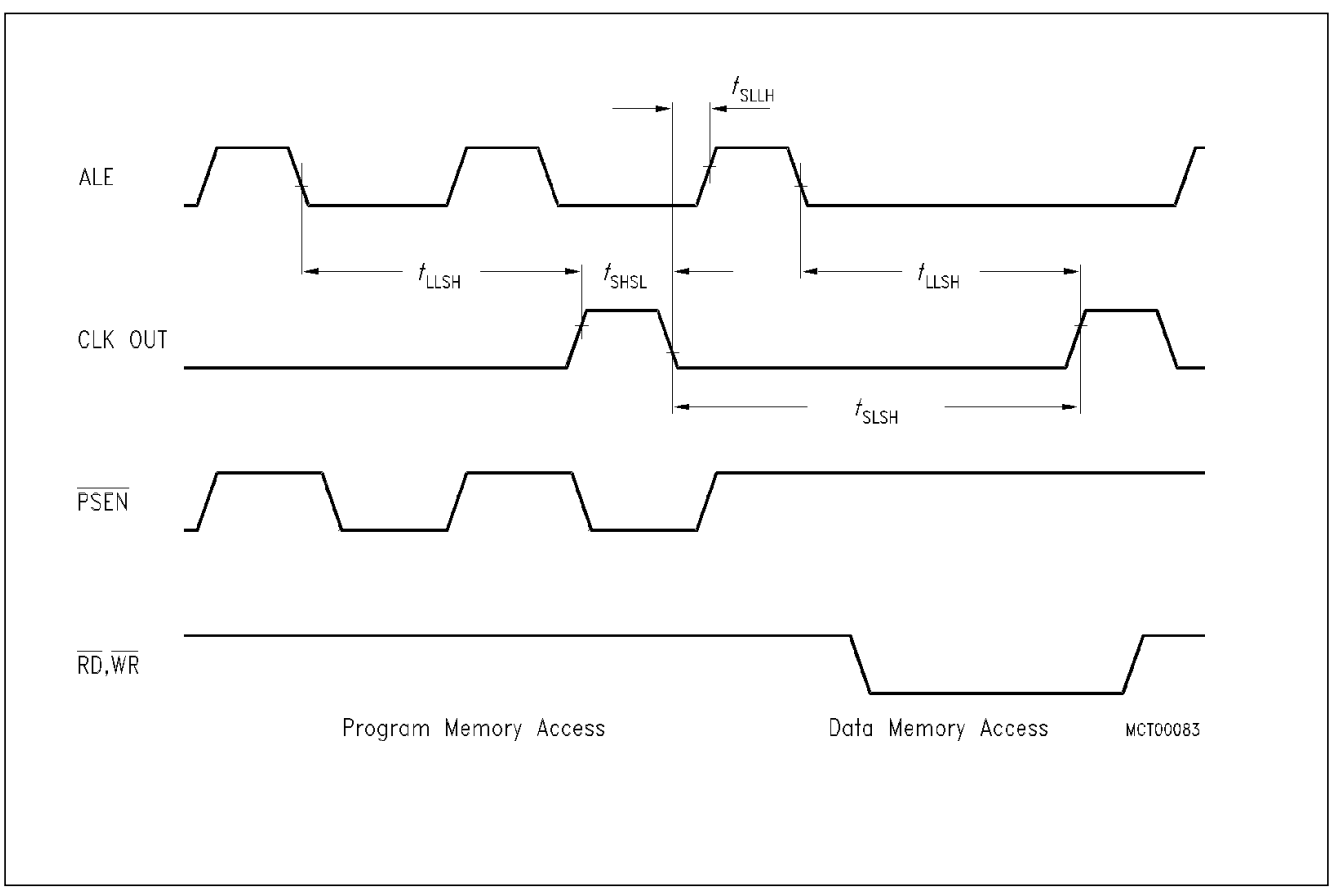


A.C. testing inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels.

A.C. Testing Input, Output, Float Waveforms

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
System Clock Timing						
ALE to CLKOUT	t_{LLSH}	543	–	7 t_{CLCL} – 40	–	ns
CLKOUT high time	t_{SHSL}	127	–	2 t_{CLCL} – 40	–	ns
CLKOUT low time	t_{SLSH}	793	–	10 t_{CLCL} – 40	–	ns
CLKOUT low to ALE high	t_{SLLH}	43	123	t_{CLCL} – 40	t_{CLCL} + 40	ns



System Clock Timing

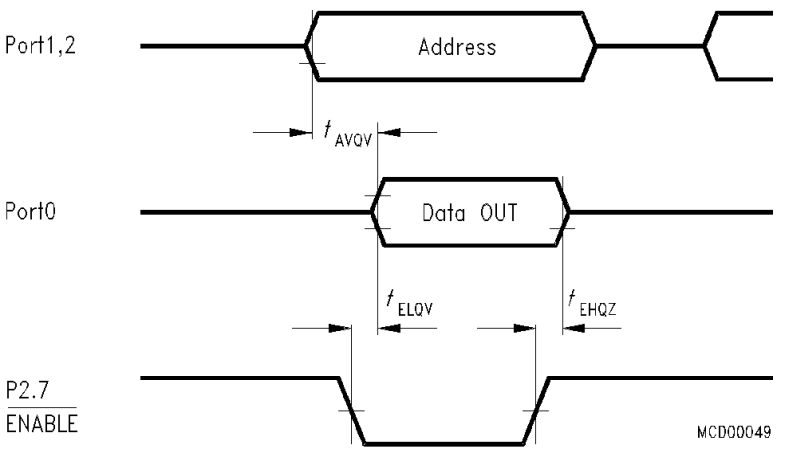
ROM Verification Characteristics

T_A = 25 °C ± 5 °C; V_{CC} = 5 V ± 10 %; V_{SS} = 0 V

Parameter	Symbol	Limit values		Unit
		min	max.	

ROM Verification

Address to valid data	t_{AVQV}	–	48 t_{CLCL1}	ns
ENABLE to valid data	t_{ELQV}	–	48 t_{CLCL1}	ns
Data float after ENABLE	t_{EHOZ}	0	48 t_{CLCL1}	ns
Oscillator frequency	1/t_{CLCL}	4	6	MHz



Address: P1.0–P1.7=A0–A7
P2.0–P2.4=A8–A12
Data: Port 0 =D0–D7

Inputs: P2.5–P2.6, $\overline{PSEN}$=V_{SS}
ALE, $\overline{EA}$= V_{IH}
$\overline{RESET}$ = V_{IL}

Address: P1.0-P1.7 = A0-A7
P2.0-P2.4 = A8-A12

Data: Port 0 = D0-D7

Inputs: P2.5-P2.6, $\overline{PSEN}$ = V_{SS}
ALE, $\overline{EA}$ = V_{IH}
$\overline{RESET}$ = V_{IL}

ROM Verification