CLOCK/TIMER SAF3019P

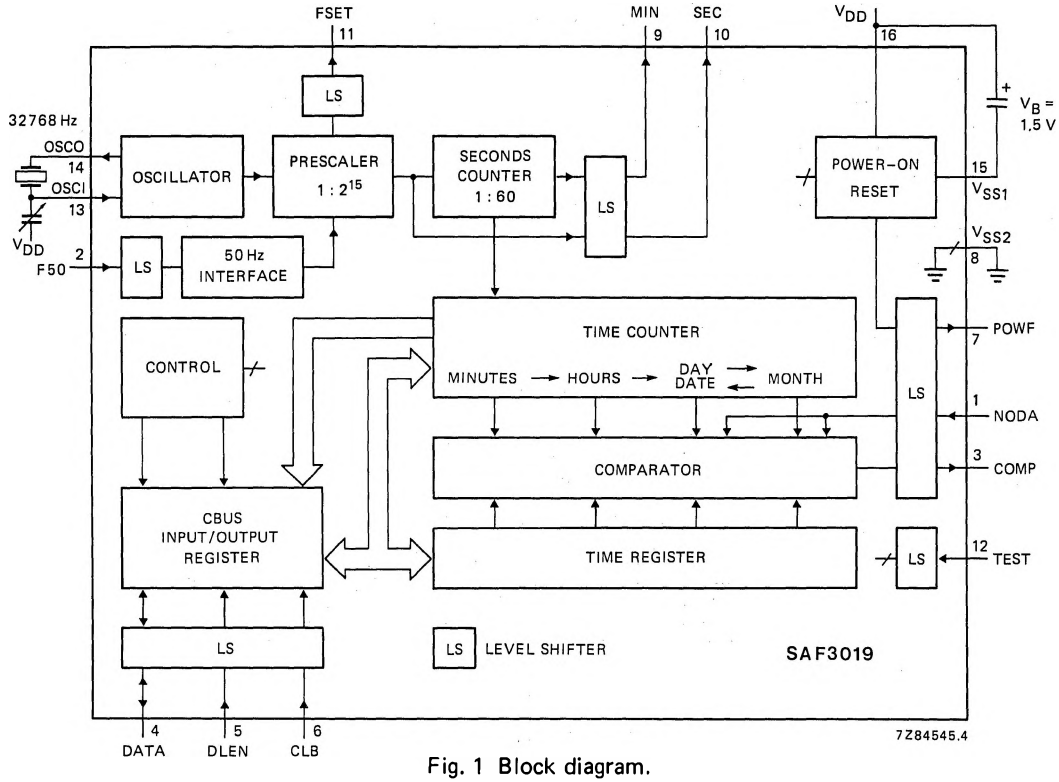

Fig. 1 Block diagram.

Features

- serial bidirectional CBUS interface for input/output of minutes, hours, day and month
- additional pulse outputs for seconds and minutes
- time register for presetting a time for alarm or remote switching functions
- battery back-up for clock function during supply interruption
- controlled either by the 50 Hz mains frequency or a crystal oscillator (automatic switch)

QUICK REFERENCE DATA

Supply voltage		V_{DD}	typ. 5 V
Battery supply voltage range	T_{amb} = −40 to + 85 °C	V_B	1.5 to 2.6 V
	T_{amb} = 0 to + 70 °C	V_B	1.3 to 2.6 V
Crystal oscillator frequency		f_{osc}	typ. 32.768 Hz
Alternative input frequency (pin 2)		f_{F50}	typ. 50 Hz
Operating ambient temperature range		T_{amb}	−40 to + 85 °C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38D, DE).

GENERAL DESCRIPTION

The SAF3019 is a C-MOS integrated circuit comprising a digital clock for minutes, hours, day and month, as well as an additional register for resetting minutes, hours, day and month. The time counter provides cycles of 28, 30 or 31 days automatically, depending on the length of the month.

The time reference is the 50 Hz mains frequency or a 32.768 Hz on-chip reference oscillator with an external crystal. If the 50 Hz mains frequency is interrupted, the circuit is automatically switched to crystal oscillator operation.

The circuit can be controlled by a microcomputer. The data transmission (e.g. TIME SET and TIME READ of the time counter and time register) is achieved via the CBUS. A microcomputer then controls the data processing and the display unit drive.

The circuit uses a 5 V supply for data transmission. If this 5 V supply is interrupted, the clock function is maintained by a 1.5 V battery. The clock can then continue to function for an extended period, because the battery load current is only a few μA.

OPERATION DESCRIPTION

Oscillator and prescaler (outputs OSCO, FSET; inputs OSCI, F50)

The 32.768 Hz reference oscillator is achieved by connecting a quartz crystal between the output OSCO and the input OSCI (see also Fig. 7). The oscillator frequency of 32.768 Hz is divided by 256, and again by 128, in a prescaler. This results in a pulse once every second which controls the time counter. The divided-by-256 oscillator frequency (128 Hz) is available at FSET, which is used for fine-adjustment of the oscillator without loading it.

The circuit can also be operated by applying the 50 Hz mains frequency to input F50. This signal is divided-by-50 to obtain a pulse every second to drive the time counter. Input F50 has a Schmitt trigger characteristic which allows slowly rising pulses at this input.

If the mains frequency is interrupted, automatic quartz crystal operation is obtained (see Fig. 8). When the 50 Hz operation is not used, input F50 should be connected to ground (V_{SS2}).

Time counter (outputs SEC, MIN)

The one-second pulses are counted by a (no direct TIME READ) seconds counter and, after 60 seconds, they are transferred to successive counters for minutes, hours, day and month. This counter can be TIME SET and TIME READ by a microcomputer via the CBUS interface. The cycle length for the time counter is given in Table 1.

The seconds and minutes pulses are avilable at output SEC and MIN respectively, with a pulse ratio of 0.5.

The input/output DATA is set LOW at each transfer of seconds to the minutes counter (i.e. each minute), as long as the CBUS is not occupied by a DLEN = HIGH transmission.

DATA will be set HIGH again by a TIME ADDRESS/TIME READ or TIME SET instruction.

Table 1 Cycle lengths of time counter

unit	counting cycle	carry for following unit	content of month counter
minutes	00 59	59 → 00	1 12
hours	00 23	23 → 00	1 12
days	01 28	28 → 01	2
		or 29 → 01*	2
	01 30	30 → 01	4, 6, 9, 11
	01 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	01 12	12 → 01	

* The day counter may be set to 29.2. by a TIME SET instruction (for a leap year), then the month transfer occurs at 1.3.

Comparator (output COMP; input NODA)

The time register for a preset switching time (alarm or remote switching) is a 24-bit memory, which can also be set and read-out via the CBUS interface. If both the times of the time counter and the time register are equal, the output COMP becomes HIGH for one minute.

It is possible to choose a comparison between time counter and the time register either based upon minutes, hours, day and month (i.e. clock time *and* date) or minutes and hours (i.e. daily). It is controlled by bit 'UC' and input NODA (see also Table 3) during setting of the month register;

comparison with date: UC = 0 *and* NODA = LOW

comparison daily: UC = 1 *or* NODA = HIGH.

CBUS interface

The data transmission of the SAF3019 to the microcomputer (TIME READ) and vice versa (TIME SET) is possible via the CBUS; DATA (input/output), DLEN (input) and CLB (input).

Data and addresses are transmitted serially via the DATA line, which are synchronized with the clock burst (CLB) pulses from the microcomputer. The duration of the data transmission is determined by the number of CLB pulses when DLEN = HIGH.

The IC includes a word format checking function, which allows the CBUS to be used for controlling other circuits as well. The following word lengths are recognized as valid transmissions:

- TIME ADDRESS (3-bits and 1 start bit);
- TIME SET (10-bits and 1 start bit).

A TIME ADDRESS instruction always has to be followed by a TIME READ (7-bits) sequence. A TIME SET instruction combines address and data. With each instruction (each TIME ADDRESS and TIME READ instruction cycle) two digits of the time counter and time register can be set. The result is, that for a complete TIME READ and TIME SET transmission, 4 cycles TIME ADDRESS/TIME READ or 4 TIME SET instructions are needed.

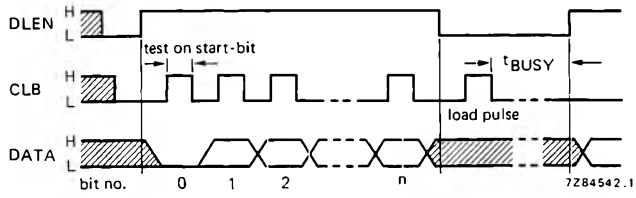

Fig. 2 CBUS data transmission.

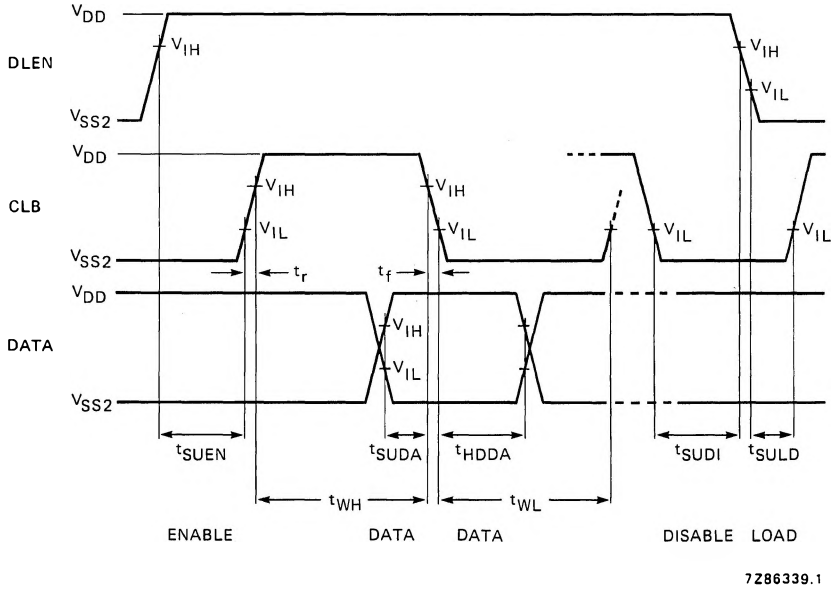

Fig. 3 CBUS timing.

TIME READ

First the bits S, A0 and A1 are transferred from the microcomputer to the SAF3019 with the TIME ADDRESS instruction. With the next instruction (TIME READ), the contents of the selected digits are transferred from the SAF3019 to the microcomputer.

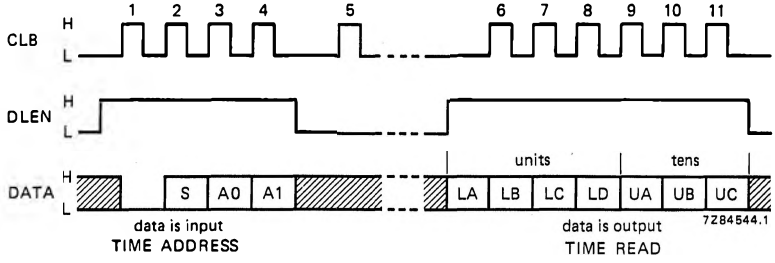

Fig. 4 TIME ADDRESS/TIME READ cycle.

Table 2 Selected digits with respect to the address bits and the TIME READ instruction function.

S	A0	A1	LA	LB	LC	LD	UA	UB	UC	instruction	
0	1	1	D	D	D	D	D	D	D	minutes	time read counter
0	0	1	D	D	D	D	D	D	0	hours	
0	1	0	D	D	D	D	D	D	0	date	
0	0	0	D	D	D	D	D	0	0	month	
1	1	1	D	D	D	D	D	D	D	minutes	time read register
1	0	1	D	D	D	D	D	D	0	hours	
1	1	0	D	D	D	D	D	D	0	date	
1	0	0	D	D	D	D	D	0	0	month	

D = data bit.

TIME SET

The TIME SET instruction transfers the address bits S, A0 and A1 as well as the selected digits of the BCD-coded incoming data from the microcomputer to the SAF3019. The last bit (UC) can control special functions. A TIME SET instruction will not stop the time counter, and also will not generate a non-selected digit for transmission.

The prescaler and seconds counter are reset with the TIME SET instruction when S = 0, A0 = 0, A1 = 0 (addressed for month) and UC = 0. If the seconds counter is between 30 and 59, this instruction generates a transfer for the minutes counter. Therefore, this instruction may be used for a very simple correction of the time counter if the deviation is within ±30 seconds.

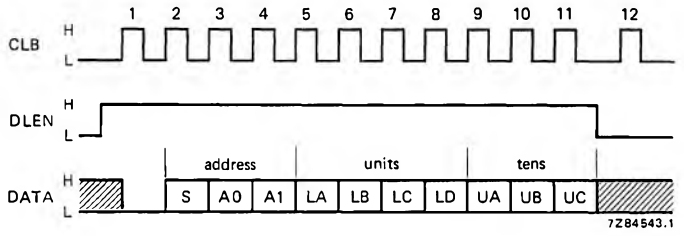

Fig. 5 Data format for TIME SET instruction.

Table 3 Selected digits with respect to the address bits and the possible TIME SET instruction function.

S	A0	A1	LA	LB	LC	LD	UA	UB	UC	instruction	
0	1	1	D	D	D	D	D	D	D	minutes	time set counter
0	0	1	D	D	D	D	D	D	X	hours	
0	1	0	D	D	D	D	D	D	X	date	
0	0	0	D	D	D	D	D	X	1	month	
0	0	0	X	X	X	X	X	X	0	seconds	reset counter
1	1	1	D	D	D	D	D	D	D	minutes	time set register
1	0	1	D	D	D	D	D	D	X	hours	
1	1	0	D	D	D	D	D	D	X	date	
1	0	0	D	D	D	D	D	X	0	month*	
1	0	0	D	D	D	D	D	X	1	month**	

D = data bit; X = 1 or 0.

* Compare *with* date. ** Compare *without* date.

Level shifters

The circuit has been designed for low-voltage operation. However, to interface with the microcomputer, most inputs and outputs have level shifters to operate with the 5 V supply voltage of the microcomputer. These level shifters only function when the 5 V supply (V_{DD}) is available. The internal clock function is independent of this supply.

Power failure (output POWF)

If the supply voltage V_{DD}-V_{SS1} is below a certain internal value (V_{POWF}), the power-failure output (POWF) is set HIGH. The threshold voltage V_{POWF} is lower than the minimum battery voltage V_{DD}-V_{SS1}. This battery is required as back-up for the logic circuitry. It is impossible to have data transmission via the CBUS when V_{DD}-$V_{SS1} < V_{POWF}$, however, the clock will continue running as long as V_{DD}-V_{SS1} does not drop to a lower value. The CBUS is released directly when V_{DD}-V_{SS1} becomes larger than V_{POWF}, but POWF stays HIGH until the next TIME SET instruction, which sets POWF LOW again.

N.B. The 5 V supply voltage (V_{DD}-V_{SS2}) must be switched off when exchanging the battery.

TEST input

The TEST input is used for testing purposes and it is connected to ground (V_{SS2}) for normal operation.

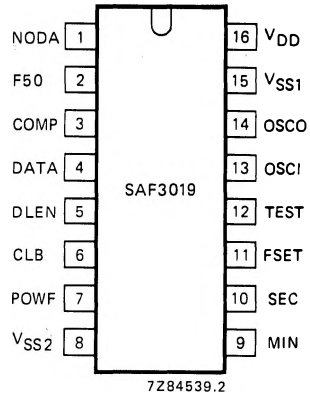

Fig. 6 Pinning diagram.

PINNING

16	V_{DD}	common positive supply (5 V; V_B = 1.5 V)
15	V_{SS1}	negative battery supply (V_B)
8	V_{SS2}	ground (V_{DD})
4	DATA	data input/output } CBUS (bidirectional)
5	DLEN	data line enable input } CBUS (bidirectional)
6	CLB	clock burst input } CBUS (bidirectional)
1	NODA	comparator mode select input
12	TEST	test mode input (normally ground)
2	F50	50 Hz mains frequency input
13	OSCI	input and output of the on-chip oscillator
14	OSCO	input and output of the on-chip oscillator
10	SEC	1 pulse per second output
9	MIN	1 pulse per minute output
3	COMP	comparator output
7	POWF	power failure output
11	FSET	frequency setting signal output (128 Hz)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges	$V_{DD} - V_{SS1}$		−0.5 to + 8	V
	$V_{DD} - V_{SS2}$		−0.5 to + 8	V
Voltage on any pin (except OSCI, OSCO)	V_I	V_{SS2}	−0.6 to V_{DD} + 0.6	V
Voltage on pins OSCI, OSCO	V_I	V_{SS1}	−0.6 to V_{DD} + 0.6	V
Input currents	$\|I_I\|$	max.	10	mA
Output currents	$\|I_O\|$	max.	10	mA
Power dissipation per output	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	200	mW
Operating ambient temperature range	T_{amb}		−40 to + 85	°C
Storage temperature range	T_{stg}		−65 to + 150	°C

D.C. CHARACTERISTICS

V_{SS2} = 0 V; V_{DD} = 4.5 to 5.5 V; T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	with respect to V_{SS2}*	V_{DD}	4.5	5	5.5	V
Battery voltage	between V_{DD} and V_{SS1}	V_B	1.5	–	2.6	V
	at T_{AMB} = 0 to 70 °C	V_B	1.3	–	2.6	V
Time keeping battery voltage		V_{BO}	1.3	–	2.6	V
Supply current	I_O = 0 mA**	$-I_{SS2}$	–	–	50	μA
Battery current	V_B = 1.5 V	$-I_{SS1}$	–	–	10	μA
Inputs DLEN, DATA, CLB, F50, NODA						
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input current at V_I = V_{SS2} or V_{DD}	V_{DD} = 5.5 V	$\|I_I\|$	–	–	1	μA
Input F50 hysteresis	$\Delta V = V_{IH} - V_{IL}$	ΔV	0.2	–	–	V
Outputs SEC, MIN, COMP, POWF (buffer outputs)						
Output voltage HIGH	$-I_O$ = 0.5 mA	V_{OH}	V_{DD} − 0.4	–	–	V
Output voltage LOW	I_O = 1.6 mA	V_{OL}	–	–	0.4	V
Output DATA (N-channel open drain)						
Output voltage LOW	I_O = 1.6 mA	V_{OL}	–	–	0.4	V
Output leakage current	V_O = 5.5 V (HIGH)	I_{OR}	–	–	1	μA

* All outputs are available down to V_{SS2} = V_B at reduced current capability.

** V_I = V_{SS2} or V_I = V_{DD} at all inputs; quartz crystal oscillator operation: f = 32 768 Hz, series resistance of crystal $R_{s\,max}$ = 25 kΩ (40 kΩ for 0 to + 70 °C), C_L = 10 pF.

APPLICATION INFORMATION

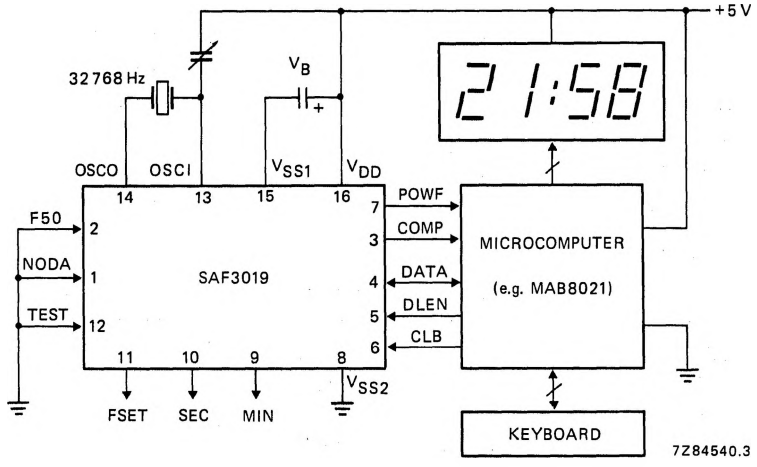

Fig. 7 Typical application of the SAF3019 in a microcomputer controlled system.

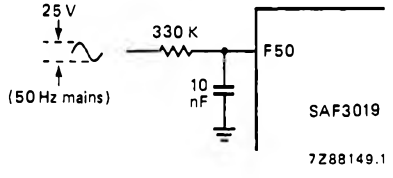

Fig. 8 Circuitry for applying the 50 Hz mains to input F50.

A.C. CHARACTERISTICS

V_{SS2} = 0 V; V_{DD} = 4.5 to 5.5 V; T_{amb} = −40 to + 85 °C; unless otherwise specified

See Figs 2 and 3 for all timing.

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs DLEN, DATA, CLB, NODA						
Rise and fall times	note 1	t_r, t_f	–	–	1	μs
CLB pulse width HIGH		t_{WH}	4	–	∞	μs
CLB pulse width LOW		t_{WL}	4	–	∞	μs
Data set-up time DATA ⟶ CLB		t_{SUDA}	1	–	–	μs
Data hold time DATA ⟶ CLB		t_{HDDA}	2	–	–	μs
Enable set-up time DLEN ⟶ CLB		t_{SUEN}	2	–	–	μs
Disable set-up time CLB ⟶ DLEN		t_{SUDI}	2	–	–	μs
Set-up time DLEN ⟶ CLB (load pulse)		t_{SULD}	1	–	–	μs
Busy-time from load pulse to next start of transmission		t_{BUSY}	2	–	–	μs
CLB frequency		f_{CLB}	0	–	100	kHz
Input F50						
Rise and fall times	notes 1 and 2	t_r, t_f	–	–	10	ms
Pulse width HIGH		t_{WH}	30	–	–	μs
Pulse width LOW		t_{WL}	30	–	–	μs
Oscillator (OSCI, OSCO)						
Series resistance of crystal	f = 32.768 Hz at T_{amb} =	R_s	–	–	25	kΩ
	0 to 70 °C	R_s	–	–	40	kΩ
Load capacitance		C_L	–	10	–	pF

Notes

1. All timing values are referred to V_{IH} and V_{IL} within a voltage swing of minimum V_{SS2} to V_{DD}.
2. The supply current I_{SS2} increases at slow rise/fall times.