National Semiconductor

SCAN18540T
Inverting Line Driver with TRI-STATE® Outputs

General Description

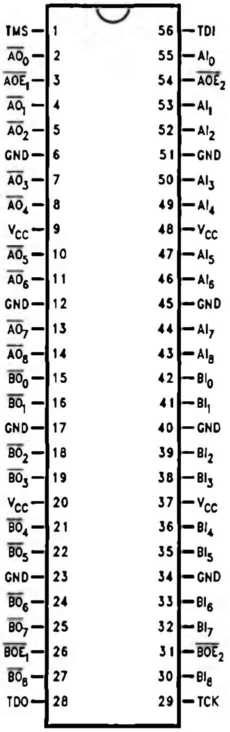
The SCAN18540T is a high speed, low-power line driver featuring separate data inputs organized into dual 9-bit bytes with byte-oriented paired output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- IEEE 1149.1 (JTAG) compliant
- Dual output enable signals per byte
- TRI-STATE outputs for bus-oriented applications
- 9-bit data busses for parity applications
- Reduced-swing outputs source 32 mA/sink 64 mA (Comm), source 24 mA/sink 48 mA (Mil)
- Guaranteed to drive 50Ω transmission line to TTL input levels of 0.8V and 2.0V
- TTL compatible inputs
- 25 mil pitch SSOP (Shrink Small Outline Package)
- Includes CLAMP and HIGHZ instructions
- Member of National's SCAN products

Ordering Code: See Section 11

Connection Diagram



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Pin Names	Description
$AI_{(0-8)}$	Input pins, A side
$BI_{(0-8)}$	Input pins, B side
$\overline{AOE}_1$, $\overline{AOE}_2$	TRI-STATE Output Enable Input pins, A side
$\overline{BOE}_1$, $\overline{BOE}_2$	TRI-STATE Output Enable Input pins, B side
$\overline{AO}_{(0-8)}$	Output pins, A side
$\overline{BO}_{(0-8)}$	Output pins, B side

Truth Tables

Inputs			$\overline{AO}$ (0–8)
$\overline{AOE_1}$	$\overline{AOE_2}$	AI (0–8)	
L	L	H	L
H	X	X	Z
X	H	X	Z
L	L	L	H

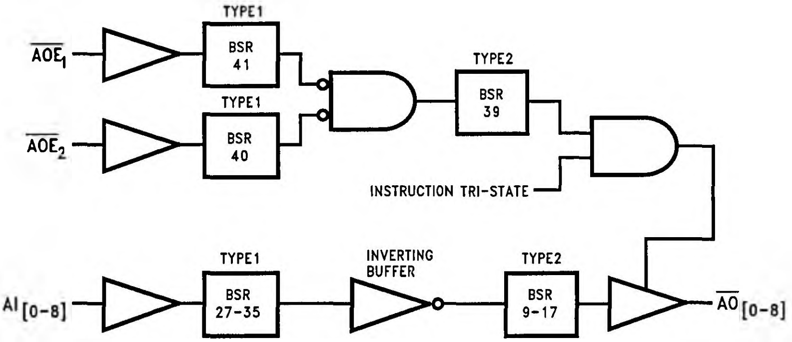
Inputs			$\overline{BO}$ (0–8)
$\overline{BOE_1}$	$\overline{BOE_2}$	BI (0–8)	
L	L	H	L
H	X	X	Z
X	H	X	Z
L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Order Number	Description
SCAN18540TSSC	SSOP in Tubes
SCAN18540TSSCX	SSOP in Tape and Reel
SCAN18540TFMQB	Flatpak Military
5962-9312701MXA	Military SMD #

Block Diagrams

Byte-A



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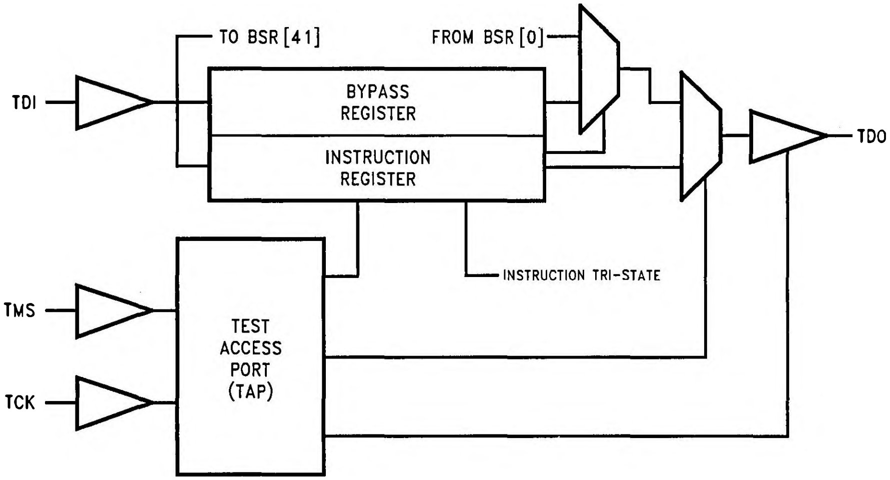
Tap Controller



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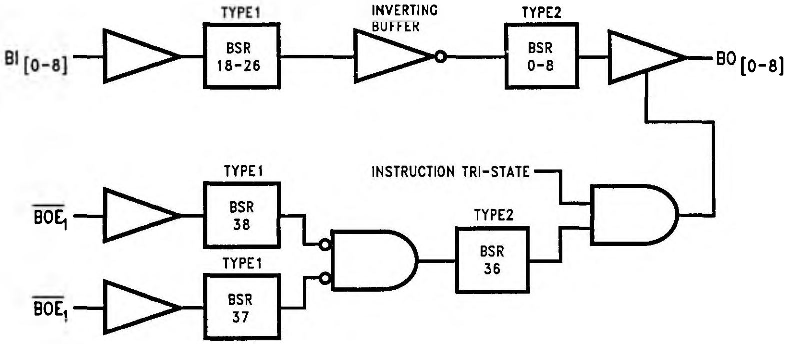
Byte-B



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Note: BSR stands for Boundary Scan Register

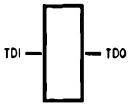
Description of BOUNDARY-SCAN Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10–11* for a further description of scan cell TYPE1 and *Figure 10–12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition
Logic 0



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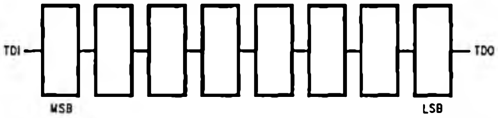
The INSTRUCTION register is an 8-bit register which captures the default value of 01001101. The two least significant bits of this captured value (01) are required by IEEE Std 1149.1. The upper six bits are unique to the SCAN18540T device. SCAN CMOS Test Access Logic devices do not include the IEEE 1149.1 optional identification register. Therefore, this unique captured value can be used as a "pseudo ID" code to confirm that the correct device is placed in the appropriate location in the boundary scan chain.

Instruction Register Scan Chain Definition



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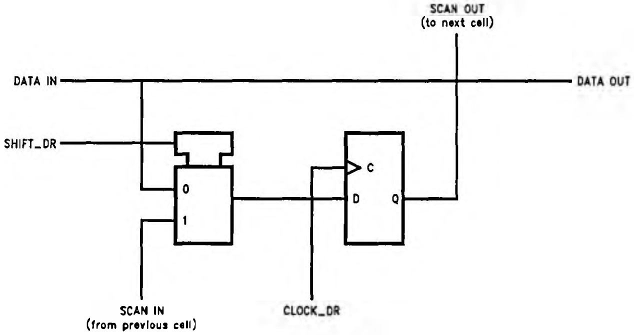
MSB → LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
All Others	BYPASS

Scan Cell TYPE1



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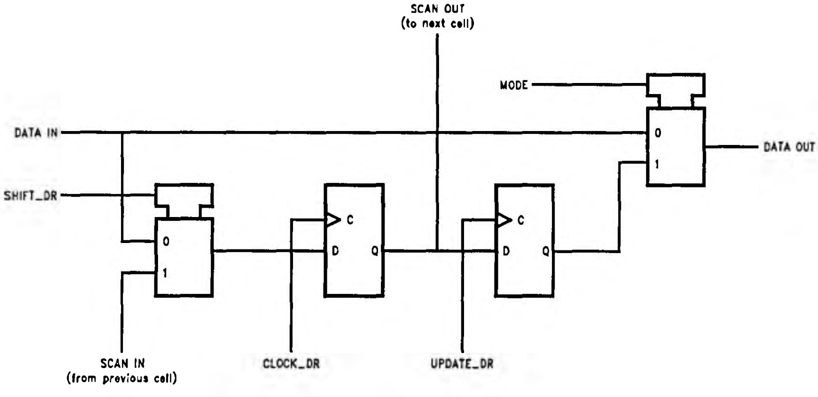
Scan Cell TYPE2



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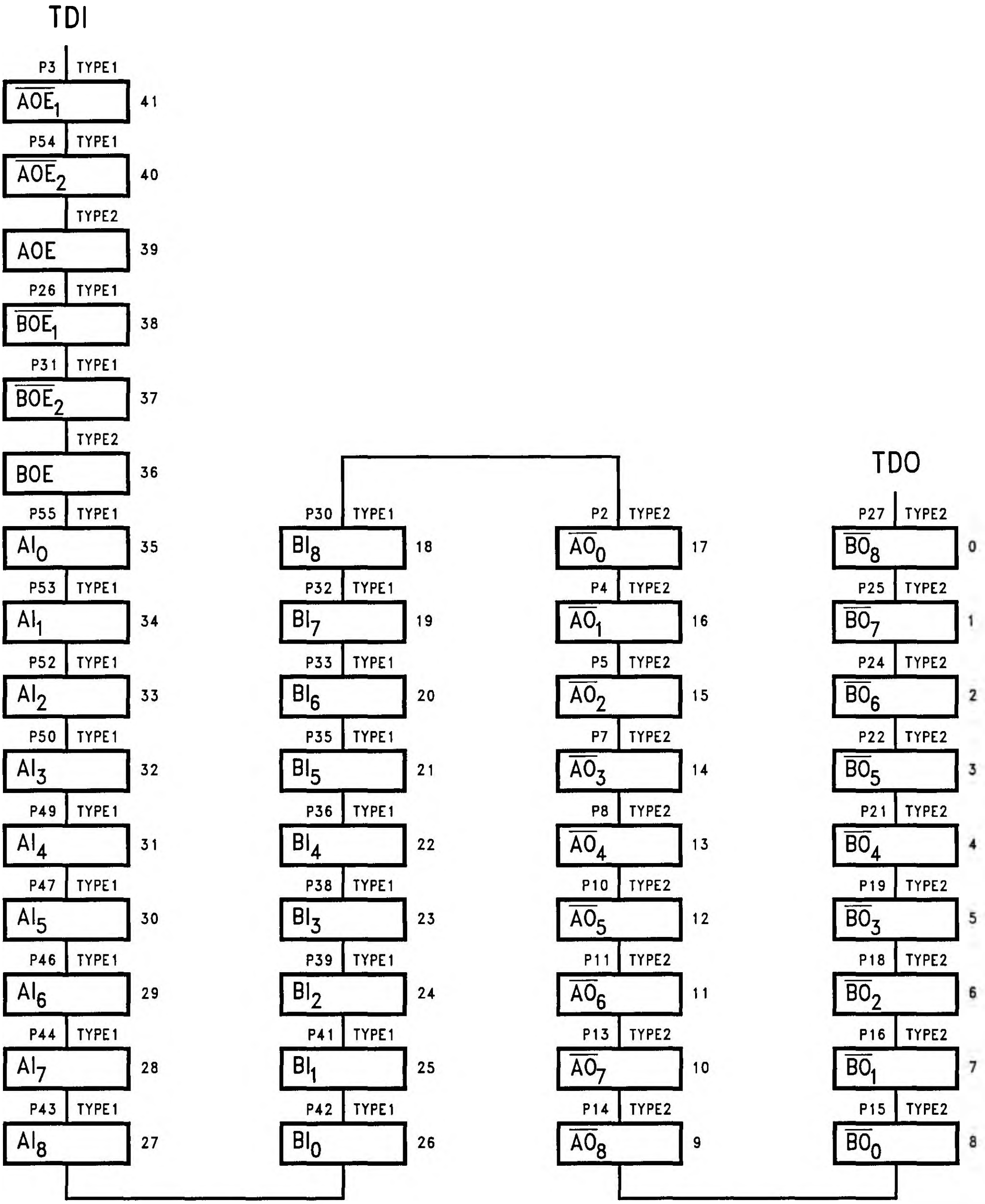
Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register

Scan Chain Definition (42 Bits in Length)



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Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
41	$\overline{AOE_1}$	3	Input	TYPE1	Control Signals
40	$\overline{AOE_2}$	54	Input	TYPE1	
39	AOE		Internal	TYPE2	
38	$\overline{BOE_1}$	26	Input	TYPE1	
37	$\overline{BOE_2}$	31	Input	TYPE1	
36	BOE		Internal	TYPE2	
35	AI_0	55	Input	TYPE1	A-in
34	AI_1	53	Input	TYPE1	
33	AI_2	52	Input	TYPE1	
32	AI_3	50	Input	TYPE1	
31	AI_4	49	Input	TYPE1	
30	AI_5	47	Input	TYPE1	
29	AI_6	46	Input	TYPE1	
28	AI_7	44	Input	TYPE1	
27	AI_8	43	Input	TYPE1	
26	BI_0	42	Input	TYPE1	B-in
25	BI_1	41	Input	TYPE1	
24	BI_2	39	Input	TYPE1	
23	BI_3	38	Input	TYPE1	
22	BI_4	36	Input	TYPE1	
21	BI_5	35	Input	TYPE1	
20	BI_6	33	Input	TYPE1	
19	BI_7	32	Input	TYPE1	
18	BI_8	30	Input	TYPE1	
17	AO_0	2	Output	TYPE2	A-out
16	AO_1	4	Output	TYPE2	
15	AO_2	5	Output	TYPE2	
14	AO_3	7	Output	TYPE2	
13	AO_4	8	Output	TYPE2	
12	AO_5	10	Output	TYPE2	
11	AO_6	11	Output	TYPE2	
10	AO_7	13	Output	TYPE2	
9	AO_8	14	Output	TYPE2	
8	BO_0	15	Output	TYPE2	B-in
7	BO_1	16	Output	TYPE2	
6	BO_2	18	Output	TYPE2	
5	BO_3	19	Output	TYPE2	
4	BO_4	21	Output	TYPE2	
3	BO_5	22	Output	TYPE2	
2	BO_6	24	Output	TYPE2	
1	BO_7	25	Output	TYPE2	
0	BO_8	27	Output	TYPE2	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source/Sink Current (I_O)	±70 mA
DC V_{CC} or Ground Current Per Output Pin	±70 mA
Junction Temperature	
SSOP	+140°C
Storage Temperature	−65°C to +150°C
ESD (Min)	2000V

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of SCAN circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
SCAN Products	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
Commercial	−40°C to +85°C
Military	−55°C to +125°C
Minimum Input Edge Rate dV/dt V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Commercial		Military	Commercial	Units	Conditions
			$T_A = +25°C$		$T_A = -55°C$ to $+125°C$	$T_A = -40°C$ to $+85°C$		
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Input Voltage	4.5	1.5	2.0	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Input Voltage	4.5	1.5	0.8	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Output Voltage	4.5		3.15	3.15	3.15	V	$I_{OUT} = -50\ \mu A$
		5.5		4.15	4.15	4.15		
		4.5		2.4		2.4	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -32$ mA
		5.5		2.4		2.4		
		4.5		2.4	2.4		V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24$ mA
		5.5		2.4	2.4			
V_{OL}	Maximum Low Output Voltage	4.5		0.1	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		5.5		0.1	0.1	0.1		
		4.5		0.55		0.55	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 64$ mA
		5.5		0.55		0.55		
		4.5		0.55	0.55			$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 48$ mA
		5.5		0.55	0.55			
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{IN} TDI, TMS	Maximum Input Leakage	5.5		2.8	3.7	3.6	μA	$V_I = V_{CC}$
				−385	−385	−385	μA	$V_I = GND$
	Minimum Input Leakage	5.5		−160	−160	−160	μA	$V_I = GND$
I_{OLD}	†Minimum Dynamic Output Current	5.5		94	63	94	mA	$V_{OLD} = 0.8V$ Max
I_{OHD}				−40	−27	−40	mA	$V_{OHD} = 2.0V$ Min

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	Commercial		Military	Commercial	Units	Conditions
			$T_A = +25°C$		$T_A = -55°C$ to $+125°C$	$T_A = -40°C$ to $+85°C$		
			Typ	Guaranteed Limits				
I_{OZ}	Maximum Output Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH}
I_{OS}	Output Short Circuit Current	5.5		−100	−100	−100	mA Min	V_O = 0V
I_{CC}	Maximum Quiescent Supply Current	5.5		16.0	168	88	μA	V_O = Open TDI, TMS = V_{CC}
		5.5		750	930	820	μA	V_O = Open TDI, TMS = GND
I_{CCt}	Maximum I_{CC} Per Input	5.5		2.0	2.0	2.0	mA	$V_I = V_{CC}-2.1V$
		5.5		2.15	2.15	2.15	mA	$V_I = V_{CC}-2.1V$ TDI/TMS Pin, Test One with the other Floating

*All outputs loaded; thresholds associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Noise Specifications: See Section 4

Symbol	Parameter	V_{CC} (V)	Commercial		Military	Commercial	Units	Fig. No.
			$T_A = +25°C$		$T_A = -55°C$ to $+125°C$	$T_A = -40°C$ to $+85°C$		
			Typ	Guaranteed Limits				
V_{OLP}	Maximum High Output Noise (Notes 2, 3)	5.0	1.0	1.5			V	4-13
V_{OLV}	Minimum Low Output Noise (Notes 2, 3)	5.0	−0.6	−1.2			V	4-13
V_{OHP}	Maximum Overshoot (Notes 1, 3)	5.0	$V_{OH}+1.0$	$V_{OH}+1.5$			V	4-13
V_{OHV}	Minimum V_{CC} Droop (Notes 1, 3)	5.0	$V_{OH}-1.0$	$V_{OH}-1.8$			V	4-13
V_{IHD}	Minimum High Dynamic Input Voltage Level (Notes 1, 4)	5.5	1.6	2.0	2.0	2.0	V	
V_{ILD}	Maximum Low Dynamic Input Voltage Level (Notes 1, 4)	5.5	1.4	0.8	0.8	0.8	V	

Note 1: Worst case package.

Note 2: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched LOW and one output held LOW.

Note 3: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched HIGH and one output held HIGH.

Note 4: Maximum number of data inputs (n) switching. (n-1) input switching 0V to 3V. Input under test switching 3V to threshold (V_{ILD}).

AC Electrical Characteristics Normal Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$ $C_L = 50$ pF			Military $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		Commercial $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay Data to Q	5.0	2.5 2.5		9.0 9.0	2.5 2.5	10.5 10.5	2.5 2.5	9.8 9.8	ns	4-1, 2
t_{PLZ}, t_{PHZ}	Disable Time	5.0	1.5 1.5		10.2 10.2	1.5 1.5	11.2 11.2	1.5 1.5	10.7 10.7	ns	4-3, 4
t_{PZL}, t_{PZH}	Enable Time	5.0	2.0 2.0		11.8 9.5	2.0 2.0	13.5 11.5	2.0 2.0	12.8 10.5	ns	4-3, 4

*Voltage Range 5.0 is 5.0V ± 0.5V.

AC Electrical Characteristics Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial			Military		Commercial		Units	Fig. No.
			$T_A = +25°C$ $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF			
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay TCK to TDO	5.0	3.5 3.5		13.2 13.2	3.5 3.5	15.8 15.8	3.5 3.5	14.5 14.5	ns	4-8
t_{PLZ}, t_{PHZ}	Disable Time TCK to TDO	5.0	2.5 2.5		11.5 11.5	2.5 2.5	12.8 12.8	2.5 2.5	11.9 11.9	ns	4-9, 10
t_{PZL}, t_{PZH}	Enable Time TCK to TDO	5.0	3.0 3.0		14.5 14.5	3.0 3.0	16.7 16.7	3.0 3.0	15.8 15.8	ns	4-9, 10
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Update--DR State	5.0	5.0 5.0		18.0 18.0	5.0 5.0	21.7 21.7	5.0 5.0	19.8 19.8	ns	4-8
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Update-IR State	5.0	5.0 5.0		18.6 18.6	5.0 5.0	21.2 21.2	5.0 5.0	20.2 20.2	ns	4-8
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	5.5 5.5		19.9 19.9	5.5 5.5	23.0 23.0	5.5 5.5	21.5 21.5	ns	4-8
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Update-DR State	5.0	4.0 4.0		16.4 16.4	4.0 4.0	19.6 19.6	4.0 4.0	18.2 18.2	ns	4-9, 10
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Update-IR State	5.0	5.0 5.0		19.5 19.5	5.0 5.0	22.4 22.4	5.0 5.0	20.8 20.8	ns	4-9, 10
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	5.0 5.0		19.9 19.9	5.0 5.0	23.3 23.3	5.0 5.0	21.5 21.5	ns	4-9, 10
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Update-DR State	5.0	5.0 5.0		18.9 18.9	5.0 5.0	22.6 22.6	5.0 5.0	20.9 20.9	ns	4-9, 10
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Update-IR State	5.0	6.5 6.5		22.4 22.4	6.5 6.5	26.2 26.2	6.5 6.5	24.2 24.2	ns	4-9, 10
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	7.0 7.0		23.8 23.8	7.0 7.0	27.4 27.4	7.0 7.0	25.7 25.7	ns	4-9, 10

*Voltage Range 5.0 is 5.0V ±0.5V.

All Propagation Delays involving TCK are measured from the falling edge of TCK.

AC Operating Requirements Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial	Military	Commercial	Units	Fig. No.
			$T_A = +25°C$ $C_L = 50$ pF	$T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		
			Guaranteed Minimum				
t_S	Setup Time, H or L Data to TCK (Note 1)	5.0	3.0	3.0	3.0	ns	4-11
t_H	Hold Time, H or L TCK to Data (Note 1)	5.0	4.5	5.5	4.5	ns	4-11
t_S	Setup Time, H or L $\overline{AOE}_n$, $\overline{BOE}_n$ to TCK (Note 3)	5.0	3.0	3.0	3.0	ns	4-11
t_H	Hold Time, H or L TCK to $\overline{AOE}_n$, $\overline{BOE}_n$ (Note 3)	5.0	4.5	4.5	4.5	ns	4-11
t_S	Setup Time, H or L Internal AOE, BOE, to TCK (Note 2)	5.0	3.0	3.0	3.0	ns	4-11
t_H	Hold Time, H or L TCK to Internal AOE, BOE (Note 2)	5.0	3.0	3.0	3.0	ns	4-11
t_S	Setup Time, H or L TMS to TCK	5.0	8.0	8.0	8.0	ns	4-11
t_H	Hold Time, H or L TCK to TMS	5.0	2.0	2.0	2.0	ns	4-11
t_S	Setup Time, H or L TDI to TCK	5.0	4.0	4.0	4.0	ns	4-11
t_H	Hold Time, H or L TCK to TDI	5.0	4.5	4.5	4.5	ns	4-11
t_W	Pulse Width TCK	5.0					
	H		15.0	15.0	15.0	ns	4-12
	L		5.0	5.0	5.0		
f_{max}	Maximum TCK Clock Frequency	5.0	25	25	25	MHz	
T_{PU}	Wait Time, Power Up to TCK	5.0	100	100	100	ns	
T_{DN}	Power Down Delay	0.0	100	100	100	ms	

*Voltage Range 5.0 is 5.0V ±0.5V.

All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Note 1: This delay represents the timing relationship between the data input and TCK at the associated scan cells numbered 0-8, 9-17, 18-26, and 27-35.

Note 2: This delay represents the timing relationship between AOE/BOE and TCK for scan cells 36 and 39 only.

Note 3: Timing pertains to BSR 37, 38, 40 and 41.

Extended AC Electrical Characteristics: See Section 4

Symbol	Parameter	T_A = Com V_{CC} = Com C_L = 50 pF 18 Outputs Switching (Note 2)			T_A = Mil V_{CC} = Mil C_L = 50 pF 18 Outputs Switching (Note 2)		T_A = Com V_{CC} = Com C_L = 250 pF (Note 3)		T_A = Mil V_{CC} = Mil C_L = 250 pF (Note 3)		Units
		Min	Typ	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay Data to Output	3.0 3.0		11.0 11.0	3.0 3.0	11.5 11.5	4.0 4.0	13.0 15.0	4.0 4.0	14.0 16.0	ns
t_{PZH}, t_{PZL}	Output Enable Time	2.5 2.5		11.5 14.0	2.5 2.5	12.5 14.5	(Note 4)		(Note 4)		ns
t_{PHZ}, t_{PLZ}	Ouput Disable Time	2.0 2.0		11.5 11.5	2.0 2.0	12.0 12.0	(Note 5)		(Note 5)		ns
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output		0.5	1.0				1.0			ns
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output		0.5	1.0				1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination LOW to HIGH and/or HIGH to LOW.

Note 2: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low etc.).

Note 3: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 4: TRI-STATE delays are load dominated and have been excluded from the datasheet.

Note 5: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	4.0	pF	V_{CC} = 5.0V
C_{OUT}	Output Pin Capacitance	13.0	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	34.0	pF	V_{CC} = 5.0V