CMOS GATE ARRAYS (M-Series)

FEATURES

- **Customer programmable LSI**
- **330 to 1100 gate complexity**
- **Mature silicon gate technology with local oxidation**
- **Library of 60 pre-designed, fully characterized macrocells available**
- **Full CAD, including auto-place and auto-route, for quick error-free design**
- **Very low power consumption (e.g. standby power for SCC 0700 is 0.25mW)**
- **Excellent noise immunity**
- **Power supply range 3 to 15V**
- **Over 80% utilization typical**
- **Fully programmable I/O pins, each having a wide range of functions**
- **Input protection by series resistor and diode clamp to V_{SS}**
- **TTL outputs (buffers) drive up to four LSTTL loads**
- **−55°C to +125°C operating temperature**
- **Plastic and ceramic DIP, ceramic leadless chip carriers, and plastic leaded chip carriers available**

PRODUCT DESCRIPTION

The SCCXXXX gate array family offers the circuit designer the facility to create a semi-custom circuit with a unique set of CAD (Computer-Aided Design) tools in a well-established CMOS process.

Signetics M-Series CMOS Gate Arrays are single chip programmable devices that allow customization of user logic. Only metalization and contact are programmed in these mature CMOS devices. Thus, fast turnaround from logic to completed silicon is achieved.

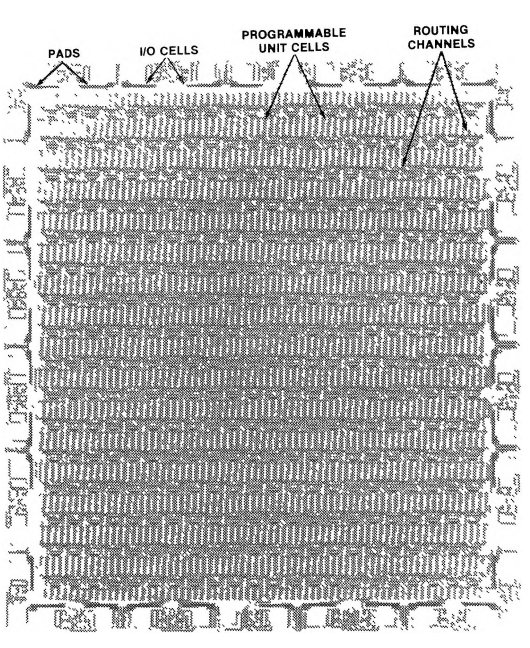
Each device in this family of low power gate arrays contains numerous identical, uncommitted unit cells (Figure 1) which are interconnected by two custom masks (metal and contact). Each unit cell contains four pairs of N and P transistors. Access to the transistors is from both the top and bottom of the cells and, additionally, there are two poly feed-throughs at each side of the cell. This homogenous cell design allows for excellent routing flexibility, and many designs result in better than 80% utilization of the gates available.

The M-Series Gate Arrays are built on a mature, state-of-the-art 4-micron Si-gate CMOS process incorporating an epi-substrate, which significantly reduces the potential for latch as compared with other bulk CMOS processes.

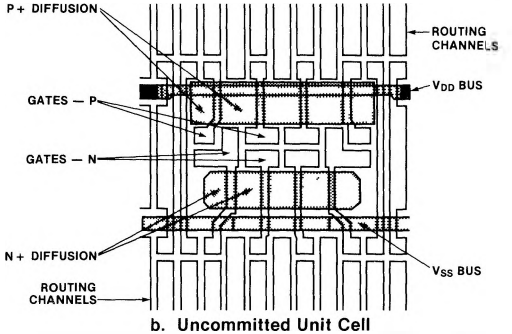
Computer Aided Design (CAD) is used throughout the design process to ensure accurate implementation of customer logic (see Figure 14 for typical process flow).

ORDERING INFORMATION

Contact Local Sales Representative



a. SCC0700 CMOS Gate Array



b. Uncommitted Unit Cell

	SCC0330	SCC0450	SCC0700	SCC1100
Gate equivalents (2 input)	330	448	704	1116
Unit cells	165	224	352	558
Rows	11	14	16	18
Unit cells per row	15	16	22	31
Pins (max.)	40	28	40	68
I/O stages (max.)	38	26	38	66
I/O options				
3 state I/O (max.)	34	26	38	66
Direct or inverted inputs (max.)	38	26	38	66
Drivers (max.)	38	14	22	66
Buffers (max.)	34	12	16	66
Schmitt Triggers (max.)	34	8	10	66
Pin pull-up/pull down resistors (max.)	34	26	34	66

c. Product Matrix

Figure 1. Internal Configuration and Functional Characteristics of M-Series CMOS Gate Arrays

ABSOLUTE MAXIMUM RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	− 0.5 to + 18V
Voltage on any input when pin pull up/down resistors are: Used Not used	 V_I V_I	 − 0.5 to V_{DD} + 0.5V − 0.5 to + 18V
DC current into any input or output	± 1	Max. 10mA
Power dissipation per output	P	Max. 100mW
Power dissipation per package For standard temperature range: − 40°C to + 85°C (plastic and ceramic DIP) For T_{amb} = − 40°C to + 60°C For T_{amb} = + 60°C to + 85°C	 P_{tot} P_{tot}	 Max 400mW Derate linearly by 8mW/K to 200mW
For extended temperature range: − 55°C to + 125°C (ceramic DIP) For T_{amb} = − 55°C to + 100°C For T_{amb} = + 100°C to + 125°C	 P_{tot} P_{tot}	 Max. 400mW Derate linearly by 8mW/K to 200mW
Storage temperature range	T_{stg}	− 65°C to + 150°C

DC ELECTRICAL CHARACTERISTICS V_{SS} = 0V, for all devices unless otherwise specified

SYMBOL AND PARAMETER	OPERATING TEMP (T_{amb})[1]	SUPPLY VOLTAGE	TEST CONDITIONS	TEMPERATURE RANGE[1]						UNIT
				T_{amb} = LOW		T_{amb} = 25°C		T_{amb} = HIGH		
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{DD} Quiescent device current	Standard	5	All valid input combinations, $V_I = V_{SS}$ or V_{DD}	—	50	—	50	—	375	µA
		10		—	100	—	100	—	750	
		15		—	200	—	200	—	1500	
	Extended	5		—	15	—	15	—	375	
		10		—	25	—	25	—	750	
		15		—	50	—	50	—	1500	
V_{OL} Output voltage Low	Both standard and extended ranges	5	$V_I = V_{SS}$ or V_{DD}, I_O < 1.0µA	—	0 05	—	0 05	—	0 05	V
		10		—	0 05	—	0 05	—	0 05	
		15		—	0 05	—	0 05	—	0 05	
V_{OH} Output voltage High		5		4 95	—	4 95	—	4 95	—	
		10		9 95	—	9 95	—	9 95	—	
		15		14 95	—	14 95	—	14 95	—	
V_{IL} Input voltage Low: INPI/INPB	Both standard and extended ranges	5	V_O = 0.5V or 4.5V; I_O < 1 0µA	—	1 5	—	1 5	—	1 5	
		10		—	3 0	—	3.0	—	3 0	
		15	V_O = 1 0V or 9 0V, I_O < 1 0µA	—	4.0	—	4 0	—	4 0	
V_{IH} Input voltage High: INPI/INPB		5		3 5	—	3 5	—	3 5	—	
		10	V_O = 1 5V or 13.5V, I_O < 1.0µA	7 0	—	7 0	—	7 0	—	
		15		11 0	—	11 0	—	11 0	—	
V_{IL} Input voltage Low INPA, INPD, INPS	Both standard and extended ranges	5	V_O = 0 5V or 4 5V, I_O < 1.0µA	—	1 0	—	1 0	—	1 0	
		10		—	2 0	—	2 0	—	2 0	
		15	V_O = 1 0V or 9.0V, I_O < 1 0µA	—	2.5	—	2 5	—	2 5	
V_{IH} Input voltage High: INPA, INPD, INPS		5		4.0	—	4 0	—	4 0	—	
		10	V_O = 1 5V or 13 5V; I_O < 1 0µA	8 0	—	8 0	—	8 0	—	
		15		12 5	—	12 5	—	12.5	—	

DC ELECTRICAL CHARACTERISTICS (Continued) V_{SS} = 0V; for all devices unless otherwise specified.

SYMBOL AND PARAMETER	OPERATING TEMP (T_{amb})[1]	SUPPLY VOLTAGE	TEST CONDITIONS	TEMPERATURE RANGE[1]						UNIT
				T_{amb} = LOW		T_{amb} = 25°C		T_{amb} = HIGH		
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{OL} Output (sink) current Low driver outputs	Standard	5	V_I = 0V or 5V; V_O = 0.4V	1.1	—	0.9	—	0.7	—	mA
		10		4.0	—	3.3	—	2.6	—	
		15		12.0	—	10.0	—	8.0	—	
	Extended	5		1.2	—	0.9	—	0.6	—	
		10		4.2	—	3.3	—	2.2	—	
		15	V_I = 0V or 10V; V_O = 0.5V	13.0	—	10.0	—	6.7	—	
I_{OL} Output (sink) current Low buffer outputs	Standard	5		2.2	—	1.8	—	1.4	—	
		10	V_I = 0V or 15V; V_O = 1.5V	8.0	—	6.6	—	5.6	—	
		15		24.0	—	20.0	—	16.0	—	
	Extended	5		2.4	—	1.8	—	1.2	—	
		10		8.4	—	6.6	—	4.4	—	
		15		26.0	—	20.0	—	13.4	—	
$-I_{OH}$ Output (source) current High	Standard	5	V_I = 0V or 5V; V_O = 4.6V	1.1	—	0.9	—	0.7	—	
		10		3.1	—	2.6	—	2.0	—	
		15	V_I = 0V or 10V; V_O = 9.5V	12.0	—	10.0	—	8.0	—	
	Extended	5		1.2	—	0.9	—	0.6	—	
		10		3.5		2.6		1.7		
		15	V_I = 0V or 15V; V_O = 13.5V	13.0	—	10.0	—	6.7	—	
$\pm I_{IN}$ Input leakage current	Standard	10	V_I = 0V or 10V	—	0.3	—	0.3	—	1.0	μA
		15		—	0.3	—	0.3	—	1.0	
	Extended	10	V_I = 0V or 15V	—	0.1	—	0.1	—	1.0	
		15		—	0.1	—	0.1	—	1.0	
I_{OZH} Three-state output and open N-channel output leakage current High	Standard	10	Output returned to V_{DD}	—	1.6	—	1.6	—	12.0	
		15		—	1.6	—	1.6	—	12.0	
	Extended	10		—	0.4	—	0.4	—	5.0	
		15		—	0.4	—	0.4	—	5.0	
$-I_{OZL}$ Three-state output and open P-channel output leakage current Low	Standard	10	Output returned to V_{SS}	—	1.6	—	1.6	—	12.0	
		15		—	1.6	—	1.6	—	12.0	
	Extended	10		—	0.4	—	0.4	—	5.0	
		15		—	0.4	—	0.4	—	5.0	
V_{TH} Upper threshold voltage	Standard	5	Internal Schmitt trigger	—	—	3.4 (Typical values)		—	—	V
		10		—	—	6.8 (Typical values)		—	—	
		15		—	—	10.2 (Typical values)		—	—	
V_{TL} Lower threshold voltage		5		—	—	2.2 (Typical values)		—	—	
		10		—	—	3.0 (Typical values)		—	—	
		15		—	—	3.8 (Typical values)		—	—	
V_H Hysteresis voltage input: INPS	—	5	—	—	—	0.2 (Typical values)		—	—	
		10		—	—	0.6 (Typical values)		—	—	
		15		—	—	0.8 (Typical values)		—	—	

NOTES.
1. T_{amb} Low: −40°C for standard temperature range; −55°C for extended temperature range. T_{amb} High: +85°C for standard temperature range; +125°C for extended temperature range.
2. Pin-connected pull-up and pull-down resistors are typically 7 to 78 K-ohms — see PERIPHERY
3. When pull-up or pull-down resistors are used, current limits for I_{DD} must be extrapolated

DC CHARACTERISTICS (Continued)

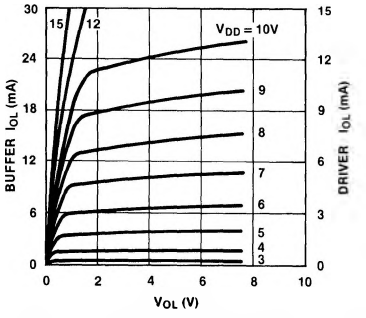


Figure 2. Minimum Output Current LOW as a Function of the Output Voltage LOW; Buffer and Driver Outputs

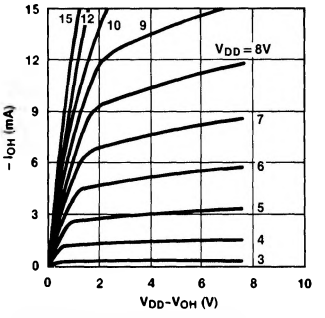


Figure 3. Minimum Output Current HIGH as a Function of the Supply Voltage Minus the Output Voltage HIGH

AC ELECTRICAL CHARACTERISTICS V_{SS} = 0V; T_{amb} = 25°C

SYMBOL AND PARAMETER		PWR SUP (V_{DD})	MIN	TYP	MAX	UNIT
f_{max}	Maximum toggle frequency flip-flop GT00 (no set/reset)	5	6	12	—	MHz
		10	12	24	—	MHz
		15	15	30	—	MHz
f_s	Maximum system frequency (may depend on number of gates in sequence)	5	3	6	—	MHz
		10	6	12	—	MHz
		15	9	18	—	MHz
t_p	Propagation delays for 2-input NAND gate with fanout of 2	5	—	8	16	ns
		10	—	3.2	6.4	ns
		15	—	2	4	ns

SYMBOL AND PARAMETER		PWR SUP (V_{DD})	MIN	TYP	MAX	UNIT
OUTPUT STAGE TRANSITION TIMES; Input transition ≤ 20ns, C_L = 50pF; V_{SS} = 0V, T_{amb} = 25°C						
t_{THL}	Driver outputs High-to-Low	5		60	120	ns
		10		30	60	ns
		15		20	40	ns
t_{THL}	Buffer outputs High-to-Low	5		30	60	ns
		10		15	30	ns
		15		10	20	ns
t_{TLH}	Buffer outputs Low-to-High	5		40	80	ns
		10		18	36	ns
		15		12	24	ns

GATE DELAYS

Nominal Propagation Delay

In Figures 6 through 12, examples are given of the nominal propagation delay times of several library cells, these being calculated from the delay figures given in the individual macro descriptions. These graphs are intended to provide quick-reference data to enable the designer to make an estimate of critical a.c. path without having built or simulated a network.

Accurate delay figures can only be obtained after incorporating the wiring length load automatically calculated by INGATE (i.e., the result of the automatic routing program). A maximum delay is obtained by multiplying the nominal value by 2.2.

GATE DELAYS (Continued)

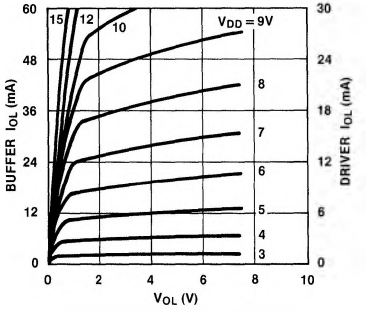


Figure 4. Typical Output Current LOW as a Function of the Output Voltage LOW; Buffer and Driver Outputs

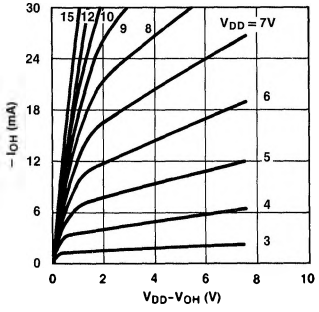


Figure 5. Typical Output Current HIGH as a Function of the Supply Voltage Minus the Output Voltage HIGH

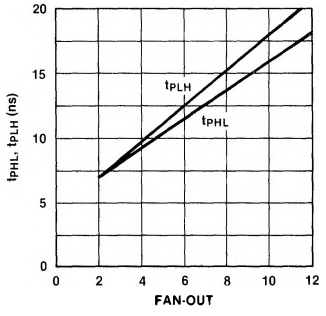


Figure 6. Nominal Propagation Delay as a Function of the Fan-Out; GIN1 (Single Inverter)

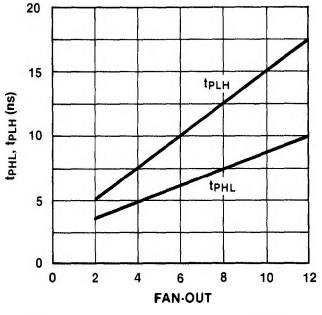


Figure 7. Nominal Propagation Delay as a Function of the Fan-Out; GNAND2 (2-Input NAND Gate)

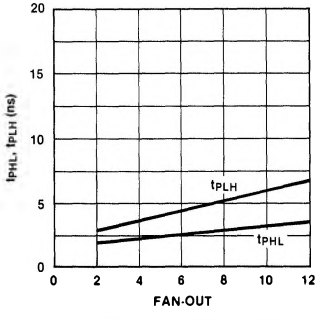


Figure 8. Nominal Propagation Delay as a Function of the Fan-Out; GIN4 (Quadruple Inverter)

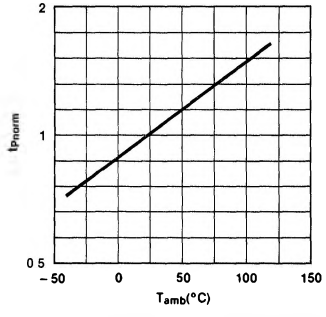


Figure 9. Normalized Propagation Delay (t_{Pnorm}) as a Function of the Ambient Temperature

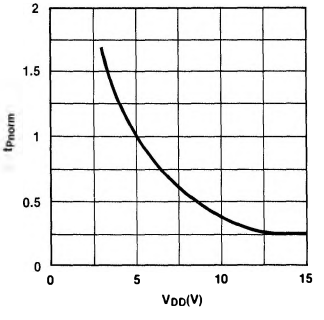


Figure 10. Normalized Propagation Delay (t_{Pnorm}) as a Function of the Supply Voltage

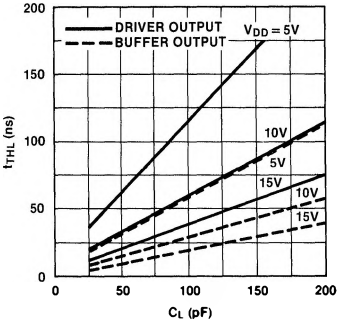


Figure 11. Output Transition Time (HIGH-to-LOW) as a Function of the Load Capacitance

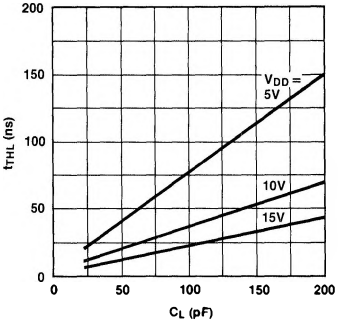
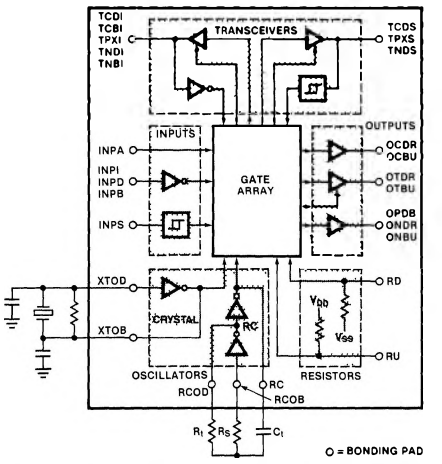


Figure 12. Output Transition Time (LOW-to-HIGH) as a Function of the Load Capacitance for Driver and Buffer Outputs

PERIPHERY

To provide a versatile interface, M-Series CMOS arrays have numerous I/O pads—see Figure 1a. These peripheral elements can be configured to match the input or output requirements of a wide variety of logic families. Accordingly, a bonding pad may have one of the following functions assigned to it:

- INPUT STAGE which includes an input protection circuit (series resistor and single diode clamp to V_{SS}). The recommended maximum load is 260 array gates, or 100 array gates for optimum speed performance. Because the input voltage is not clamped to V_{DD}, input voltages greater than the supply voltage is possible, thus allowing voltage level shifting.
- SCHMITT TRIGGER input stage for noise reduction, pulse shaping, or suppression of oscillation spikes associated with slow input clock transitions. The recommended maximum load is 10 array gates, or 5 for optimum speed performance.
- TRANSCEIVER input/output stage
- THREE-STATE output with driver or buffer performance capability for bussing applications
- COMPLEMENTARY OUTPUT with driver or buffer performance capability.
- OPEN DRAIN N- or P-transistor output
- PULL-UP/PULL-DOWN resistors (see Figure 2 for availability) may be added at various I/O stages. The values available are 5, 10, 15, 30, 60, 65, 70 and 75 Kohms.



TRANSCEIVERS WITH INVERTER INPUT	
TCDI	complementary driver output
TCBI	complementary buffer output
TPXI	open drain p-channel driver output
TNDI	open drain n-channel driver output
TNBI	open drain n-channel buffer output
TRANSCEIVER WITH SCHMITT TRIGGER INPUT	
TCDS	complementary driver output
TPXS	open drain p-channel driver output
TNDS	open drain n-channel driver output
INPUTS	
INPA	direct access to array
INPI	inverter
INPD	driver
INPB	buffer
INPS	Schmitt trigger
OUTPUTS	***FANOUT: DRIVER = 4 LSTTL LOADS @ 4.5V BUFFER = 6 LSTTL LOADS @ 4.5V***
OCDR	complementary driver
OCBU	complementary buffer
OTDR	3-state driver
OTBU	3-state buffer
OPDB	open drain p-channel driver
ONDR	open drain n-channel driver
ONBU	open drain n-channel buffer
OSCILLATORS	
XTOD	crystal oscillator with driver stage
XTOB	crystal oscillator with buffer stage
RCOD	RC oscillator with driver stage
RCOB	RC oscillator with buffer stage
RESISTORS	
RD	pull-down resistors
RU	pull-up resistors

Figure 13. The SCCXXXX I/O Cell Library

Table 1. THE SCCXXXX GATE ARRAY CELL LIBRARY

LIBRARY IDENT. CODE	LOGIC ELEMENT	FUNCTION	NUMBER OF UNITS	NUMBER OF EQUIV. GATES	REMARKS
Inverters/buffers					
GIN1	Inverter	A	¼	½	Max. 2 in one unit
GIN2	Array driver inverting	A	½	1	2 times GIN1
GIN3	Array driver inverting	A	¾	1 + ½	3 times GIN1
GIN4	Array driver inverting	A	1	2	4 times GIN1
GIN6	Array driver inverting	A	1 + ½	3	6 times GIN1
GIN8	Array driver inverting	A	2	4	8 times GIN1
GIN12	Array driver inverting	A	3	6	12 times GIN1
GB12	Array buffer non-inverting	A	1	2	2 times GIN1
GB13	Array buffer non-inverting	A	1	2	3 times GIN1
NAND/AND gates					
GNAND2	2-input NAND	$\overline{A1 \cdot A2}$	½	1	
GNAND3	3-input NAND	$\overline{A1 \cdot A2 \cdot A3}$	¾	1 + ½	
GNAND4	4-input NAND	$\overline{A1 \cdot A2 \cdot A3 \cdot A4}$	1	2	
GAND2	2-input AND	$A1 \cdot A2$	1	2	Output GIN2
GAND3	3-input AND	$A1 \cdot A2 \cdot A3$	1	2	
OR/NOR gates					
GNOR2	2-input NOR	$\overline{A1 + A2}$	½	1	
GNOR3	3-input NOR	$\overline{A1 + A2 + A3}$	¾	1 + ½	
GNOR4	4-input NOR	$\overline{A1 + A2 + A3 + A4}$	1	2	
GOR2	2-input OR	$A1 + A2$	1	2	Output GIN2
GOR3	3-input OR	$A1 + A2 + A3$	1	2	
Complex logic functions					
GF01	Complex function	$\overline{A1 + B1 \cdot B2}$	1	2	
GF02		$\overline{A1 + B1 \cdot B1 \cdot B3}$	1	2	
GF03		$\overline{A1 \cdot A2 + B1 \cdot B2}$	1	2	
GF06		$\overline{A1 + A2 + B1 \cdot B2}$	1	2	
GF15		$\overline{A1 + B1 \cdot (C1 + C2)}$	1	2	
GF51		$\overline{A1 \cdot (B1 + B2)}$	1	2	
GF52		$\overline{A1 \cdot (B1 + B2 + B3)}$	1	2	
GF53		$\overline{(A1 + A2) \cdot (B1 + B2)}$	1	2	
GF56		$\overline{A1 \cdot A2 \cdot (B1 + B2)}$	1	2	
GF65		$\overline{A1 \cdot (B1 + C1 \cdot C2)}$	1	2	
GXOR1	EXCLUSIVE-OR	$\overline{A \cdot B + \bar{A} \cdot \bar{B}}$	1	2	Unbuffered
GXNOR1	EXCLUSIVE-NOR	$A \cdot B + \bar{A} \cdot \bar{B}$	1	2	Unbuffered
GXOR2	EXCLUSIVE-OR	$A \cdot B + \bar{A} \cdot \bar{B}$	1	2	Buffered
GXNOR2	EXCLUSIVE-NOR	$A \cdot B + \bar{A} \cdot \bar{B}$	1	2	Buffered
GXOR3	EXCLUSIVE-OR	$A \cdot B + \bar{A} \cdot \bar{B}$	2	4	
Transmission gate latches					
GTL0	Strobed D-LATCH without SET and RESET		1	2	
GTLRP	Strobed D-LATCH with RESET		1 + ½	3	Positive triggered
GTLRN	Strobed D-LATCH with RESET		1 + ½	3	Negative triggered
GTLSP	Strobed D-LATCH with SET		1 + ½	3	Positive triggered
GTLSN	Strobed D-LATCH with SET		1 + ½	3	Negative triggered
GTL2	Strobed D-LATCH with SET and RESET		1 + ½	3	

Table 1. THE SCCXXXX GATE ARRAY CELL LIBRARY (Continued)

LIBRARY IDENT. CODE	LOGIC ELEMENT	FUNCTION	NUMBER OF UNITS	NUMBER OF EQUIV. GATES	REMARKS
Compound latches					
GGM0	MASTER module without SET and RESET		2	4	
GGMR	MASTER module with RESET		2	4	All positive triggered
GGMS	MASTER module with SET		2	4	
GGM2	MASTER module with SET and RESET		2	4	
GGS0	SLAVE module without SET and RESET		2	4	
GGSR	SLAVE module with RESET		2	4	All negative triggered
GGSS	SLAVE module with SET		2	4	
GGS2	SLAVE module with SET and RESET		2	4	
Transmission gate master-slave flip-flop (MD-D-FF)					
GT00	MS-D-FF without SET and RESET		2	4	
GTR0P	MS-D-FF with RESET on MASTER		2 + ½	5	Positive triggered
GTR0N	MS-D-FF with RESET on MASTER		2 + ½	5	Negative triggered
GTRRP	MS-D-FF with RESET on MASTER and SLAVE		3	6	Positive triggered
GTRRN	MS-D-FF with RESET on MASTER and SLAVE		3	6	Negative triggered
GTSSP	MS-D-FF with SET on MASTER and SLAVE		3	6	Positive triggered
GTSSN	MS-D-FF with SET on MASTER and SLAVE		3	6	Negative triggered
GT22	MS-D-FF with SET and RESET on MASTER and SLAVE		3	6	

DESIGNING A GATE ARRAY CHIP

The design of a gate array chip can be subdivided into several steps, which logically succeed each other, but can sometimes be performed in parallel. (See Figure 14.)

Logic Network Description

This transfers the user specification into a logic network description, using the gate array cells from the cell library.

The cell library contains several logic functions, ranging from simple logic gates (AND, NAND, etc.) to more complex flip-flop functions. For each cell, the logic function and timing are known. A macro-facility is available for user convenience.

SIMON — Logic Simulation

This step checks the logical behavior of the described network against the user specification. The well-proven logic simulator, SIMON, is used to simulate the response of the network on the user-supplied input stimuli. SIMON is an event-driven logic simulator with variable gate delay and uses five logic values (HIGH, LOW, UNKNOWN, etc.).

If the response of the simulated network does not comply with the user specification, the network has to be corrected and simulated again.

INGATE, Cell Placement and Routing

The INGATE step takes care of cell placement and automatic routing in accordance with the logic network description. The gate array cells used in the network have to be placed on the chip area in rows. The special construction of the cells results in very efficient use of the available chip area. The INGATE program calculates the wiring for the entire chip using only two mask steps (contacts and aluminum). User interaction is possible and useful for extremely dense circuits.

When large signal tracks occur on a chip, the capacitance of these can increase the fan-out driven by a gate output. This extra fan-out is computed in the INGATE program and can be fed back for use in the SIMON program to calculate the extra delay values that are necessary.

Mask-Making

The INGATE program interfaces directly with the CIRCUIT MASK program, which produces the control tapes for the mask generators for the two masks.

Testing

The logic simulator enables the fault coverage and efficiency of the user-supplied test sequences to be determined. The program interfaces with a test generation program that adds the d.c. parametric test and generates the control tapes to enable testing on any of the equipment used in the CAD program.

This equipment includes the following:

- Sentry VII
- Sentry 21

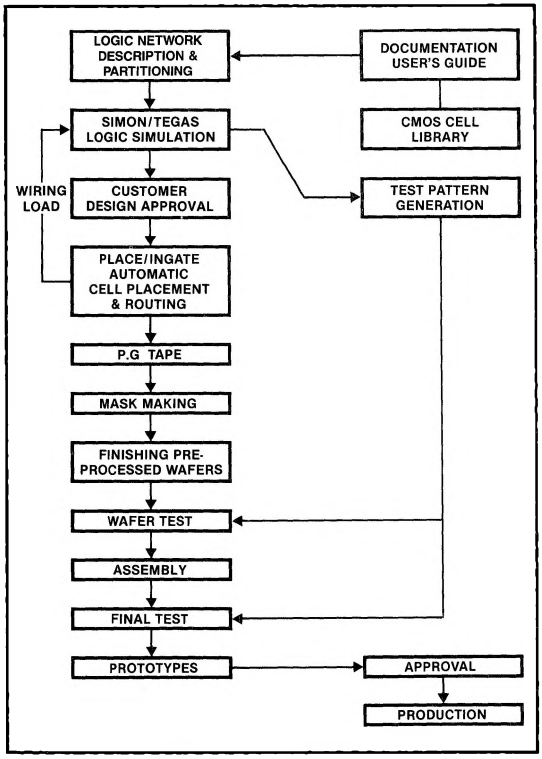


Figure 14. Development Flow

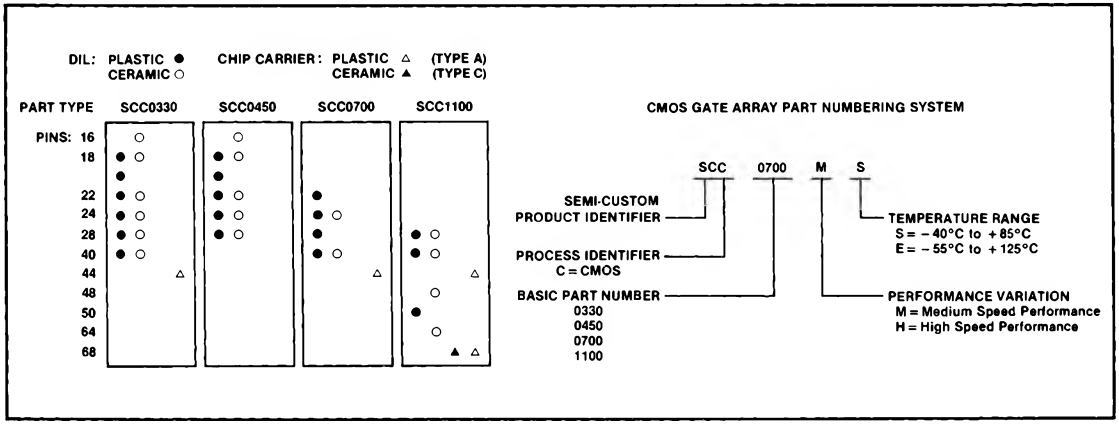
DESIGN PROCEDURE

Gate Count

The following step-by-step procedure is intended to guide the designer in determining the correct gate count.

- Simplify the logic circuit.
- Prepare a detailed logic drawing using only library cells provided in this data sheet.
- Expand all MSI functions to the level of gates and flip-flops (see e.g. the logic diagrams HE4000B family).
- Eliminate all unused functions and simplify the complex functions. Standard off-the-shelf products e.g. up/down counters, programmable counters and latches are often devices for considerable simplification.
- Partition the logic into several sections based on the pattern of interconnecting wiring. Circuits with numerous interconnections should be grouped together and interconnections between groups should be kept to a minimum.
- Examine the logic to see if complex functions can be used to reduce the gate count. Reduction can be achieved by using GF.. functions and eliminating unnecessary inversions.
- Rearrange the logic into the library cells. When fan-out is more than 10 to 15, add or use buffers to minimize delays.
- One "equivalent gate" is a 2-input device.
- A rough estimate count can quickly be made by using HE4000B family gate count table.
- Sequential logic is more desirable as extensive, random interconnection yields a lower utilization factor. In addition, regular LSI functions, such as memories, may lead to inefficient use of a gate array.

PACKAGING INFORMATION AND PART NUMBERING SYSTEM



GATE COUNT FOR HE400B FAMILY

A gate count is given below of 98 different devices that are described in the HE4000B CMOS Family Databook.

Only the gates to be implemented in the array area are given.

The connections to the 'outside world' are via the inputs or outputs located in the periphery area (among the bonding pads).

Preliminary list (use for indication only)

TYPE NUMBER	NUMBER OF EQUIV. GATES	TYPE NUMBER	NUMBER OF EQUIV. GATES
HEF4000B	4	HEF4502B	6
HEF4001UB	4	HEF4508B	12
HEF4002B	4	HEF4510B	82
HEF4006B	76	HEF4511B	49
HEF4007B	▲	HEF4512B	26
HEF4008B	45	HEF4514B	60
HEF4011UB	4	HEF4515B	60
HEF4012B	4	HEF4516B	82
HEF4013B	14	HEF4517B	552
HEF4014B	57	HEF4518B	58
HEF4015B	41	HEF4519B	27
HEF4017B	38	HEF4520B	54
HEF4018B	57	HEF4521B*	128
HEF4019B	8	HEF4522B	62
HEF4020B	70	HEF4526B	62
HEF4021B	73	HEF4527B	60
HEF4022B	31	HEF4528B	—
HEF4023B	6	HEF4531B	36
HEF4024B	35	HEF4532B	24
HEF4025B	6	HEF4534B	—
HEF4027B	22	HEF4539B	24
HEF4028B	23	HEF4541B**	100
HEF4029B	75	HEF4543B	65
HEF4030B	12	HEF4555B	16
HEF4031B	277	HEF4556B	16
HEF4035B	46	HEF4557B	360
HEF4040B	61	HEF4585B	40
HEF4041B	▲	HEF4724B	52
HEF4042B	11	HEF4731B; V	1064
HEF4043B	8	HEF4737B; V	—
HEF4044B	8	HEF40097B	▲
HEF4047B	—	HEF40098B	▲
HEF4049B	▲	HEF40106B	▲
HEF4050B	▲	HEF40160B	54
HEF4068B	6	HEF40161B	54
HEF4069UB	▲	HEF40162B	52
HEF4070B	12	HEF40163B	52
HEF4071B	8	HEF40174B	34
HEF4072B	6	HEF40175B	24
HEF4073B	6	HEF40192B	68
HEF4075B	6	HEF40193B	68
HEF4076B	30	HEF40194B	64
HEF4077B	12	HEF40195B	40
HEF4078B	6	HEF40240B	▲
HEF4081B	8	HEF40244B	▲
HEF4082B	4	HEF40245B	▲
HEF4085B	8	HEF40373B	16
HEF4086B	8	HEF40374B	32
HEF4093B	▲		
HEF4094B	54		

*Excluding V'_{DD} and V'_{SS}
**Excluding power-on reset
▲Located in the periphery