Signetics

NE/SE5018
8-Bit μP-Compatible D/A Converter

Product Specification

Linear Products

DESCRIPTION

The NE/SE5018/19 is a complete 8-bit digital-to-analog converter subsystem on one monolithic chip. The data inputs have input latches which are controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal) and high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full-scale while maintaining a low temperature coefficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

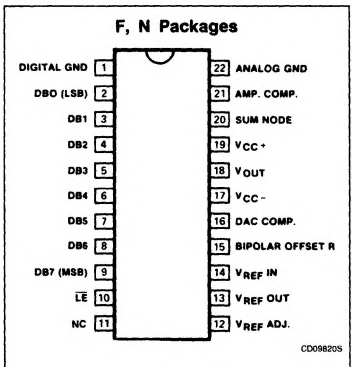
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± ½ LSB (0.19%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 8085, 6800 and many other μPs**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog – digital multiplication**

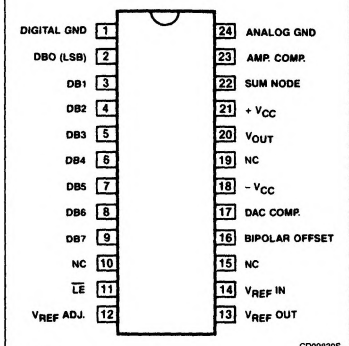
PIN CONFIGURATIONS

F, N Packages



CD09820S

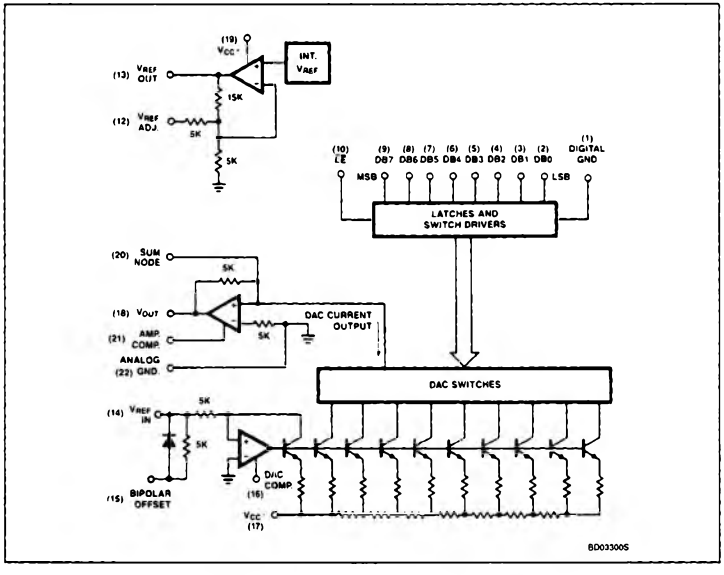
D Package[1]



CD09830S

NOTE:
1. SOL and non-standard pinout.

BLOCK DIAGRAM



BD03300S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
22-Pin Cerdip	0 to +70°C	NE5018F
22-Pin Cerdip	−55°C to +125°C	SE5018F
22-Pin Plastic DIP	0 to +70°C	NE5018N
22-Pin Plastic DIP	−55°C to +125°C	SE5018N
24-Pin SOL Package	0 to +70°C	NE5018D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF\ IN}$	Voltage at V_{REF} input	12	V
V_{REF} ADJ	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
$I_{REF\ SC}$	Short-circuit current to ground at $V_{REF\ OUT}$	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1] F package N package D package	 1740 2190 1600	 mW mW mW
T_A	Operating temperature range SE5018 NE5018	 −55 to +125 0 to +70	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

NOTES:
1. Derate above 25°C at the following rates:
   F package at 13.9mW/°C.
   N package at 17.5mW/°C.
   D package at 12.8mW/°C.

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5018. $-55°C \leq T_A \leq 125°C$, NE5018. $0°C \leq T_A \leq 70°C$, unless otherwise specified.[1] Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SE5018			NE/SE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.19			±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	μA
V_{FS}	Full-scale output	Unipolar mode, $V_{REF} = 5.000V$, all bits high, $T_A = 25°C$	9.50		10.5	9.50		10.5	V
$+V_{FS}$	Full-scale output	Bipolar mode, $V_{REF} = 5.000V$ all bits high, $T_A = 25°C$	4.75		5.25	4.75		5.25	V
$-V_{FS}$	Negative full scale	Bipolar mode, $V_{REF} = 5.000V$, all bits low, $T_A = 25°C$	−5.25		−4.75	−5.25		−4.75	V
V_{ZS}	Zero-scale Output	Unipolar mode, $V_{REF} = 5.000V$ all bits low, $T_A = 25°C$	−30		+30	−30		+30	mV
I_{OS}	Output short circuit current	$T_A = 25°C$, $V_{OUT} = 0V$		15	40		15	40	mA
$PSR+_{(OUT)}$	Output power supply rejection (+)	V− = −15V, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		0.001	0.01		0.001	0.01	%FS %VS
$PSR-_{(OUT)}$	Output power supply rejection (−)	V+ = +15V, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		0.001	0.01		0.001	0.01	%FS %VS
TC_{FS}	Full-scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20			20		ppm/°C
TC_{ZS}	Zero-scale temperature coefficient			5			5		ppm/°C
I_{REF}	Reference output current				3			3	mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$[8], $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	V− = −15V, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		0.003	0.01		0.003	0.01	%VR/%VS
$PSR-_{(REF)}$	Reference power supply rejection (−)	V+ = −15V, $-13.5V \leq V- \leq 16.5V$,		0.003	0.01		0.003	0.01	%VR/%VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$ $T_A = 25°C$	4.9	5.0	5.25	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC $V_{REF\ IN}$ input impedance	$I_{REF} = 1.0mA$, $T_A = 25°C$	4.15	5.0	5.85	4.15	5.0	5.85	kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

NOTE:
1. Refer to Figure 2.

AC ELECTRICAL CHARACTERISTICS[1] V_{CC} = ± 15V, T_A = 25°C.

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	NE/SE5018/19			UNIT
					Min	Typ	Max	
t_{SLH}	Settling time	± ½ LSB	Input	All bits low-to-high[2]		1.8		μs
t_{SHL}	Settling time	± ½ LSB	Input	All bits high-to-low[3]		2.3		μs
t_{PLH}	Propagation delay	Output	Input	All bits switched low-to-high[2]		300		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched high-to-low[3]		150		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change[2, 3]		150		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-high transition[4]		300		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-low transition[5]		150		ns
t_S	Setup time	$\overline{LE}$	Input	1, 6	100			ns
t_H	Hold time	Input	$\overline{LE}$	1, 6	50			ns
t_{PW}	Latch enable pulse width			1, 6	150			ns

NOTES:
1. Refer to Figure 3.
2. See Figure 6.
3. See Figure 7.
4. See Figure 8.
5. See Figure 9.
6. See Figure 10.
7. For reference currents > 3mA, use of an external buffer is required.

8-Bit μP-Compatible D/A Converter — NE/SE5018

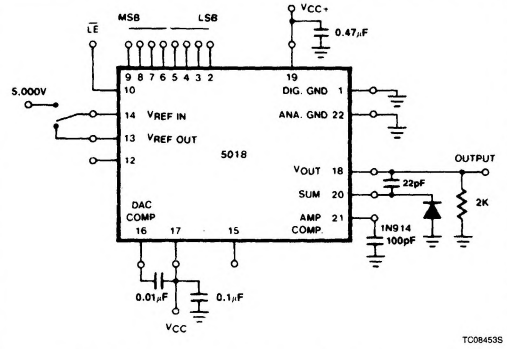


Figure 2. DC Parametric Test Configuration

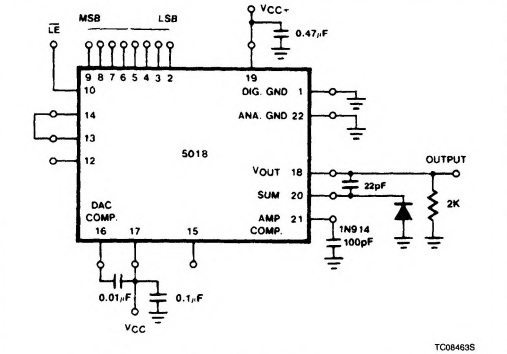


Figure 3. AC Parametric Test Configuration

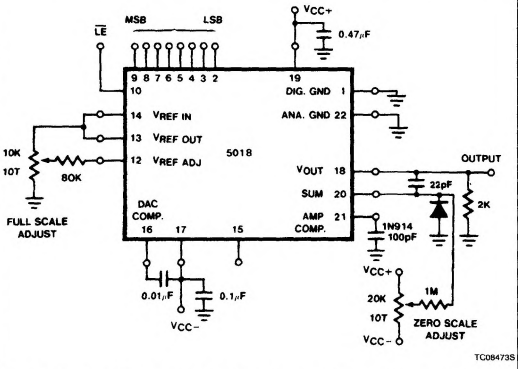


Figure 4. Full-/Zero-Scale Adjust — Unipolar Output (0 – 10V)

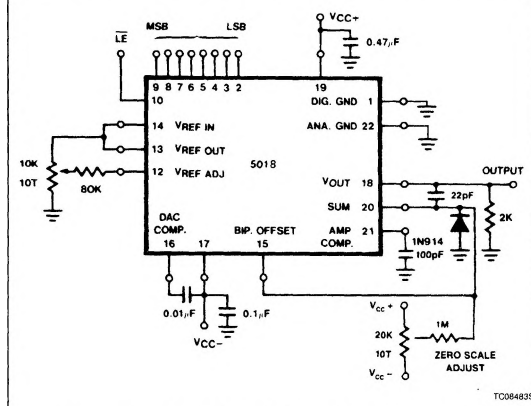


Figure 5. Bipolar Output Operation (−5 to +5V)

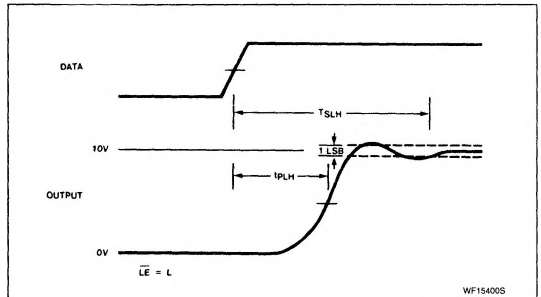


Figure 6. Settling Time and Propagation Delay, Low-to-High Data

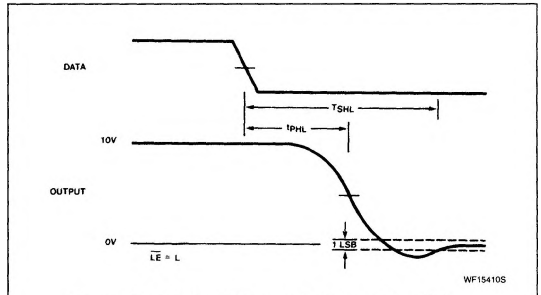


Figure 7. Settling Time and Propagation Delay, High-to-Low Data

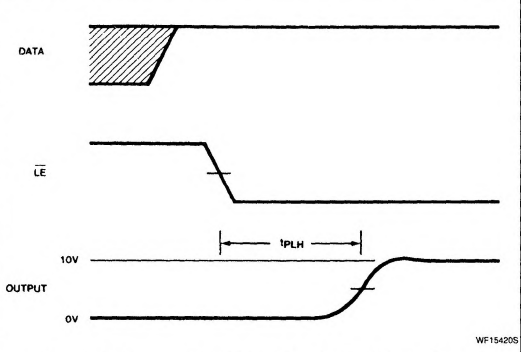


Figure 8. Propagation Delay, Latch Enable to Output

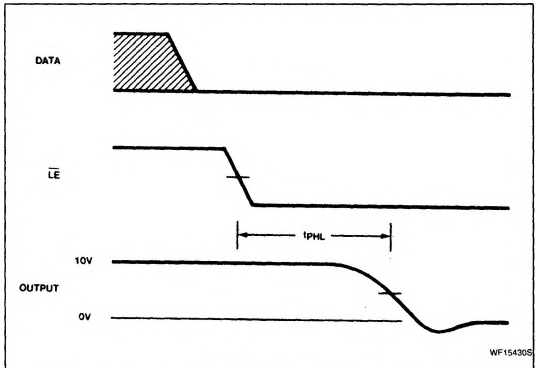


Figure 9. Propagation Delay, Latch Enable to Output

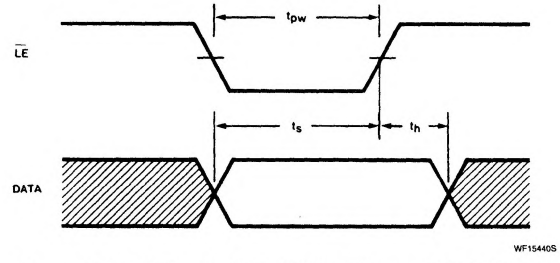


Figure 10. Latch Enable Pulse Width, Setup and Hold Times