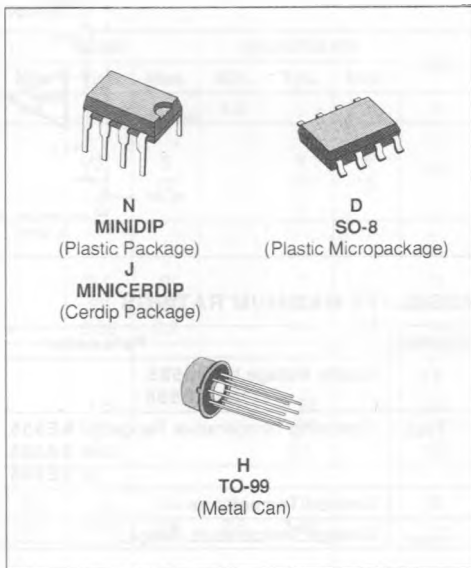


PRECISION TIMERS

- LOW TURN OFF TIME
- MAXIMUM OPERATING FREQUENCY GREATER THAN 500Hz
- TIMING FROM MICROSECONDS TO HOURS
- OPERATES IN BOTH ASTABLE AND MONO-STABLE MODES
- HIGH OUTPUT CURRENT CAN SOURCE OR SINK 200mA
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.005% PER °C

DESCRIPTION

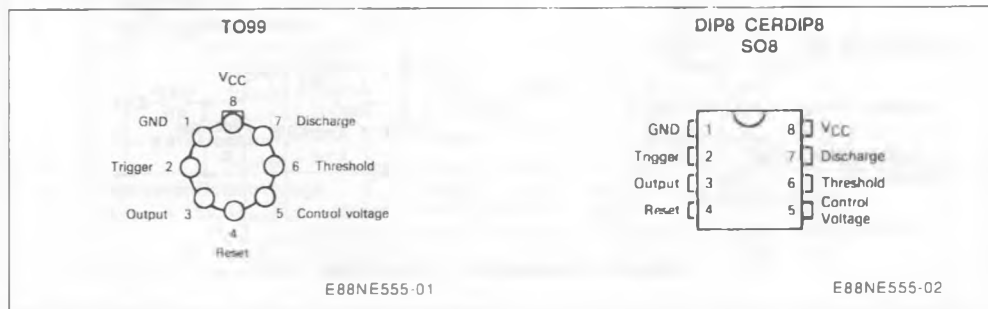
The NE555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA. The NE555 is available in plastic and ceramic minidip package and in a 8-lead micropackage and in metal can package version.



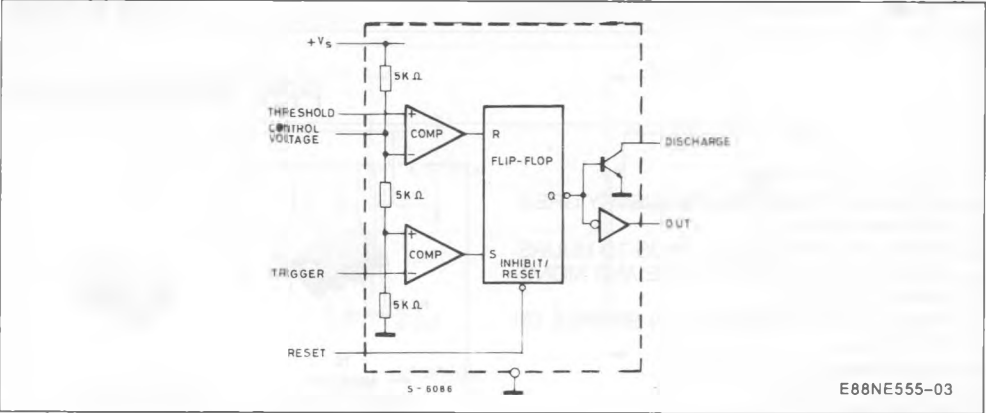
ORDER CODES

Part Number	Temperature Range	Package			
		H	N	J	D
NE555	0°C to 70°C	•	•	•	•
SA555	- 40°C to 105°C	•	•	•	•
SE555	- 55°C to 125°C	•			

PIN CONNECTION (top views)



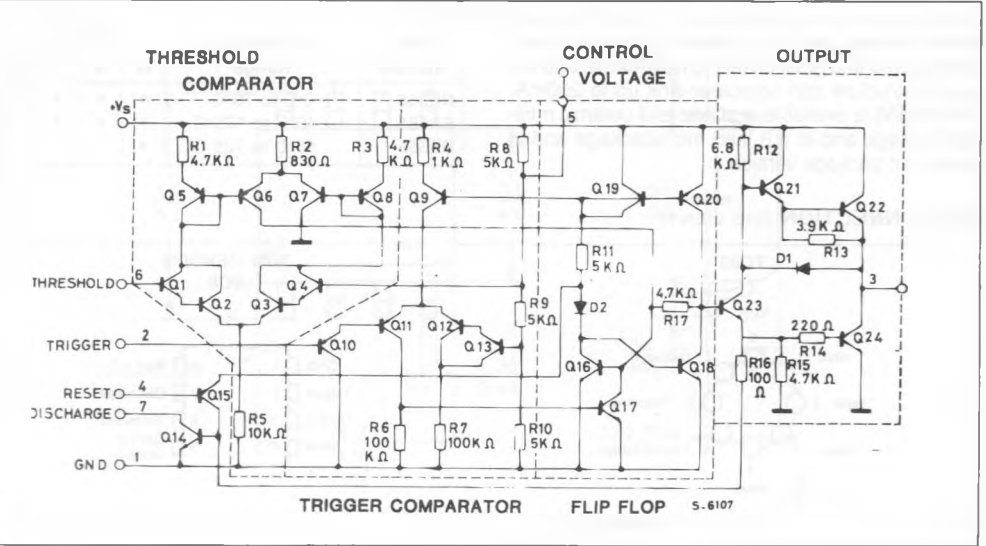
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage for SE555 for NE555	18 16	V
T_{op}	Operating Temperature Range for NE555 for SA555 for SE555	0 to 70 - 40 to 105 - 55 to 125	°C
T_j	Junction Temperature	150	°C
T_{sig}	Storage Temperature Range	- 65 to 150	°C

SCHEMATIC DIAGRAM



THERMAL DATA

			Plastic Dip	Ceramic Dip	SO8	Metal Can
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	max.	120°C/W	150°C/W	200°C/W	155°C/W

ELECTRICAL CHARACTERISTICS

$T_{amb} = +25^{\circ}\text{C}$, $V_S = +5\text{V}$ to $+15\text{V}$ (unless otherwise specified)

Symbol	Parameter	SE555			NE555/SA555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CC}	Supply Voltage	4.5		18	4.5		16	V
I_S	Supply Current ($R_L = \infty$) Note 1 Low State $V_{CC} = +5\text{V}$ $V_{CC} = +15\text{V}$ High State $V_{CC} = 5\text{V}$		3 10 2	5 12		3 10 2	6 15	mA
	Timing Error (monostable) ($R_A = 2$ to $100\text{k}\Omega$, $C = 0.1\mu\text{F}$) Initial Accuracy (note 2) Drift with Temperature Drift with Supply Voltage		0.5 30 0.05	2 100 0.2		1 50 0.1	3 ppm/ $^{\circ}\text{C}$ %/V	
	Timing Error (astable) ($R_A, R_B = 1\text{k}\Omega$ to $100\text{k}\Omega$, $C = 0.1\mu\text{F}$, $V_S = +15\text{V}$) initial Accuracy (note 2) Drift with Temperature Drift with Supply Voltage		1.5 90 0.15			2.25 150 0.3	% ppm/ $^{\circ}\text{C}$ %/V	
V_{CL}	Control Voltage level $V_{CC} = +15\text{V}$ $V_{CC} = +5\text{V}$	9.6 2.9	10 3.33	10.4 3.8	9 2.6	10 3.33	11 4	V
V_{th}	Threshold Voltage $V_{CC} = +15\text{V}$ $V_{CC} = +5\text{V}$	9.4 2.7	10 3.33	10.6 4	8.8 2.4	10 3.33	11.2 4.2	V
I_{th}	Threshold Current (note 3)		0.1	0.25		0.1	0.25	μA
V_{trig}	Trigger Voltage $V_{CC} = +15\text{V}$ $V_{CC} = +5\text{V}$	4.8 1.45	5 1.67	5.2 1.9	4.5 1.1	5 1.67	5.6 2.2	V
I_{trig}	Trigger Current ($V_{trig} = 0\text{V}$)		0.5	0.9		0.5	2.0	μA
V_{reset}	Reset Voltage (note 4)	0.4	0.7	1	0.4	0.7	1	V
I_{reset}	Reset Current $V_{reset} = +0.4\text{V}$ $V_{reset} = 0\text{V}$		0.1 0.4	0.4 1		0.1 0.4	0.4 1.5	mA
V_{OL}	Low Level Output Voltage $V_{CC} = +15\text{V}$, $I_{O(sink)} = 10\text{mA}$ $I_{O(sink)} = 50\text{mA}$ $I_{O(sink)} = 100\text{mA}$ $I_{O(sink)} = 200\text{mA}$ $V_{CC} = +5\text{V}$, $I_{O(sink)} = 8\text{mA}$ $I_{O(sink)} = 5\text{mA}$		0.1 0.4 2 2.5 0.1 0.05	0.15 0.5 2.2		0.1 0.4 2 2.5 0.3 0.25	0.25 0.75 2.5 0.4 0.35	V
V_{OH}	High Level Output Voltage $V_{CC} = +15\text{V}$, $I_{O(source)} = 200\text{mA}$ $I_{O(source)} = 100\text{mA}$ $V_{CC} = +5\text{V}$, $I_{O(source)} = 100\text{mA}$	13 3	12.5 13.3 3.3		12.75 2.75	12.5 13.3 3.3		V

ELECTRICAL CHARACTERISTICS(continued)

Symbol	Parameter	SE555			NE555/SA555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$I_{dis(off)}$	Discharge Pin Leakage Current (output high)		20	100		20	100	nA
$V_{dis(sat)}$	Discharge pin Saturation Voltage (output low) (note 5) $V_{CC} = +15V, I_{dis} = 15mA$ $V_{CC} = +5V, I_{dis} = 4.5mA$		180 80	480 200		180 80	480 200	mV
t_r t_f	Output Rise Time Output Fall Time		100 100	200 200		100 100	300 300	ns
t_{off}	Turn off Time (note 6), $V_{reset} = V_{CC}$		0.5			0.5		μs

- Notes :
- 1. Supply current when output is high is typically 1 mA less
 - 2. Tested at $V_S = +5V$ and $V_S = +15V$
 - 3. This will determine the maximum value of $R_A + R_B$ for +15V operation the max total is $R = 20M\Omega$ and for 5V operation, the max total $R = 3.5M\Omega$
 - 4. Specified with trigger input high
 - 5. No protection against excessive Pin 7 current is necessary, providing the package dissipation rating will not be exceeded
 - 6. Time measured from a positive going input pulse from 0 to 0.8xVS into the threshold to the drop from high to Low of the output trigger is tied to threshold.

Figure 1 : Minimum Pulse Width Required for Tri-gering.

Figure 2 : Supply Current Vs. Supply Voltage.

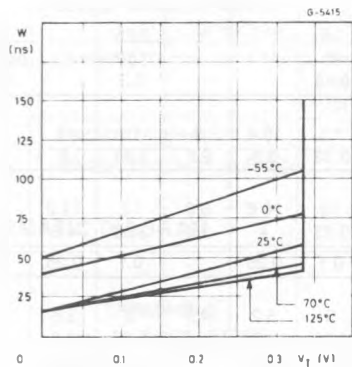


Figure 3 : Delay Time Vs. Temperature.

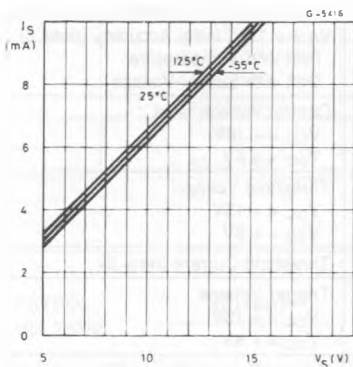


Figure 4 : Low Output Voltage Vs. Output Sink Current.

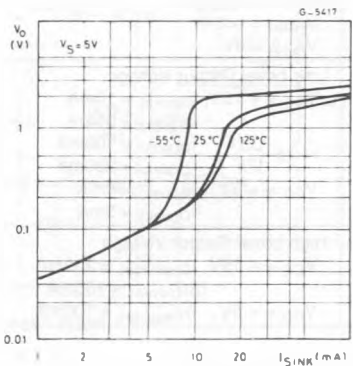
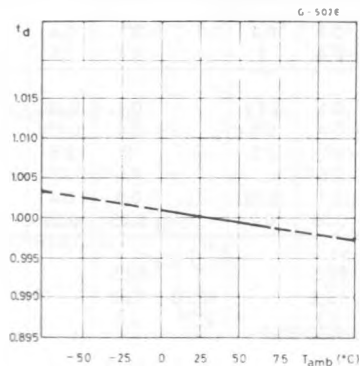
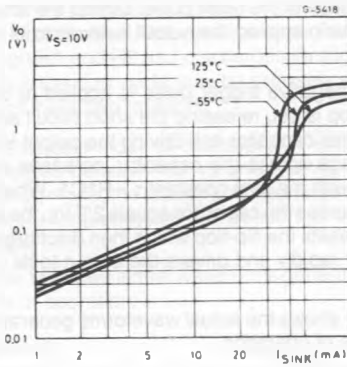
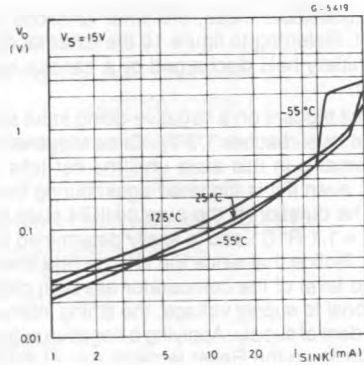
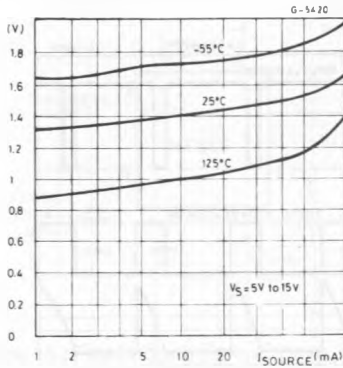
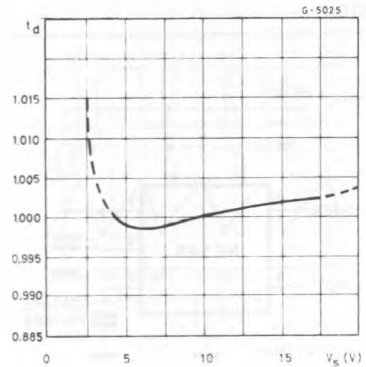
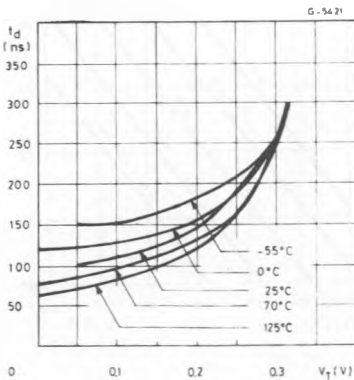


Figure 5 : Low Output Voltage Vs. Output Sink Current.**Figure 6 : Low Output Voltage Vs. Output Sink Current.****Figure 7 : High Output Voltage Drop Vs. Output Source Current.****Figure 8 : Delay Time Vs. Supply Voltage.****Figure 9 : Propagation Delay Vs. Voltage Level of Trigger Value.**

APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one-shot. Referring to figure 10 the external capacitor is initially held discharged by a transistor inside the timer.

The circuit triggers on a negative-going input signal when the level reaches $1/3 V_S$. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by $t = 1.1 R_1 C_1$ and is easily determined by figure 12. Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (pin 4) and the Trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant $\tau = R_1 C_1$. When the voltage across the capacitor equals $2/3 V_S$, the comparator resets the flip-flop which then discharge the capacitor rapidly and drives the output to its LOW state.

Figure 11 shows the actual waveforms generated in this mode of operation.

When Reset is not used, it should be tied high to avoid any possibly or false triggering.

Figure 10.

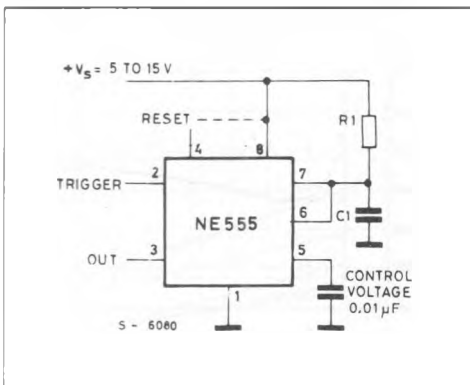


Figure 11.

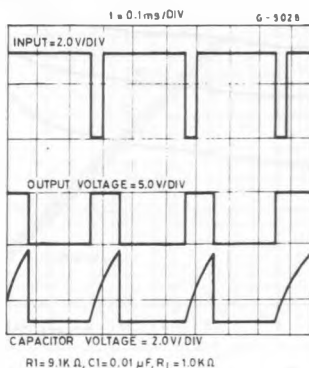
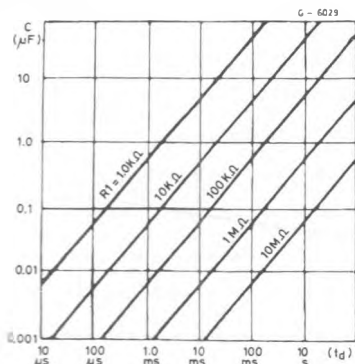


Figure 12.



ASTABLE OPERATION

When the circuit is connected as shown in figure 13 (pin 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R1 and R2 and discharges through R2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C1 charges and discharges between $1/3 V_S$ and $2/3 V_S$. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 14 shows actual waveforms generated in this mode of operation.

Figure 13.

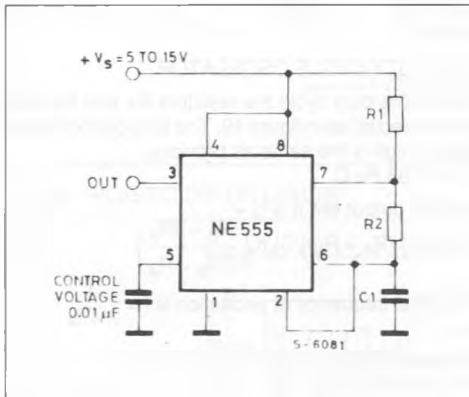
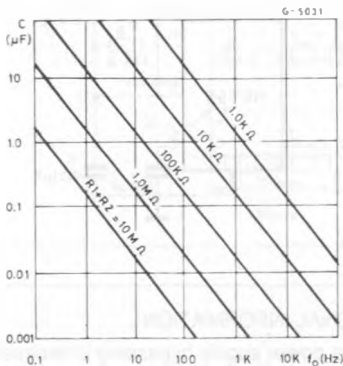


Figure 15 : FreeRunning Frequency vs. R1, R2, and C1.



The charge time (output HIGH) is given by :

$$t_1 = 0.693 (R_1 + R_2) C_1$$

and the discharge time (output LOW) by :

$$t_2 = 0.693 (R_2) C_1$$

Thus the total period T is given by :

$$T = t_1 + t_2 = 0.693 (R_1 + 2R_2) C_1$$

The frequency of oscillation is then :

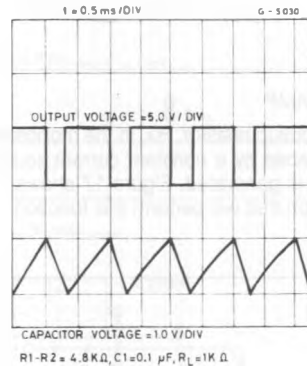
$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2) C_1}$$

and may be easily found by figure 15.

The duty cycle is given by :

$$D = \frac{R_2}{R_1 + 2R_2}$$

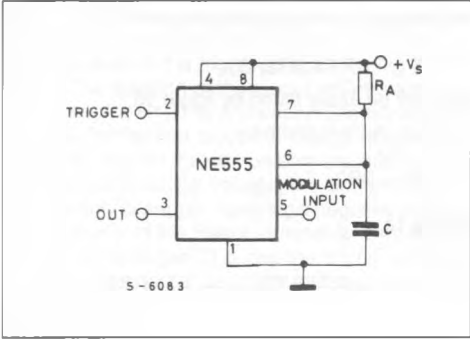
Figure 14.



PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. Figure 16 shows the circuit.

Figure 16 : Pulse Width Modulator.



LINEAR RAMP

When the pullup resistor, R_A , in the monostable circuit is replaced by a constant current source, a linear ramp is generated. Figure 17 shows a circuit configuration that will perform this function.

Figure 17.

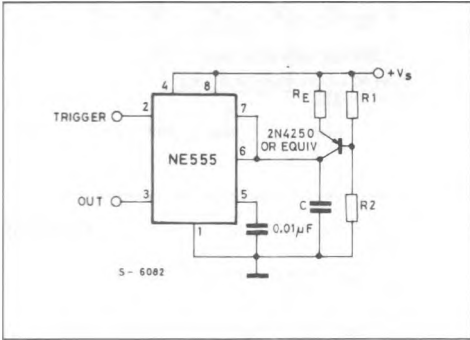


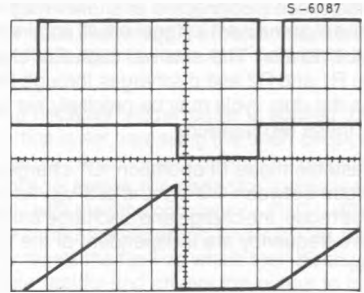
Figure 18 shows waveforms generator by the linear ramp.

The time interval is given by :

$$T = \frac{2/3 V_S R_E (R_1 + R_2) C}{R_1 V_S - V_{BE} (R_1 + R_2)} \quad V_{BE} = 0.6V$$

Note that this circuit will not oscillate if R_B is greater than $1/2 R_A$ because the junction of R_A and R_B cannot bring pin 2 down to $1/3 V_S$ and trigger the lower comparator.

Figure 18 : Linear Ramp.



$V_S = 5V$
 $TIME = 20\mu s/DIV$
 $R_1 = 47K\Omega$
 $R_2 = 100K\Omega$
 $R_E = 2.7K\Omega$
 $C = 0.01\mu F$
 Top trace : input 3V/DIV
 Middle trace : output 5V/DIV
 Bottom trace : output 5V/DIV
 Bottom trace : capacitor voltage 1V/DIV

50% DUTY CYCLE OSCILLATOR

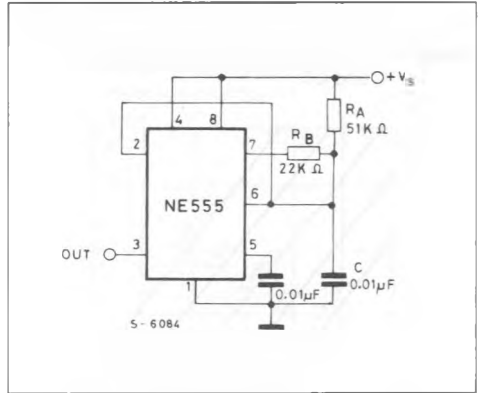
For a 50% duty cycle the resistors R_A and R_B may be connected as in figure 19. The time period for the output high is the same as previous, $t_1 = 0.693 R_A C$.

For the output low it is $t_2 =$

$$[(R_A R_B)/(R_A + R_B)] C \ln \left\{ \frac{R_B - 2R_A}{2R_B - R_A} \right\}$$

Thus the frequency of oscillation is $f = \frac{1}{t_1 + t_2}$

Figure 19 : 50% Duty Cycle Oscillator.

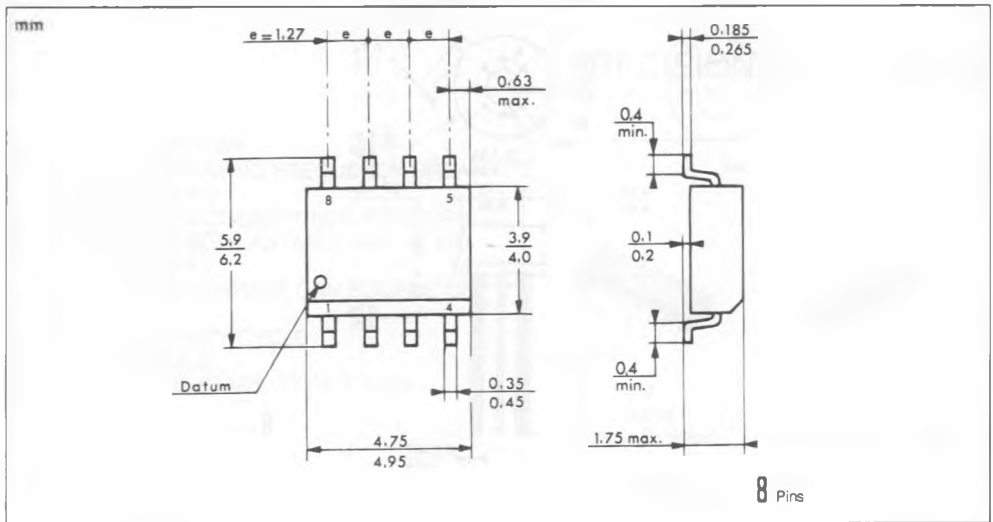


ADDITIONAL INFORMATION

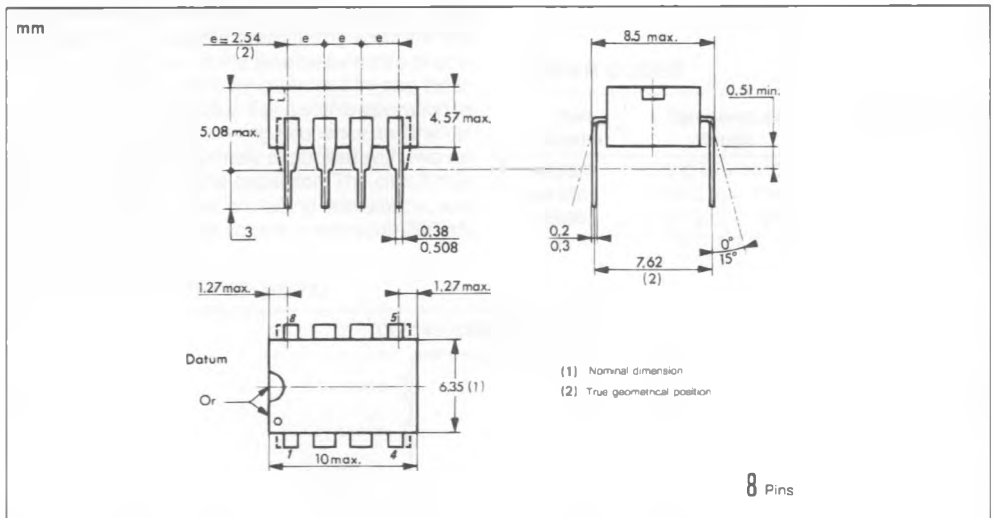
Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is $0.1\mu F$ in parallel with $1\mu F$ electrolytic.

PACKAGE MECHANICAL DATA

8 PINS – PLASTIC MICROPACKAGE (SO)



8 PINS – PLASTIC DIP OR Cerdip



8 PINS – METAL CAN TO 99

