

## **FEATURES**

- High-voltage start-up
- Low operating current (4mA)
- Linearly decreasing PWM frequency to 22KHz
- Frequency jittering to reduce EMI emission
- Fixed PWM frequency (65KHz)
- Peak-current-mode control
- Cycle-by-cycle current limiting
- Leading-edge blanking
- Synchronized slope compensation
- Internal open-loop protection
- GATE output maximum voltage clamp (18V)
- V<sub>DD</sub> under-voltage lockout (UVLO)
- $\blacksquare$  V<sub>DD</sub> over voltage protection (OVP)
- Programmable over-temperature protection (RT)
- Internal latch circuit (OVP, RT)
- Constant power limit (full AC input range)
- Internal OTP sensor with hysteresis

## **APPLICATIONS**

General-purpose switch-mode power supplies and flyback power converters, including:

- Power Adapters
- Open-Frame SMPS

## DESCRIPTION

The highly integrated SG6742 series of PWM controllers provides several features to enhance the performance of flyback converters.

## **TYPICAL APPLICATION**



To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency at light-load conditions. To avoid acoustic noise problems, the minimum PWM frequency is set above 22KHz. This green-mode function enables the power supply to meet international power conservation requirements. With the internal high-voltage start-up circuitry, the power loss due to bleeding resistors is eliminated. To further reduce power consumption, SG6742 is manufactured using the BiCMOS process, which allows an operating current of 4mA.

SG6742 integrates a frequency a hopping function that helps reduce EMI emission of a power supply with minimum line filters. Also, its built-in synchronized slope compensation achieves stable peak-current-mode control. The proprietary internal line compensation ensures constant output power limit over a wide AC input voltages, from  $90V_{AC}$  to  $264V_{AC}$ .

SG6742 provides many protection functions. In addition to cycle-by-cycle current limiting, the internal open-loop protection circuit ensures safety should an open-loop or output short-circuit failure occur. PWM output is disabled until  $V_{DD}$  drops below the UVLO lower limit when the controller starts up again. As long as  $V_{DD}$  exceeds about 26V, the internal OVP circuit is triggered.

SG6742 is available in an 8-pin DIP or SOP package.



**PIN CONFIGURATION** 

#### Highly Integrated Green-Mode PWM Controller

#### SG6742

## MARKING INFORMATION



## **ORDERING INFORMATION**

Part Number	<b>PWM Frequency</b>	Pb-Free	Package	
SG6742SZ	65KHz		SOP-8	
SG6742DZ (Preliminary)	65KHz		DIP-8	

## **PIN DESCRIPTIONS**

	SCINF I		
Pin No.	Symbol	Function	Description
1	GND	Ground	Ground.
2	FB	Feedback	The signal from the external compensation circuit is fed into this pin. The PWM duty cycle is determined in response to the signal on this pin and the current-sense signal on SENSE pin.
3	NC	NA	NC pin.
4	HV	Start-up Input	For start-up, this pin is pulled high to the line input or bulk capacitor via resistors.
5	RT	Temperature Detection	For over-temperature protection, an external NTC thermistor is connected from this pin to GND pin. The impedance of the NTC decreases at high temperatures. Once the voltage of the RT pin drops below a fixed limit, PWM output is disabled.
6	SENSE	Current Sense	Current sense. The sensed voltage is used for peak-current-mode control and cycle-by-cycle current limiting.
7	VDD	Power Supply	Power supply. The internal protection circuit disables PWM output as long as $V_{\text{DD}}$ exceeds the OVP trigger point.
8	GATE	Driver Output	The totem-pole output driver. Soft driving waveform is implemented for improved EMI.



**Product Specification** 

#### SG6742

## **BLOCK DIAGRAM**





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## **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter			Value		Unit
V <sub>DD</sub>	Supply Voltage	Supply Voltage				V
V <sub>HV</sub>	Input Voltage to HV Pin			500		V
VL	Input Voltage to FB, SENSE, CS Pin			-0.3 to 7.	0	V
0				DIP	800	144
PD	Power Dissipation $T_A < 50^{\circ}C$			SOP	400	mW
<b>_</b>						°0444
$R_{\Theta JA}$	Thermal Resistance (Junction-to-Air)			SOP	141.0	
TJ	Operating Junction Temperature			-40 to +125		°C
T <sub>STG</sub>	Storage Temperature Range				50	°C
TL	Lead Temperature (Wave Soldering or Infrared, 10 Seconds)					°C
	Electrostatic Discharge Capability, Human Body Model All pins except HV pin					KV
ESD	Electrostatic Discharge Capability, Machine Model	All pins except HV	pin	400		V

\* All voltage values, except differential voltages, are given with respect to the GND pin.

\* Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

# **ELECTRICAL CHARACTERISTICS**

 $V_{DD} = 15V$ ;  $T_A = 25^{\circ}C$ , unless otherwise noted.

## **V**<sub>DD</sub> Section

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
V <sub>DD-OP</sub>	Continuously Operating Voltage				22	V
V <sub>DD-ON</sub>	Start Threshold Voltage		15.5	16.5	17.5	V
V <sub>DD-OFF</sub>	Minimum Operating Voltage		9.5	10.5	11.5	V
I <sub>DD-ST</sub>	Start-up Current	V <sub>DD-ON</sub> – 0.16V			30	μA
I <sub>DD-OP</sub>	Operating Supply Current	V <sub>DD</sub> = 15V, GATE open		4	5	mA
IDD-OLP	Internal Sink Current	V <sub>TH-OLP</sub> +0.1V	50	70	90	μA
V <sub>TH-OLP</sub>	I <sub>DD-OLP</sub> Off Voltage		6.5	7.5	8.0	V
V <sub>DD-OVP</sub>	V <sub>DD</sub> Over-Voltage Protection		25	26	27	V
t <sub>D-VDDOVP</sub>	V <sub>DD</sub> Over-Voltage Protection Debounce Time		75	125	200	μs

## **HV Section**

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
I <sub>HV</sub>	Supply Current Drawn from HV Pin	V <sub>AC</sub> =90V (V <sub>DC</sub> =120V) ; V <sub>DD</sub> =10μF		1.2		mA
I <sub>HV-LC</sub>	II eakage Current After Start-up	$HV = 500V,$ $V_{DD} = V_{DD-OFF} + 1V$		1	20	μA



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## **Oscillator Section**

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
-	Fraguency in Newinel Mede	Center Frequency	62	65	68	
Fosc	Frequency in Nominal Mode	Hopping Range	±3.7	±4.2	±4.7	-KHz
t <sub>HOP</sub>	Hopping Period			4.4		ms
F <sub>OSC-G</sub>	Green-Mode Frequency		18	22	25	KHz
F <sub>DV</sub>	Frequency Variation vs. V <sub>DD</sub> Deviation	V <sub>DD</sub> =11V to 22V			5	%
F <sub>DT</sub>	Frequency Variation vs. Temp. Deviation	T <sub>A</sub> =-20 to 85°C			5	%

\* Hopping off at green-mode.

# **Feedback Input Section**

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
Av	Input Voltage to Current-Sense Attenuation		1/4.5	1/4.0	1/3.5	V/V
Z <sub>FB</sub>	Input Impedance		4		7	kΩ
V <sub>FB-OPEN</sub>	Output High Voltage	FB pin open	5.5			V
V <sub>FB-OLP</sub>	FB Open-Loop Trigger Level		5.0	5.2	5.4	V
t <sub>D-OLP</sub>	Delay Time of FB Pin Open Loop Protection		53	56	59	ms
V <sub>FB-N</sub>	Green-Mode Entry FB Voltage		1.9	2.1	2.3	V
V <sub>FB-G</sub>	Green-Mode Ending FB Voltage			V <sub>FB-N</sub> -0.5		V





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## **Current-Sense Section**

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
Z <sub>SENSE</sub>	Input Impedance			12		ΚΩ
VSTHFL	Current Limit Flatten Threshold Voltage		0.87	0.90	0.93	V
V <sub>STHVA</sub>	Current Limit Valley Threshold Voltage	V <sub>STHFL</sub> -V <sub>STHVA</sub>	0.18	0.22	0.26	V
t <sub>PD</sub>	Delay to Output			100	200	ns
t <sub>LEB</sub>	Leading-Edge Blanking Time		275	350	425	ns
V <sub>S-SCP</sub>	Threshold Voltage for SENSE Short-circuit Protection		0.10	0.15	0.20	v
t <sub>D-SSCP</sub>	Delay Time for SENSE Short-circuit Protection	V <sub>SENSE</sub> < 0.15V	100	150	200	μs

### GATE Section

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
DCY <sub>MAX</sub>	Maximum Duty Cycle		60	65	70	%
V <sub>GATE-L</sub>	Gate Low Voltage	$V_{DD}$ =15V, I <sub>O</sub> =50mA			1.5	V
V <sub>GATE-H</sub>	Gate High Voltage	$V_{DD}$ =12V, I <sub>O</sub> =50mA	8			V
tr	Gate Rising Time	$V_{DD}$ =15V, C <sub>L</sub> =1nF	150	250	350	ns
tf	Gate Falling Time	$V_{DD}$ =15V, C <sub>L</sub> =1nF	30	50	90	ns
IGATE-SOURCE	Gate Source Current	V <sub>DD</sub> =15V, GATE=6V	250			mA
V <sub>GATE-CLAMP</sub>	Gate Output Clamping Voltage	V <sub>DD</sub> =22V			18	V

# **RT Section**

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
I <sub>RT</sub>	Output Current from the RT Pin		92	100	108	μA
V <sub>RTTH1</sub>	Over-Temperature Protection Threshold	$0.7V < V_{RT} < 1.05V$ , after	1.015	1.050	1.085	v
	Voltage Over-Temperature Protection Threshold	12ms latch off $V_{RT} < 0.7V$ , after 100µs				
V <sub>RTTH2</sub>	Voltage	latch off	0.65	0.70	0.75	V
t <sub>D-OTP1</sub>	Over-Temperature Latch-off Debounce	$V_{RTTH2} < V_{RT} < V_{RTTH1}$	8	12	16	ms
t <sub>D-OTP2</sub>	Over-Temperature Latch-off Debounce	V <sub>RT</sub> < V <sub>RTTH2</sub>	60	100	140	μs

## **Over Temperature Protection (OTP)**

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
T <sub>OTP</sub>	Protection Junction Temperature			135		°C
T <sub>Restart</sub>	Restart Junction Temperature <sup>™</sup>			Т <sub>отр</sub> -25		°C

\* When activated, the output is disabled and the latch is turned off.

\*\* This is the threshold temperature for enabling the output again and resetting the latch after over-temperature protection has been activated.



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## **TYPICAL CHARACTERISTICS**













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Highly Integrated Green-Mode PWM Controller

### **OPERATION DESCRIPTION**

## Start-up Current

For start-up, the HV pin is connected to the line input or bulk capacitor through an external diode and resistor  $R_{HV}$ , which are recommended as 1N4007 and 100K $\Omega$ . Typical start-up current drawn from the HV pin is 1.2mA and it charges the hold-up capacitor through the diode and resistor. When the  $V_{DD}$  capacitor level reaches  $V_{DD-ON}$ , the start-up current switches off. At this moment, the  $V_{DD}$ capacitor only supplies the SG6742 to keep the  $V_{DD}$ before the auxiliary winding of the main transformer to carry on provide the operating current.

## **Operating Current**

Operating current is around 4mA. The low operating current enables better efficiency and reduces the requirement of  $V_{DD}$  hold-up capacitance.

## **Green-Mode Operation**

The proprietary green-mode function provides an off-time modulation to reduce the switching frequency in light-load and no-load conditions. The on-time is limited for better abnormal or brownout protection.  $V_{FB}$ , which is derived from the voltage feedback loop, is taken as the reference. Once  $V_{FB}$  is lower than the threshold voltage, switching frequency is continuously decreased to the minimum green mode frequency, around 22KHz.

## **Current Sensing / PWM Current Limiting**

Peak-current-mode control is utilized to regulate output voltage and provide pulse-by-pulse current limiting. The switch current is detected by a sense resistor into the SENSE pin. The PWM duty cycle is determined by this current sense signal and  $V_{FB}$ , the feedback voltage. When the voltage on the SENSE pin reaches around  $V_{COMP} = (V_{FB}-1.2)/4$ , a switch cycle is terminated immediately.  $V_{COMP}$  is internally clamped to a variable voltage around 0.85V for output power limit.

## Leading-Edge Blanking

Each time the power MOSFET is switched on, a turn-on spike occurs on the sense-resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled and it cannot switch off the gate driver.

## Under-Voltage Lockout (UVLO)

The turn-on and turn-off threshold are fixed internally at 16.5V/10.5V. During start-up, the hold-up capacitor must be charged to 16.5V through the start-up resistor so that IC is enabled. The hold-up capacitor continues to supply  $V_{DD}$  before the energy can be delivered from auxiliary winding of the main transformer.  $V_{DD}$  must not drop below 10.5V during this start-up process. This UVLO hysteresis window ensures that hold-up capacitor is adequate to supply  $V_{DD}$  during start-up.

## Gate Output / Soft Driving

The SG6742 BiCMOS output stage is a fast totem pole gate driver. Cross conduction is avoided to minimize heat dissipation, increases efficiency, and enhances reliability. The output driver is clamped by an internal 18V Zener diode to protect power MOSFET transistors against undesirable gate over voltage. A soft driving waveform is implemented to minimize EMI.

## **Built-in Slope Compensation**

The sensed voltage across the current-sense resistor is used for peak-current-mode control and pulse-by-pulse current limiting. Built-in slope compensation improves stability or prevents sub-harmonic oscillation. SG6742 inserts a synchronized positive-going ramp at every switching cycle.

## **Constant Output Power Limit**

When the SENSE voltage, across the sense resistor Rs, reaches the threshold voltage, around 0.9V, the output GATE drive is turned off after a small delay,  $t_{PD}$ . This delay introduces additional current, proportional to  $t_{PD}$ •V<sub>IN</sub> / L<sub>P</sub>. Since the delay is nearly constant, regardless of the input voltage V<sub>IN</sub>, higher input voltage results in a larger additional current and the output power limit is higher than under low input line voltage. To compensate this variation for wide AC input range, a sawtooth power-limit problem. The power limiter is designed as a positive ramp signal and is fed to the inverting input of the OCP comparator. This results in a lower current limit at high-line inputs than at low-line inputs.



## **V<sub>DD</sub> Over-Voltage Protection**

 $V_{DD}$  over-voltage protection has been built in to prevent damage due to abnormal conditions. Once the  $V_{DD}$  voltage is over the over-voltage protection voltage  $(V_{DD-OVP})$  and lasts for  $t_{D-VDDOVP}$ , the PWM pulses are be disabled until the  $V_{DD}$  voltage drops below the UVLO, then start-up again. Over-voltage conditions are usually caused by open feedback loops.

## **Thermal Protection**

An NTC thermistor  $R_{NTC}$  in series with a resistor  $R_A$  can be connected from pin RT to ground. A constant current  $I_{RT}$  is output from pin RT. The voltage on RT pin can be expressed as  $V_{RT} = I_{RT} \times (R_{NTC} + Ra)$ , in which  $I_{RT} = 2 x$  $(1.3V / R_I)$ . At high ambient temperature,  $R_{NTC}$  is smaller, such that  $V_{RT}$  decreases. When  $V_{RT}$  is less than 1.05V  $(V_{RTTHI})$ , the PWM is turned off after 12ms (t<sub>D-OTPI</sub>). If  $V_{RT}$  is less than 0.7V ( $V_{RTTH2}$ ), PWM should be turned off immediately after 100µs (t<sub>D-OTP2</sub>).

## **Limited Power Control**

The FB voltage increases every time the output of the power supply is shorted or over-loaded. If the FB voltage remains higher than a built-in threshold for longer than  $t_{D-OLP}$ , PWM output is turned off. As PWM output is turned off, the supply voltage  $V_{DD}$  begins decreasing.

When  $V_{DD}$  goes below the turn-off threshold (eg, 10.5V) the controller is totally shut down.  $V_{DD}$  is charged up to the turn-on threshold voltage of 16V through the start-up resistor until PWM output is restarted. This protection feature is activated as long as the over-loading condition persists. This prevents the power supply from overheating due to over loading conditions.

## **Noise Immunity**

Noise on the current sense or control signal may cause significant pulse width jitter, particularly in continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the SG6742, and increasing the power MOS gate resistance improves performance.



**Product Specification** 

SG6742

# **REFERENCE CIRCUIT (12V/5A)**



### BOM

Reference	Component	Reference	Component
BD1	BD 4A/600V	Q1	STP20-100CT
C1	XC 0.68µF/300V	Q2	MOS 7A/600V
C2	XC 0.1µF/300V	R1	R 100Kohm 1/2W
C3	YC 222pF/Y1	R2	R 47ohm 1/4W
C4	EC 120µF/400V	R3	R 100Kohm 1/2W
C5	CC 0.01µF/500V	R4	R 20ohm 1/8W
C6	CC 102pF/100V	R5	R 100ohm 1/8W
C7	EC 1000µF/25V	R6	R 4.7Kohm 1/8W
C8	EC 470µF/25V	R7	R 0.3ohm 2W
C9	EC 22µF/50V	R8	R 680ohm 1/8W
C10	CC 470pF/50V	R9	R 4.7Kohm 1/8W
C11	CC 222pF/50V	R10	R 150Kohm 1/8W
C12	CC 103pF/50V	R11	R 39Kohm 1/8W
D1	Zener Diode 15V 1/2W (option)	THER1	Thermistor TTC104
D2	BYV95C	T1	10mH
D3	FR103	T2	600µH(PQ2620)
D4	1N4007	U1	IC SG6742
F1	FUSE 4A/250V	U2	IC PC817
L1	Inductor (900µH)	U3	IC TL431
L2	Inductor (2µH)	VZ1	VZ 9G
L3	Inductor (900µH)		



SG6742

# PACKAGE INFORMATION 8PINS-DIP(D)





# Dimensions

Symbol	Millimeters			Inches			
	Min.	Тур.	Max.	Min.	Тур.	Max.	
A			5.334			0.210	
A1	0.381			0.015			
A2	3.175	3.302	3.429	0.125	0.130	0.135	
b		1.524			0.060		
b1		0.457			0.018		
D	9.017	9.271	10.160	0.355	0.365	0.400	
E		7.620			0.300		
E1	6.223	6.350	6.477	0.245	0.250	0.255	
е		2.540			0.100		
L	2.921	3.302	3.810	0.115	0.130	0.150	
eB	8.509	9.017	9.525	0.335	0.355	0.375	
θ°	0°	<b>7</b> °	15°	0°	7°	15°	



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# 8PINS-SOP(S)









# Dimensions

Symbol	Millimeter			Inch	Inch		
	Min.	Typ.	Max.	Min.	Тур.	Max.	
A	1.346		1.752	0.053		0.069	
A1	0.101		0.254	0.004	_	0.010	
b		0.406			0.016		
с		0.203			0.008		
D	4.648		4.978	0.183		0.196	
E	3.810		3.987	0.150		0.157	
е	1.016	1.270	1.524	0.040	0.050	0.060	
F		0.381X45°			0.015X45°		
Н	5.791		6.197	0.228		0.244	
L	0.406		1.270	0.016		0.050	
θ°	0°		8°	0°		8°	

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#### SG6742

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Demination of Terms						
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