NIPPON PRECISION CIRCUITS INC.

SM5142AP/AM

Frequency Synthesizer PLL IC

OVERVIEW

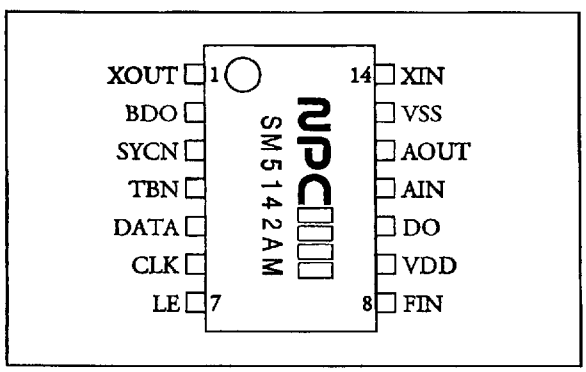
The SM5142AP/AM is a 20 MHz frequency synthesizer PLL IC, fabricated using NPC's unique Molybdenum-gate CMOS process. It is ideal for tuners that use double-conversion receivers.

FEATURES

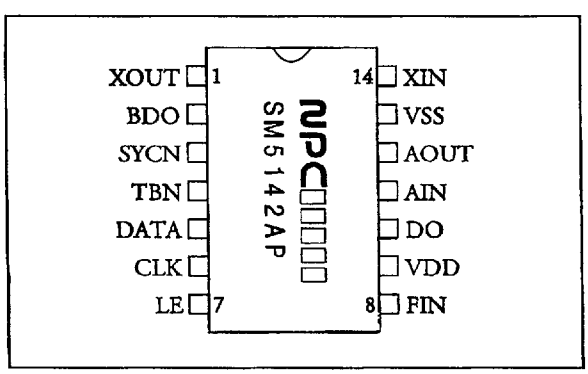
- 20 MHz direct frequency division
- 4 selectable reference frequencies (1, 5, 9 and 10 kHz)
- Built-in transistor for low-pass filter
- 60 kHz and 8 Hz outputs for external application
- Package
  - 14-pin plastic SSOP
  - 14-pin plastic DIP
- Molybdenum-gate CMOS process

PINOUTS

14-pin SSOP



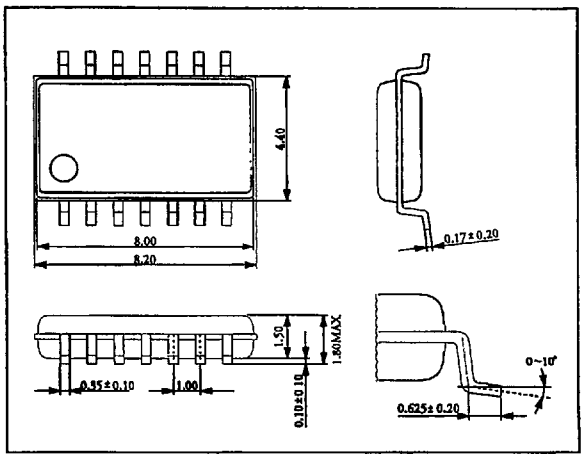
14-pin DIP



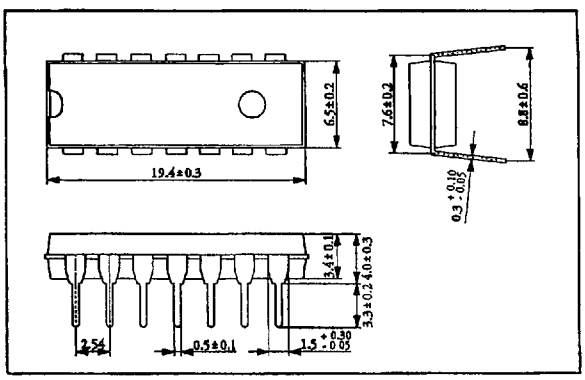
PACKAGE DIMENSIONS

Unit: mm

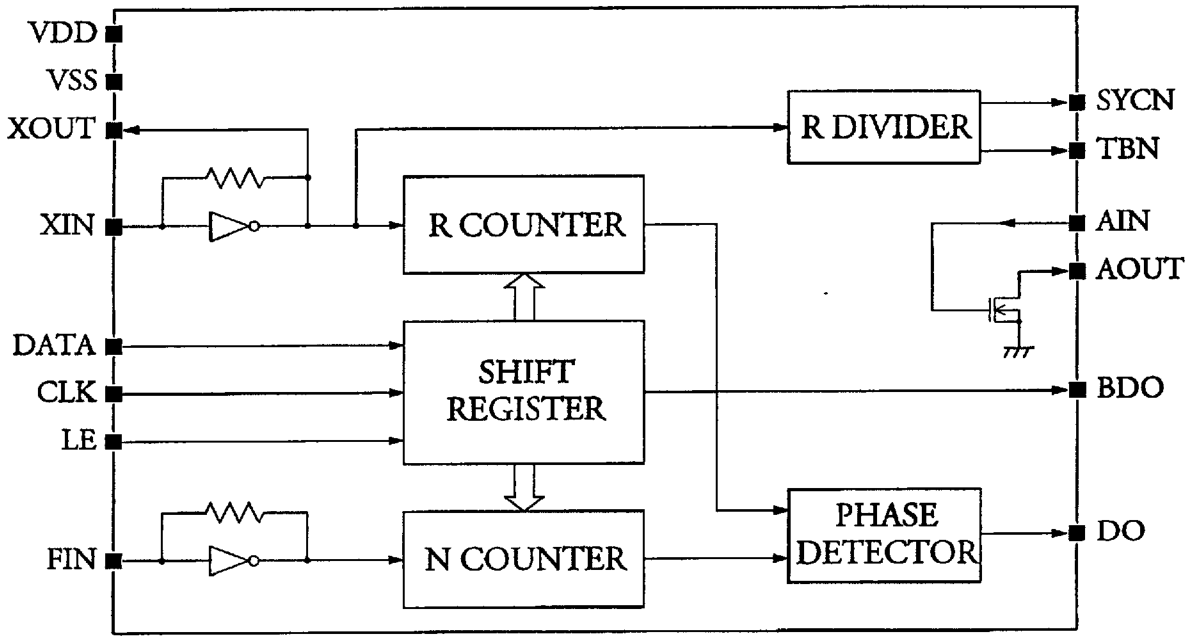
SM5142AM (14-pin SSOP)



SM5142AP (14-pin DIP)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description	
1	XOUT	O	Crystal oscillator element and capacitor connection pin. The signal from this pin can be input to a 2nd mixer stage.	
2	BDO	O	Shift register output pin	
3	SYCN	O	60 kHz controller clock output pin. N-channel open-drain output. A diode is built-in for electrostatic breakdown protection, so the voltage on this pin should not exceed the supply voltage.	
4	TBN	O	8 Hz time-base clock output pin. N-channel open-drain output. A diode is built-in for electrostatic breakdown protection, so the voltage on this pin should not exceed the supply voltage.	
5	DATA	I	Shift register data input pin	Frequency divider and mode select input pins
6	CLK	I	Clock input pin	
7	LE	I	Latch write enable signal input pin	
8	FIN	I	Programmable divider input pin. A feedback resistor is built-in, and inputs can be coupled capacitively.	
9	VDD	–	4.5 to 5.5 V supply pin	
10	DO	O	Phase comparator output pin. An active filter charge pump circuit is built-in.	
11	AIN	I	Low-pass filter amplifier input pin	
12	AOUT	O	Low-pass filter amplifier output pin. N-channel open-drain output.	
13	VSS	–	Ground pin	
14	XIN	I	Crystal oscillator element and capacitor connection pin. Feedback resistor built-in.	

SPECIFICATIONS

Absolute Maximum Ratings

$V_{SS} = 0$ V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		–0.3 to 6.5	V
Input voltage range	V_{IN}		–0.3 to V_{DD} + 0.3	V
AOUT output current range	I_{OUT}		0 to 5.0	mA
AOUT output voltage range	V_{OUT}		–0.3 to 15.0	V
Power dissipation	P_D	$T_a \leq 85$ °C	150	mW
Operating temperature range	T_{opr}		–30 to 85	°C
Storage temperature range	T_{stg}		–55 to 125	°C
Soldering temperature	T_{sld}		255	°C
Soldering time	t_{sld}		10	s

Electrical Characteristics

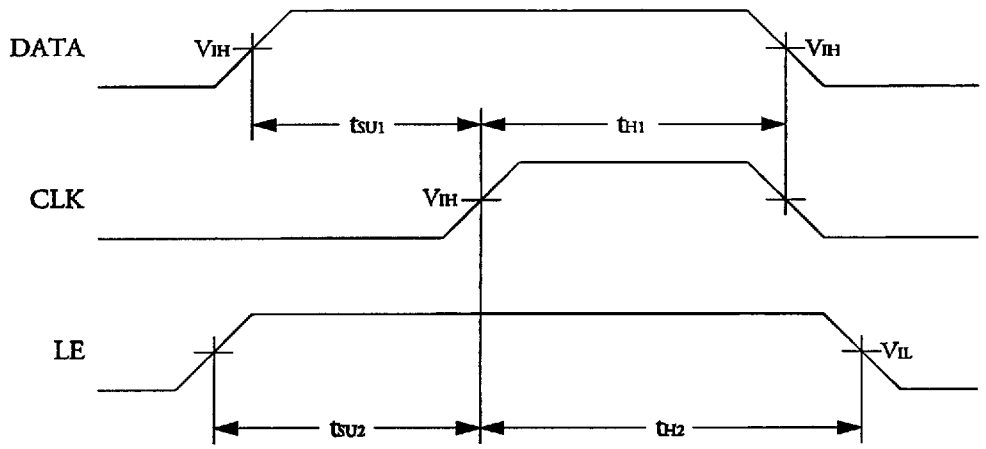
$V_{SS} = 0$ V, $T_a = -30$ to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	–	5.5	V
Current consumption[1]	I_{DD1}		–	–	12	mA
Standby mode current consumption[2]	I_{DD2}		–	2	5	mA
FIN maximum operating frequency	f_{MAX1}		20	–	–	MHz
FIN minimum operating input amplitude	$V_{IN1\ MIN}$	f_{FIN} = 20 MHz	100	–	–	mVrms
FIN minimum operating frequency	f_{MIN1}	V_{FIN} = 100 mVrms	–	–	5	MHz
XIN maximum operating frequency	f_{MAX2}	Crystal oscillator	12	–	–	MHz
FIN HIGH-level input current	I_{IH1}	$V_{IH} = V_{DD}$	–	–	40	µA
FIN LOW-level input current	I_{IL1}	$V_{IL} = V_{SS}$	–	–	40	µA
XIN HIGH-level input current	I_{IH2}	$V_{IH} = V_{DD}$	–	–	20	µA
XIN LOW-level input current	I_{IL2}	$V_{IL} = V_{SS}$	–	–	20	µA
CLK, DATA and LE HIGH-level input voltage	V_{IH}		2.0	–	V_{DD}	V
CLK, DATA and LE LOW-level input voltage	V_{IL}		0	–	0.5	V
AOUT output voltage	V_{OUT1}		–	–	13	V
Output voltage (all pins except AOUT)	V_{OUT2}		–	–	V_{DD}	V
DO HIGH-level output voltage	V_{OH1}	I_{OH} = 0.5 mA	V_{DD} – 1.0	–	–	V
DO LOW-level output voltage	V_{OL1}	I_{OL} = 0.5 mA	–	–	1.0	V
SYCN and TBN LOW-level output voltage	V_{OL2}	I_{OL} = 0.5 mA	–	–	1.0	V
BDO HIGH-level output voltage	V_{OH3}	I_{OH} = 1.0 mA	V_{DD} – 1.0	–	–	V
BDO LOW-level output voltage	V_{OL3}	I_{OL} = 1.0 mA	–	–	1.0	V
AOUT LOW-level output voltage	V_{OL4}	I_{OL} = 1.0 mA	–	–	1.0	V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
DO HIGH-level output leakage current	I_{IH}	$V_{OH} = V_{DD}$	–	–	0.1	µA
DO LOW-level output leakage current	I_{IL}	$V_{OL} = V_{SS}$	–	–	0.1	µA

1. f_{FIN} = 20 MHz (100 mVrms), 11.16 MHz crystal between XIN and XOUT, all other inputs = V_{SS}, all outputs open.
2. 11.16 MHz crystal between XIN and XOUT, all other inputs = V_{SS}, all outputs open.

Input timing characteristics



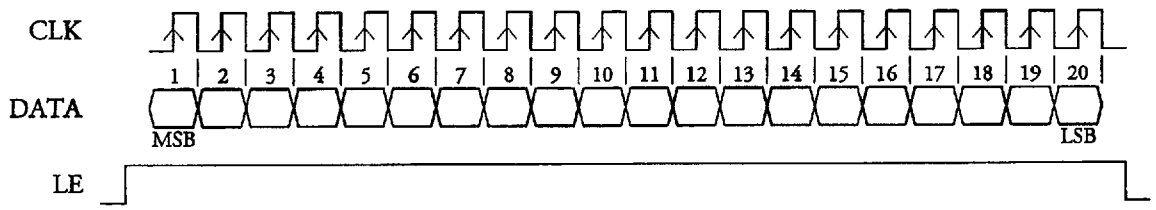
Parameter	Symbol	Rating[1]	Unit
DATA setup time	t_{SU1}	≥ 12	µs
LE setup time	t_{SU2}	≥ 12	µs
DATA hold time	t_{H1}	≥ 12	µs
LE hold time	t_{H2}	≥ 12	µs

1. 11.16 MHz crystal oscillator element. For other crystal oscillator frequencies, multiply the rating shown by ($124/f_{Xtal}$).

FUNCTIONAL DESCRIPTION

Input Data

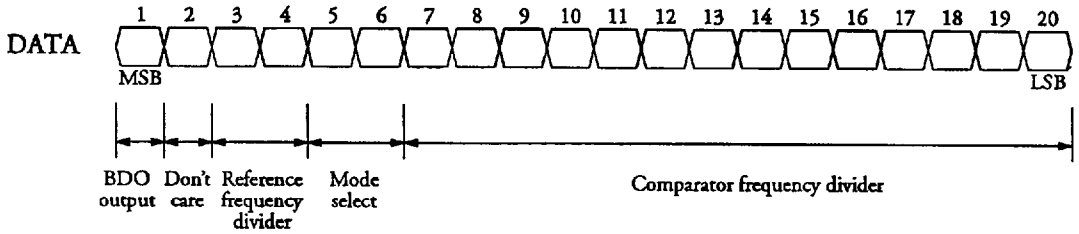
Data input timing



The 20-bit data is input on DATA with the MSB first. The data is input to the shift register on the rising edge of CLK. Accordingly, data changes should occur on the falling edge of CLK.

Data settings

The comparator frequency, reference frequency and all other parameters can be set by the 20-bit input data. The 20-bit data has the following structure.



Bit 1 sets the BDO output. BDO is HIGH when this bit is 1. BDO is LOW when this bit is 0.

Bit 2 is not used and has no meaning. It can be set to any state.

Bits 3 and 4 select the reference frequency divider as shown in the following table.

Bit 3	Bit 4	Comparator frequency[1]	Frequency divider ratio
0	0	9 kHz	1240
1	0	10 kHz	1116
0	1	1 kHz	11160
1	1	5 kHz	2232

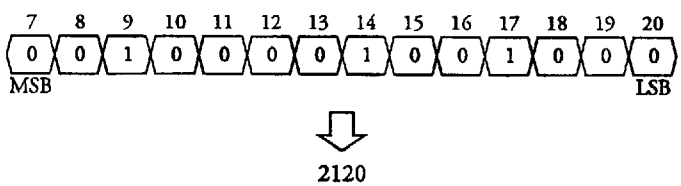
1. 11.16 MHz crystal oscillator

Bits 5 and 6 select the PLL operating mode as shown in the following table.

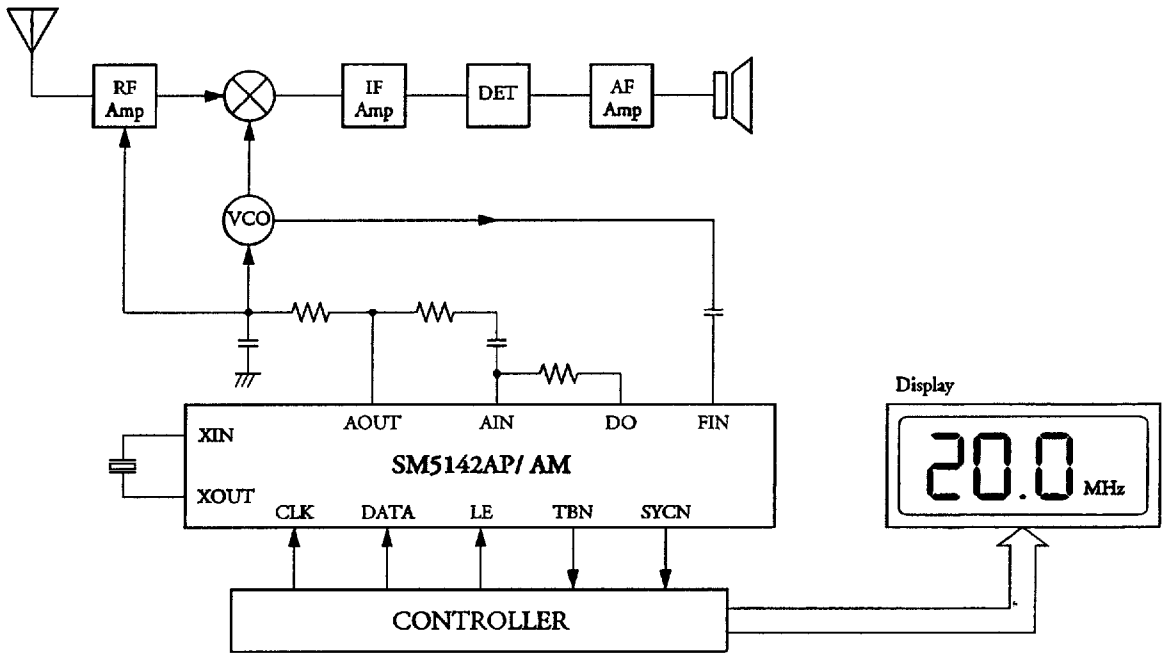
	Bit 5	Bit 6	BDO	TBN
Normal mode	0	0	Bit 1	8 Hz
Standby mode[1]	1	0	Bit 1	8 Hz
Test mode	0	1	This mode is for IC testing only and should not be used.	
	1	1		

1. The feedback resistor is open circuit, so FIN goes HIGH and the N counter operation stops.

Bits 7 to 20 set the comparator frequency divider. Bit 7 is the MSB, and bit 20 is the LSB. An example is shown below.



TYPICAL APPLICATION



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