NIPPON PRECISION CIRCUITS INC.

SM8578BV

Real-time Clock IC

OVERVIEW

The SM8578BV is a CMOS serial interface, real-time clock IC that uses a 32.768 kHz crystal oscillator for its reference timing.

It comprises second-counter to year-counter clock and calendar circuits that feature automatic leap-year adjustment, alarm and timer interrupt functions, as well as oscillator stop, timer reloading, and other detection functions. Data is transferred to and from an external controller using a 3-wire serial interface. It is available in compact 8-pin VSOP packages, making it ideal for use in all types of portable, hand-held equipment.

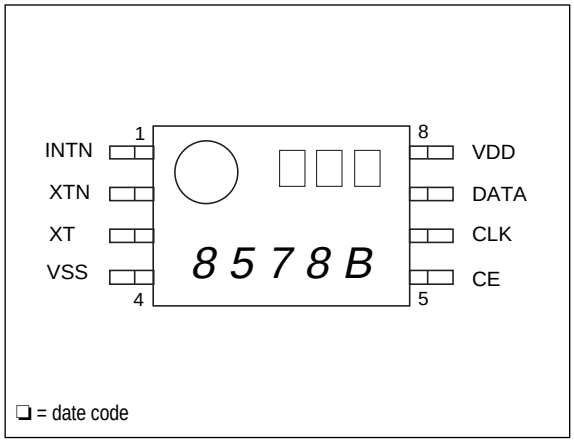
FEATURES

- 3-wire serial interface control
- Day (day of the month), weekday (Sunday to Saturday), hour and minute alarm interrupt function
- 1/4096 seconds to 255 minutes presettable interval timer interrupt function
- Oscillator stop and timer reload detect functions
- Automatic leap-year adjustment function (Western and Japanese calendars)
- 1.6 to 5.5 V supply voltage range
- 0.5 µA (typ. at 3 V) current consumption
- C_D oscillator capacitor built-in
- Compact 8-pin VSOP package

PINOUT

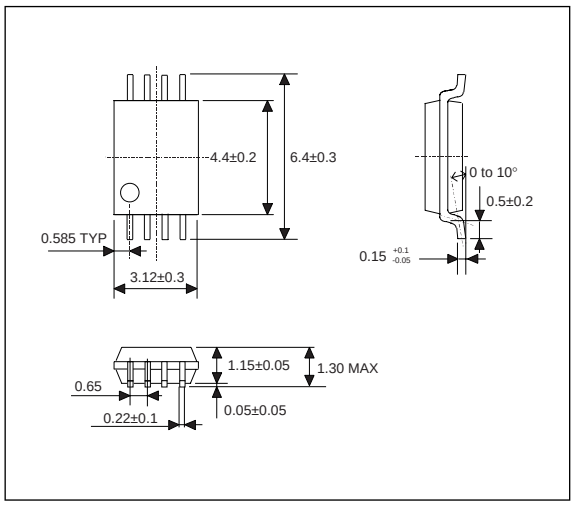
8-pin VSOP

Top view

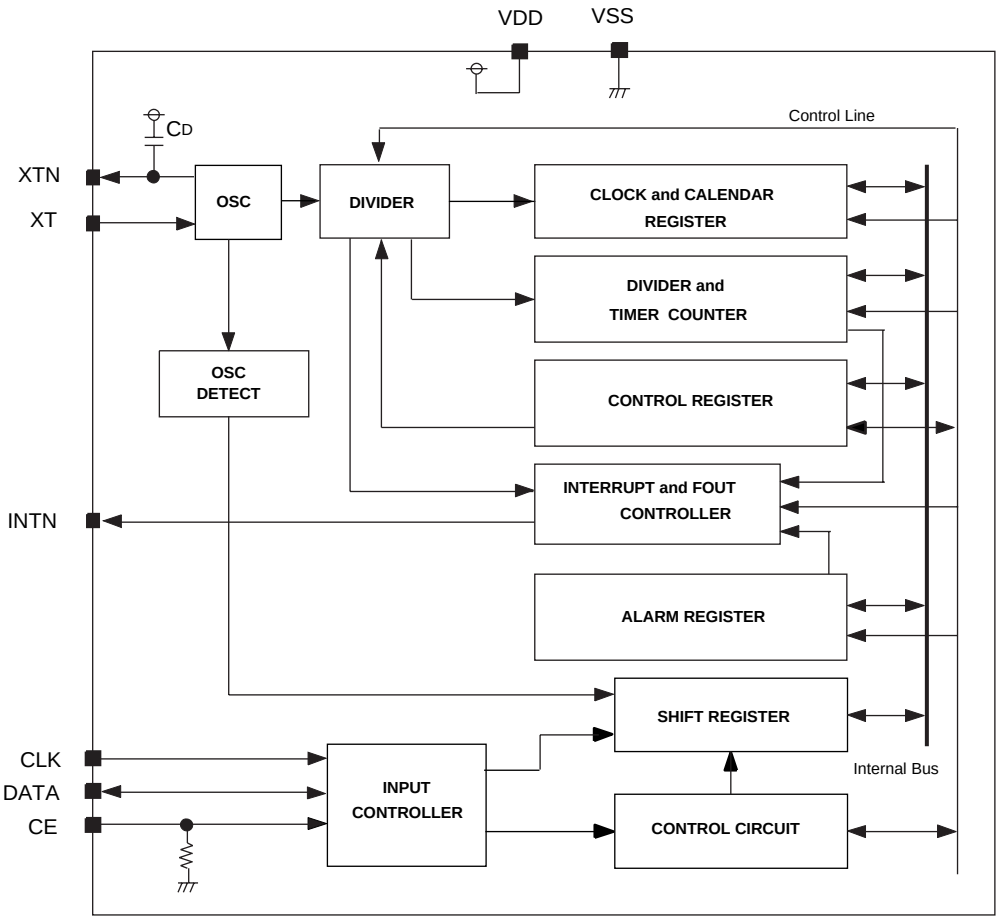


PACKAGE DIMENSIONS

Unit: mm



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Function
1	INTN	O	Timer/alarm interrupt output and the setting frequency output,corresponding to the active internal mode. N-channel open-drain output pin
2	XTN	O	Oscillator output. Oscillator capacitor C_D built-in
3	XT	I	Oscillator input
4	VSS	–	Negative supply pin
5	CE	I	Chip enable. Chip is selected when HIGH. Pull-down resistor built-in
6	CLK	I	Serial data clock. In write mode, data is input on DATA on the rising edge of CLK. In read mode, data is output on DATA on the rising edge of CLK.
7	DATA	I/O	Serial data input/output. When CE goes HIGH, initial 4-bit input data determines the device mode. Subsequent data is transferred in write or read mode, as selected by the device mode.
8	VDD	–	Positive supply voltage. A 0.1 µF pass capacitor should be connected between VDD and VSS.

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		–0.3 to 7.0	V
Input voltage range	V_{IN}	All inputs	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage range	V_{OUT1}	INTN	V_{SS} – 0.3 to 8.0	V
	V_{OUT2}	DATA	V_{SS} – 0.3 to V_{DD} + 0.3	V
Power dissipation	P_D		150	mW
Storage temperature range	T_{STG}		–55 to 125	°C
Soldering temperature	T_{SLD}		255	°C
Soldering time	t_{SLD}		10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		1.6 to 5.5	V
Operating temperature range	T_{opr}		–40 to 85	°C

DC Electrical Characteristics

V_{SS} = 0 V, V_{DD} = 1.6 to 5.5V , C_G = 10 pF, T_a = –40 to 85 °C unless otherwise noted

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Current consumption	I_{DD1}	V_{DD} = 5.0 V	CE = V_{SS} DATA, INTN = V_{DD}	–	1.0	2.0	µA
	I_{DD2}	V_{DD} = 3.0 V		–	0.5	1.0	µA
HIGH-level input voltage	V_{IH}	CE, CLK, DATA		0.8V_{DD}	–	V_{DD}	V
LOW-level input voltage	V_{IL}	CE, CLK, DATA		0	–	0.2V_{DD}	V
Input leakage current	I_{LEAK}	CE, CLK: V_{IN} = V_{DD} or V_{SS}		-0.5	–	0.5	µA
Input resistance	R_{DWN1}	V_{DD} = 5.0 V	CE: V_{IN} = V_{DD}	75	150	300	kΩ
	R_{DWN2}	V_{DD} = 3.0 V		150	300	600	kΩ
HIGH-level output voltage	V_{OH1}	V_{DD} = 5.0 V	DATA: I_{OH} = –1 mA	4.5	–	5.0	V
	V_{OH2}	V_{DD} = 3.0 V		2.0	–	3.0	V
LOW-level output voltage	V_{OL1}	V_{DD} = 5.0 V	DATA: I_{OL} = 1 mA	–	–	V_{SS} + 0.5	V
	V_{OL2}	V_{DD} = 3.0 V		–	–	V_{SS} + 0.8	V
	V_{OL3}	V_{DD} = 5.0 V	INTN: I_{OL} = 1 mA	–	–	V_{SS} + 0.25	V
	V_{OL4}	V_{DD} = 3.0 V		–	–	V_{SS} + 0.4	V
Output leakage current	I_{OZ}	DATA, INTN: V_{OUT} = V_{DD} or V_{SS}		–0.5	–	0.5	µA
Oscillator stop detection time	t_{OSC}			10	–	–	ms

Oscillator Characteristics

T_a = 25 °C, C_G = 10 pF, Seiko Epson C-002SH crystal (C_I = 30 kΩ, C_L = 6 pF) unless otherwise noted

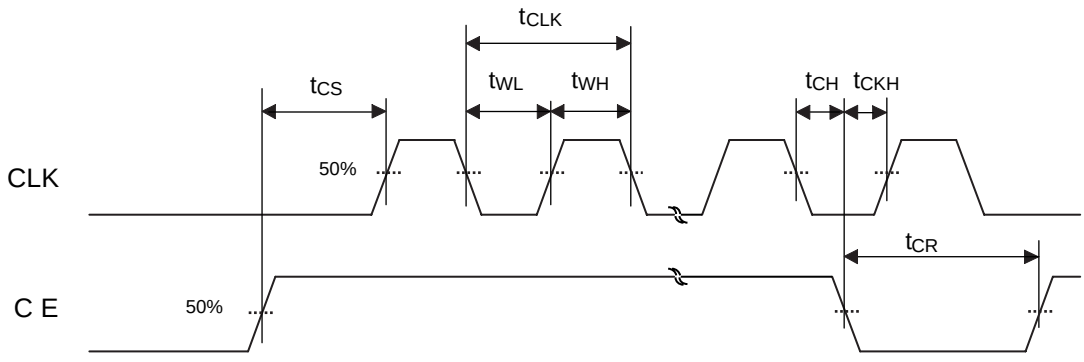
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Oscillator start time	t_{STA}	V_{DD} = 1.6 V	–	–	5.0	s
Oscillator stop voltage	V_{STO}		–	–	1.5	V
Frequency voltage characteristic	f/V	V_{DD} = 1.6 to 5.5 V	–2	–	+2	ppm/V
Frequency accuracy	ε_{IC}	V_{DD} = 5.0 V	–10	–	+10	ppm
Output capacitance	C_D	V_{DD} = 5.0 V	–	15	–	pF

AC Characteristics

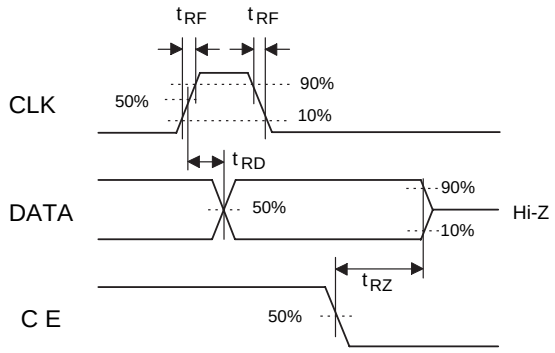
V_{SS} = 0 V, C_L = 50 pF, T_a = –40 to 85 °C unless otherwise noted

Parameter	Symbol	V_{DD} = 5 V ± 10%			V_{DD} = 3.0 V ± 10%			Unit
		min	typ	max	min	typ	max	
CLK clock period	t_{CLK}	600	–	–	1200	–	–	ns
CLK HIGH-level pulsewidth	t_{WH}	300	–	–	600	–	–	ns
CLK LOW-level pulsewidth	t_{WL}	300	–	–	600	–	–	ns
CE setup time	t_{CS}	150	–	–	300	–	–	ns
CE hold time	t_{CH}	200	–	–	400	–	–	ns
CE recovery time	t_{CR}	300	–	–	600	–	–	ns
CLK hold time	t_{CKH}	50	–	–	100	–	–	ns
Write data setup time	t_{DS}	50	–	–	100	–	–	ns
Write data hold time	t_{DH}	50	–	–	100	–	–	ns
Read data output delay time[1]	t_{RD}	–	–	200	–	–	400	ns
Output disable delay time[2]	t_{RZ}	–	–	100	–	–	200	ns
Input rise and fall time	t_{RF}	–	–	20	–	–	40	ns

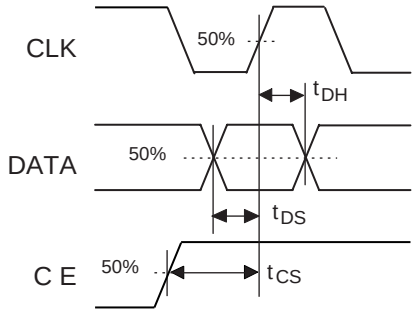
1. C_L=50pF
2. C_L=50pF, RL=10kΩ



Data read



Data write



FUNCTIONAL DESCRIPTION

Registers

Address	Register[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Readable	Writable
0	Second	FOS	40	20	10	8	4	2	1	All bits	All bits
1	Minute	fr	40	20	10	8	4	2	1	All bits	All bits (excl. bit 7)
2	Hour	fr	×	20	10	8	4	2	1	All bits	All bits (excl. bit 7)
3	Weekday	fr	6	5	4	3	2	1	0	All bits	All bits (excl. bit 7)
4	Day	fr	×	20	10	8	4	2	1	All bits	All bits (excl. bit 7)
5	Month	fr	×	×	10	8	4	2	1	All bits	All bits (excl. bit 7)
6	Year	80	40	20	10	8	4	2	1	All bits	All bits
7	Minute alarm	AE	40	20	10	8	4	2	1	All bits	All bits
8	Hour alarm	AE	×	20	10	8	4	2	1	All bits	All bits
9	Weekday alarm	AE	6	5	4	3	2	1	0	All bits	All bits
A	Day alarm	AE	×	20	10	8	4	2	1	All bits	All bits
B	Output frequency	FE	×	FD4	FD3	×	FD2	FD1	FD0	All bits	All bits
C	Cycle frequency	TE	×	TD1	TD0	×	×	×	×	All bits	All bits
D	Interval counter[2]	128	64	32	16	8	4	2	1	All bits	All bits
E	Control 1	×	×	×	TI/TP	AF	TF	AIE	TIE	All bits	All bits[3]
F	Control 2	×	TEST	×	RESET	HOLD	×	×	×	All bits	All bits

1. When power is applied, all register values are undefined. Accordingly, all registers must be set by initial input data.
2. When address D is read, the previous preset data value is output.
3. Bits AF and TF can only be set to 0 by writing to address E (i.e. reset only).

× = don't care. All don't care bits can be used as general-purpose RAM.

Clock and calendar registers (address 0 to 6)

Data in these registers is interpreted in BCD format. For example, if the second register contains 0101 1001, then the contents of the register is interpreted as the value 59 seconds. Hour register contents are values expressed in 24-hour mode.

Leap-year detection is made by dividing the year register contents (2 BCD digits) by 4. If the remainder is 0, corresponding to a leap year, the values in the weekday and day registers are adjusted automatically. Note that the year following year 99 is year 00.

The weekday register contains values representing the day of the week as shown in the following table. Note that software measures should be taken to ensure that only one bit is set to 1.

Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Weekday
0	0	0	0	0	0	1	Sunday
0	0	0	0	0	1	0	Monday
0	0	0	0	1	0	0	Tuesday
0	0	0	1	0	0	0	Wednesday
0	0	1	0	0	0	0	Thursday
0	1	0	0	0	0	0	Friday
1	0	0	0	0	0	0	Saturday

The FOS bit is the oscillator stop flag. It indicates that the oscillator has stopped due to output voltage reduction during operation. It is set to 1 when the oscillator stops, and remains 1 until reset by writing 0 to FOS. It is not affected by the function of other bits.

The fr bits are the read flags. They indicate that the contents of the corresponding register generated an overflow bit while a read cycle was in progress (CE = HIGH). If any fr bit encountered is set to 1, then all clock timer registers must be read again. The fr bits are cleared to 0 when CE goes LOW.

The seconds and year registers do not have fr bits to indicate overflow. Instead, the value of the two most significant bits (bits 5 and 6 in the seconds register,

and bits 6 and 7 in the year register) are set to 1 (for example, Year: 0010 1001 → 1110 1001). The illegal value that results can then be used to indicate overflow, serving the same function as an fr flag. The correct value of the register is restored when CE goes LOW.

Alarm registers (address 7 to A)

An alarm can be set for day, weekday, hour and minute. The weekday alarm register settings correspond to the weekdays as shown in the following table. The alarm setting can also be set for more than one weekday by setting more than one bit to 1. Note that if a weekday alarm is set, then the hour alarm, minute alarm or both should be set; the alarm may not be output correctly if only a weekday alarm is set.

Address 9	Weekday
Bit 0 = 1	Sunday
Bit 1 = 1	Monday
Bit 2 = 1	Tuesday
Bit 3 = 1	Wednesday
Bit 4 = 1	Thursday
Bit 5 = 1	Friday
Bit 6 = 1	Saturday

Bit 7 of each of the alarm registers is an alarm enable bit (AE). When AE is 0, the register contents are compared with the corresponding clock timer register contents to determine when the alarm condition has occurred. When AE is 1, all data bits in the register are considered as don't care bits. In this case, the data is ignored and the alarm condition is always active for all valid values of that register. Thus AE can be used to set regular alarms, such as hourly or daily alarms regardless of the current hour or day.

When the alarm interrupt enable bit (AIE) in register address E is 0, alarm output on INTN is disabled. TIE and FE must be set to 0, and AIE set to 1 to enable the alarm interrupt function.

Timer registers (address C to E)

The timer registers control an 8-bit presettable down-counter. The timer counter in register address D counts down using the source clock frequency assigned by bits TD0 and TD1 in register address C, as shown in the following table. When the counter becomes zero, generating a timer interrupt event, INTN goes LOW. The counter is then reloaded with the preset count and count down starts again. Thus the timer counter is used as an interval timer.

TD0	TD1	Source clock
0	0	4096 Hz
0	1	64 Hz
1	0	1 Hz (1 s)
1	1	1/60 Hz (1 min)

When the timer interrupt enable bit (TIE) in register address E is 0, timer output on INTN is disabled. AIE and FE must be set to 0, and TIE set to 1 to enable the timer interrupt function. TI/TP controls the timer output mode.

The presettable down-counter is loaded with new data whenever a write to register address D occurs. Note that when the timer interrupt is disabled (TIE = 0), the data in register address D is stored and thus register address D can be used as general-purpose RAM, just as described for the don't care bits in the register table.

When the timer enable bit (TE) is 0, the timer counter data is loaded into the counter. The count is then started by setting TE to 1.

Output frequency register (address B)

The output frequency on INTN is determined by the frequency divider ratio set by FD0 to FD2 and by the source clock frequency set by FD3 and FD4, as shown in the following tables. AIE and TIE should be 0 when setting the output frequency. When the frequency output enable bit (FE) is 0, INTN is in a high-impedance state.

FD4	FD3	Source clock
0	0	32768 Hz
0	1	1024 Hz
1	0	32 Hz
1	1	1 Hz

FD2	FD1	FD0	Divider ratio
0	0	0	1/1
0	0	1	1/2
0	1	0	1/3
0	1	1	1/6
1	0	0	1/5
1	0	1	1/10
1	1	0	1/15
1	1	1	1/30

Control register 1 (address E)

This register comprises the alarm interrupt and timer interrupt control flags.

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E	×	×	×	TI/TP	AF	TF	AIE	TIE

The TI/TP bit is an interrupt signal output mode select (interrupt/periodic) bit. In timer mode, FE and AIE should be set to 0.

When TI/TP is 0, level interrupt mode is selected. In this mode (TI/TP = 0 and TIE = 1), INTN goes LOW and TF is set to 1 when a timer interrupt event occurs. INTN remains LOW until 0 is written to TF.

When TI/TP is 1, repetitive interrupt (interval) mode is selected. In this mode (TI/TP = 1 and TIE = 1), INTN goes LOW and TF is set to 1 when a timer interrupt event occurs. INTN then goes into a high-impedance state after a preset auto-return time set by the source clock. TF remains 1 until 0 is written to TF.

The AF and TF bits are the alarm flag and timer flag, respectively. AF is set to 1 when an alarm event occurs, and TF is set to 1 when the timer down-counter drops to zero. When set they remain 1 until 0 is written to the respective bit. Neither bit can be written to with 1 data.

The AIE and TIE bits are the alarm interrupt enable and timer interrupt enable bits, respectively. When enabled and a corresponding alarm or timer interrupt event occurs, INTN output becomes active. Alarm and timer interrupts are enabled by writing 1 to the corresponding interrupt enable bit. Note that both interrupt enable bits should not be simultaneously set to 1.

Control register 2 (address F)

This register comprises the frequency divider control bits for the timers.

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F	×	TEST	×	RESET	HOLD	×	×	×

The TEST bit is an NPC factory test bit. It should be set to 0 when power is applied and when writing to register address F.

The RESET bit is the counter reset bit. When RESET is 1, the 1 Hz to 2 kHz frequency divider counters are reset and clock functions are reset. RESET is cleared by either writing 0 or automatically when CE goes LOW. It is not affected by the settings of any other bits.

The HOLD bit is the clock function stop bit. When HOLD is 1, the seconds register digit is not incremented. If, however, an increment event would have occurred, the digit is incremented when HOLD is set to 0. Accordingly, HOLD should be set to 1 for periods of less than one second to maintain correct timing.

Interrupt Operation

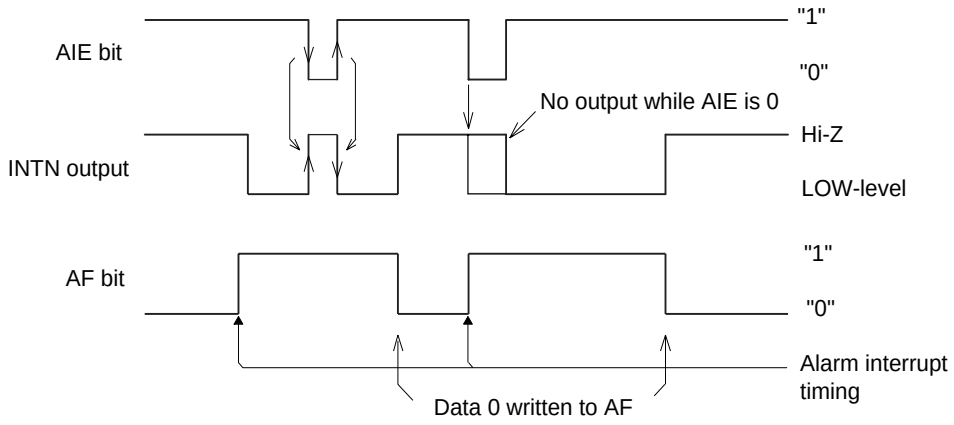
Interrrupt output

The INTN interrrupt output mode is determined by the timer interrupt bit (TIE), alarm interrupt bit (AIE), and frequency enable bit (FE), as shown in the following table. Note that only one bit can be set to 1.

TIE	AIE	FE	MODE
1	0	0	Timer interrupt output
0	1	0	Alarm interrupt output
0	0	1	Frequency output
0	0	0	Output disabled

Alarm interrupt

When AIE is 1 and an alarm event occurs, INTN output goes LOW. If AIE is 0, however, INTN is in a high-impedance state. The alarm interrupt is output when a carry from the seconds register to the minute register occurs.

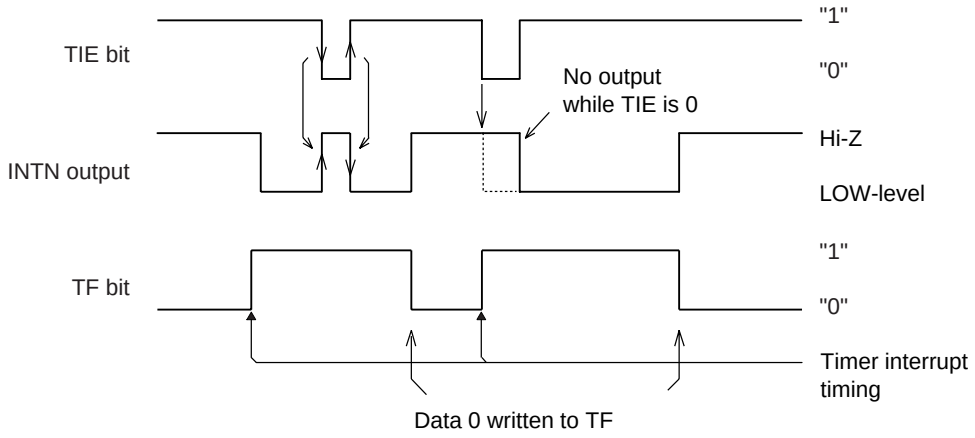


Timer interrupt

The timer interrupt mode (level interrupt or repetitive interrupt) is selected by the setting of TI/TP. In timer mode, AIE and FE should be set to 0.

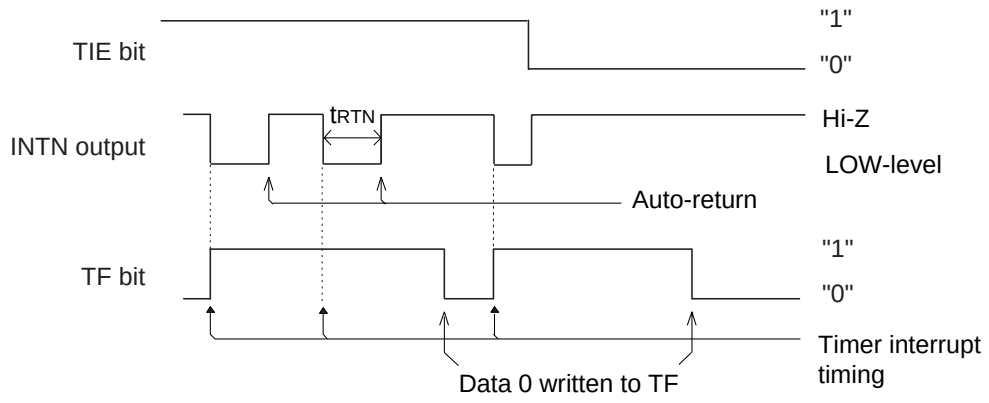
Level interrupt mode (TI/TP = 0)

When TIE is 1 and a timer interrupt event occurs, INTN goes LOW and TF is set to 1. INTN goes into a high-impedance state when 0 is written to TF. When TIE is 0, however, INTN is in a high-impedance state.



Repetitive interrupt mode (TI/TP = 1)

When TIE is 1 and a timer interrupt event occurs, INTN goes LOW and TF is set to 1. INTN then goes into a high-impedance state after the auto-return time. TF remains 1 until 0 is written to TF. When TIE is 0, however, INTN is in a high-impedance state.



The auto-return time (t_{RTN}) is determined by the source clock frequency set by register address C as shown in the following table.

Source clock	Auto-return time (t_{RTN})
4096 Hz	0.122 ms
64 Hz	7.81 ms
1 Hz	0.5 s
1/60 Hz	0.122 ms

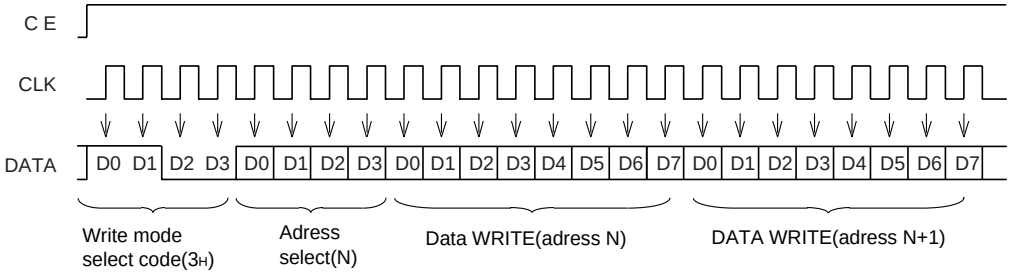
Addressing

When CE goes HIGH for either a read or write cycle, the initial input data comprises 4 mode select bits followed by 4 address bits. Subsequent data is read/written (depending on the mode selected) in 8-bit units from/to the address selected. All input/output data is in LSB-first format.

Note that if CE goes LOW before a complete 8-bit unit of input data, the entire 8 bits of data are ignored.

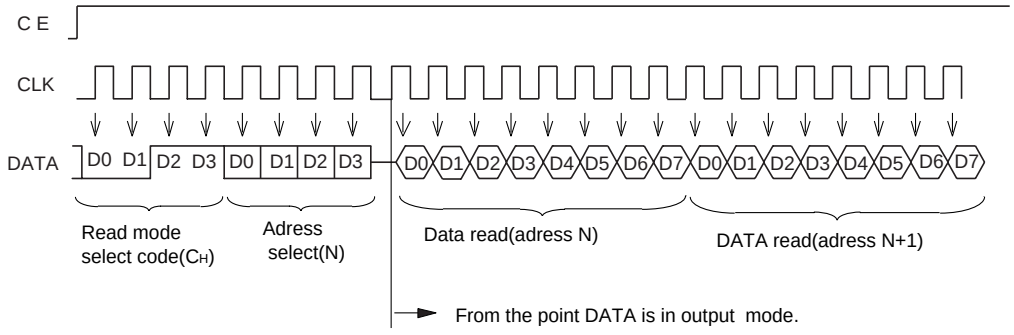
Write cycle

When the first 4 bits of input data after CE goes HIGH is 3_H, write mode is selected. The subsequent 4 bits select the address to be written. The next 8 bits of data are then written to the selected address, and then the address is automatically incremented. Subsequent input data is written to addresses in increasing order. Note that the address following address F_H is address 0_H.



Read cycle

When the first 4 bits of input data after CE goes HIGH is C_H, read mode is selected. The subsequent 4 bits select the address to be read. 8-bit is then read from the selected address, and then the address is automatically incremented. Subsequent input data is read from addresses in increasing order. Note that the address following address F_H is address 0_H.



Note that if a mode select code other than 3_H or C_H is input, all following data is ignored until a valid mode select code occurs.

Setting the Alarm

Alarms can be set for day, weekday, hour and minute. An alarm can also be set for more than one weekday. Note that it is recommended that AF and AIE be set to 0 to avoid accidental hardware interrupts while setting the alarm.

After the alarm data is entered, initialization occurs when AF is again set to 0. The alarm interrupt is enabled by writing 1 to AIE.

If the hardware interrupt is not used, then AIE should be set to 0. In this case, an alarm can still be controlled by software monitoring of AF using read cycles.

Example 1

To set an alarm for 6pm of the following day:

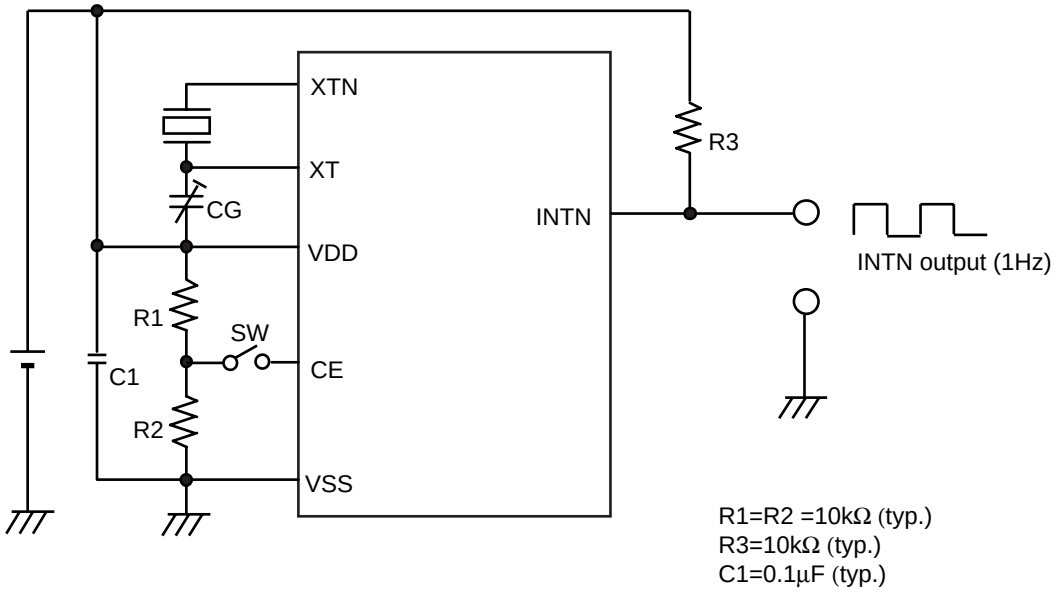
- Set bits AIE and AF to 0.
- Set the day register AE bit to 1 (don't care).
- Acquire the current weekday setting from register address 3, rotate result left by 1 bit, and write to weekday alarm register (while monitoring the fr bit).
- Write 18_H to the hour alarm register.
- Write 00_H to the minute alarm register.
- Set AF to 0 and AIE to 1.

Example 2

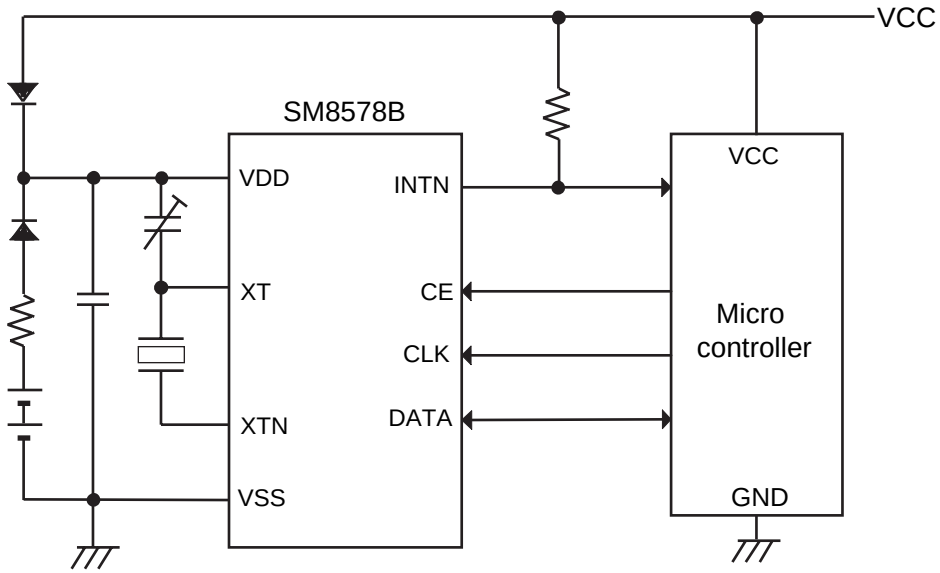
To set an alarm for 6am for Monday to Friday:

- Set bits AIE and AF to 0.
- Set the day register AE bit to 1 (don't care).
- Write $3E_H$ to the weekday alarm register.
- Write 06_H to the hour alarm register.
- Write 00_H to the minute alarm register.
- Set AF to 0 and AIE to 1.

Monitoring Oscillator Frequency



APPLICATION CIRCUIT



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NC9619CE 1997.08