

- Processed to MIL-PRF-38535
- Fast Instruction Cycle Time of 30 ns and 40 ns
- Source-Code Compatible With all 'C1x and 'C2x Devices
- RAM-Based Operation
 - 9K-Word × 16-Bit Dual-Access On-Chip Program/Data RAM
 - 1056-Word × 16-Bit Dual-Access On-Chip Data RAM
- 2K-Word × 16-Bit On-Chip Boot ROM
- 224K-Word × 16-Bit Maximum Addressable External Memory Space (64K-Word Program, 64K-Word Data, 64K-Word I/O, and 32K-Word Global)
- 32-Bit Arithmetic Logic Unit (ALU)
 - 32-Bit Accumulator (ACC)
 - 32-Bit Accumulator Buffer (ACCB)
- 16-Bit Parallel Logic Unit (PLU)
- 16 × 16-Bit Multiplier, 32-Bit Product
- Eleven Context Switch Registers
- Two Buffers for Circular Addressing
- Full-Duplex Synchronous Serial Port
- Time-Division Multiplexed (TDM) Serial Port
- Timer With Control and Counter Registers
- Sixteen Software-Programmable Wait-State Generators
- Divide-By-1 Clock Option
- IEEE Standard 1149.1† (JTAG) Test-Access Port
- Operations are Fully Static
- Fabricated Using the Texas Instruments (TI) Enhanced Performance Implanted CMOS (EPIC™) 0.64-μm Technology
- Military Operating Temperature Range
–55°C to 125°C

description

The SMJ320C50KGD digital signal processor (DSP) is a high-performance, 16-bit, fixed-point processor manufactured in 0.64-μm double-level metal CMOS technology.

The SMJ320C50 KGD employs the hot-chuck-probe process. This process uses standard probed product that is tested again, this time at full data sheet specifications, in wafer form at speed and elevated temperature (125°C). Each individual die is then sawed, inspected, and packaged for shipment.

A number of enhancements to the basic 'C2x architecture give the 'C50 a minimum 2x performance over the previous generation. A four-deep instruction pipeline, which incorporates delayed branching, delayed call to a subroutine, and delayed return from a subroutine, allows the 'C50 to perform instructions in fewer cycles. The addition of a PLU gives the 'C50 a method of manipulating bits in data memory without using the ACC and the ALU. The 'C50 has additional shifting and scaling capabilities for proper alignment of multiplicands or for storage of values to data memory.

With the addition of the IDLE2 instruction, the 'C50 achieves low-power consumption. IDLE2 removes the functional clock from the internal hardware of the 'C50 that puts it into a total-sleep mode using only 5 μA. A low-logic level on an external interrupt with a chip duration of at least five clock cycles ends the IDLE2 mode.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† IEEE Standard 1149.1–1990, IEEE Standard Test-Access Port and Boundary-Scan Architecture
EPIC is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SMJ320C50KGD
DIGITAL SIGNAL PROCESSOR
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description (continued)

SMJ MIL-TEMP PRODUCT FLOW	
Multiprobe	25°C or hot chuck probe @ 125°C
Test conditions	Per military data sheet
DC test	Hot chuck probe @ 125°C
AC test	Hot chuck probe @ 125°C @ Speed
Visual	100x
Warranty	Data sheet upon shipment, 1 year
Certificate of Compliance	Yes
Change of notification	Yes

For electrical and timing specifications, see the *SMJ320C50/SMQ320C50 Digital Signal Processors* data sheet (literature number SGUS020).

SPECIFIC DIE-RELATED INFORMATION	
Die Size (approximate)	358 mils × 338 mils
Die Thickness	11 mils ± 1 mil
Backside Surface Finish	SIO2
Die Backside Potential	Floating
Max Allowable Die Junction Operating Temperature	125°C
Glassivation Material and Thickness	3KAOX/9KACN
Recommended Packing	GEL PACK
Die Attach Information	SILVER GLASS
Suggested Bond Wire Size	1.25 AL
Suggested Bonding Method	WEDGE
ESD Sensitivity	Class II
Max Allowable Process Temperature for Die Attach	450°C



SMJ320C50 Pad Information†

	PAD	XCENTER	YCENTER	PAD NAME		PAD	XCENTER	YCENTER	PAD NAME
TOP	1	4626.18	8373.066	IAQ	BOTTOM	41	83.85	1537.224	CLKR
	2	4465.266	8373.066	TRST		42	83.85	1164.852	VDD5
	3	4245.852	8373.066	VSS1		43	83.85	1047.852	VDD6
	4	4128.852	8373.066	VSS2		44	1303.38	83.85	VSS7
	5	3955.38	8373.066	MP/MC		45	1420.38	83.85	VSS8
	6	3579.108	8373.066	D15		46	1836.276	83.85	A0
	7	3329.508	8373.066	D14		47	2074.566	83.85	A1
	8	3038.334	8373.066	D13		48	2277.366	83.85	A2
	9	2827.734	8373.066	D12		49	2515.656	83.85	A3
	10	2613.234	8373.066	D11		50	2706.756	83.85	A4
	11	2398.734	8373.066	D10		51	2945.046	83.85	A5
	12	2089.932	8373.066	D9		52	3136.146	83.85	A6
	LEFT	13	1830.036	8373.066		D8	53	3374.436	83.85
14		1467.336	8373.066	VDD1	54	3565.536	83.85	A8	
15		1350.336	8373.066	VDD2	55	3803.826	83.85	A9	
16		83.85	7404.15	VSS3	56	3952.026	83.85	VDD7	
17		83.85	7287.15	VSS4	57	4069.026	83.85	VDD8	
18		83.85	6803.55	D7	58	4235.556	83.85	TDI	
19		83.85	6592.95	D6	59	4602.234	83.85	VSS9	
20		83.85	6336.876	D5	60	4719.234	83.85	VSS10	
21		83.85	6141.876	D4	61	4884.906	83.85	CLKMD1	
22		83.85	5946.876	D3	62	5093.478	83.85	A10	
23		83.85	5751.876	D2	63	5331.768	83.85	A11	
24		83.85	5472.402	D1	64	5648.76	83.85	A12	
25		83.85	5277.402	D0	65	5887.05	83.85	A13	
26		83.85	5034.588	TMS	66	6089.85	83.85	A14	
27		83.85	4756.674	VDD3	67	6328.14	83.85	A15	
28		83.85	4639.674	VDD4	68	7100.34	83.85	VDD9	
29		83.85	4274.946	TCK	69	7217.34	83.85	VDD10	
30		83.85	4120.818	MTESTEN	70	7487.532	83.85	RD	
31	83.85	3979.404	VSS5	71	7961.148	83.85	WE		
32	83.85	3862.404	VSS6	72	8896.134	1078.35	VSS11		
33	83.85	3493.932	INT1	73	8896.134	1195.35	VSS12		
34	83.85	3275.688	INT2	74	8896.134	1640.106	DS		
35	83.85	3057.444	INT3	75	8896.134	1930.11	IS		
36	83.85	2766.27	INT4	76	8896.134	2179.866	PS		
37	83.85	2548.026	NMI	77	8896.134	2489.994	R/W		
38	83.85	2329.782	DR	78	8896.134	2738.034	STRB		
39	83.85	2111.538	TDR	79	8896.134	2908.074	BR		
40	83.85	1755.468	FSR	80	8896.134	3133.962	NC		

† Measured from corner of active area.

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SMJ320C50 Pad Information† (Continued)

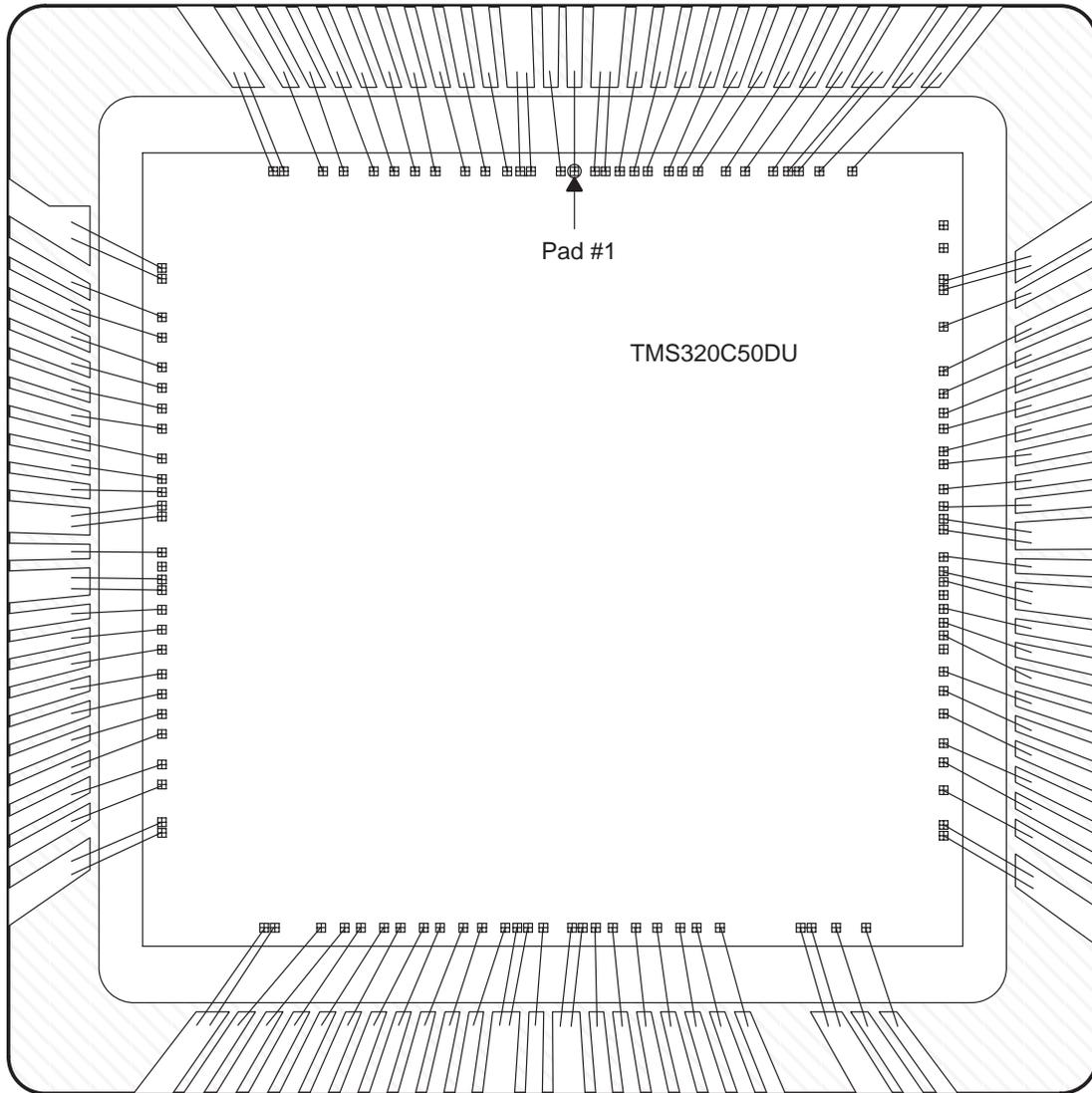
PAD	XCENTER	YCENTER	PAD NAME
81	8896.134	3281.148	CLKIN2
82	8896.134	3415.62	X2/CLKIN
83	8896.134	3568.11	X1
84	8896.134	3715.14	NC
85	8896.134	3856.554	VDD11
86	8896.134	3973.554	VDD12
87	8896.134	4122.846	TDO
88	8896.134	4398.81	VSS13
89	8896.134	4515.81	VSS14
90	8896.134	4650.282	CLKMD2
91	8896.134	4827.186	FSX
92	8896.134	5075.694	TFSX/TFRM
93	8896.134	5266.95	DX
94	8896.134	5520.294	TDX
95	8896.134	5711.55	HOLD \bar{A}
96	8896.134	5902.806	XF
97	8896.134	6214.65	CLKOUT1
98	8896.134	6542.406	IACK
99	8896.134	7002.606	VDD13
100	8896.134	7119.606	VDD14
101	8896.134	7552.818	VDD31
102	8896.134	7669.818	VDD32
TOP-R 103	7966.296	8373.066	EMU0
104	7615.452	8373.066	EMU1/OFF
105	7393.152	8373.066	VSS15
106	7276.152	8373.066	VSS16
107	6862.596	8373.066	TOUT
108	6656.364	8373.066	TCLKX
109	6454.032	8373.066	CLKX
110	6174.324	8373.066	TFSR/TADD
111	6020.352	8373.066	TCLKR
112	5860.608	8373.066	RS
113	5700.864	8373.066	READY
114	5541.12	8373.066	HOLD
115	5206.344	8373.066	BIO
116	5001.672	8373.066	VDD15
117	4884.672	8373.066	VDD16

† Measured from corner of active area.



MECHANICAL DATA

MOUNT AND BOND



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SMJ320C50KGDM50C	PREVIEW	XCEPT	KGD	0		TBD	Call TI	Call TI	
SMJ320C50KGDM66C	PREVIEW	XCEPT	KGD	0		TBD	Call TI	Call TI	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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