SMJ320LC549
FIXED-POINT DIGITAL SIGNAL PROCESSOR

SGUS032B – OCTOBER 2002 – REVISED MAY 2003

- Processed to MIL-PRF-38535 (QML)
- Advanced Multibus Architecture With Three Separate 16-Bit Data Memory Buses and One Program Memory Bus
- 40-Bit Arithmetic Logic Unit (ALU) Including a 40-Bit Barrel Shifter and Two Independent 40-Bit Accumulators
- 17- x 17-Bit Parallel Multiplier Coupled to a 40-Bit Dedicated Adder for Non-Pipelined Single-Cycle Multiply/Accumulate (MAC) Operation
- Compare, Select, and Store Unit (CSSU) for the Add/Compare Selection of the Viterbi Operator
- Exponent Encoder to Compute an Exponent Value of a 40-Bit Accumulator Value in a Single Cycle
- Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)
- Data Bus With a Bus Holder Feature
- Address Bus With a Bus Holder Feature
- Extended Addressing Mode for 8M × 16-Bit Maximum Addressable External Program Space
- 192K x 16-Bit Maximum Addressable Memory Space (64K Words Program, 64K Words Data, and 64K Words I/O)
- On-Chip ROM with Some Configurable to Program/Data Memory
- Dual-Access On-Chip RAM
- Single-Access On-Chip RAM
- Single-Instruction Repeat and Block-Repeat Operations for Program Code
- Block-Memory-Move Instructions for Better Program and Data Management
- Instructions With a 32-Bit Long Word Operand
- Instructions With Two- or Three-Operand Reads
- Arithmetic Instructions With Parallel Store and Parallel Load
- Conditional Store Instructions
- Fast Return From Interrupt
- On-Chip Peripherals
  - Software-Programmable Wait-State Generator and Programmable Bank Switching
  - On-Chip Phase-Locked Loop (PLL) Clock Generator With Internal Oscillator or External Clock Source
  - Time-Division Multiplexed (TDM) Serial Port
  - Buffered Serial Port (BSP)
  - 8-Bit Parallel Host-Port Interface (HPI)
  - One 16-Bit Timer
  - External-Input/Output (XIO) Off Control to Disable the External Data Bus, Address Bus and Control Signals
- Power Consumption Control With IDLE1, IDLE2, and IDLE3 Instructions With Power-Down Modes
- CLKOUT Off Control to Disable CLKOUT
- On-Chip Scan-Based Emulation Logic, IEEE Std 1149.1† (JTAG) Boundary Scan Logic
- 16.7-ns Single-Cycle Fixed-Point Instruction Execution Time (60 MIPS) for 3.3-V Power Supply
- Packaging
  - 164-Pin Ceramic Quad Flat Package (HFG)
- –55°C to 115°C Operating Temperature Range, QML Processing

† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

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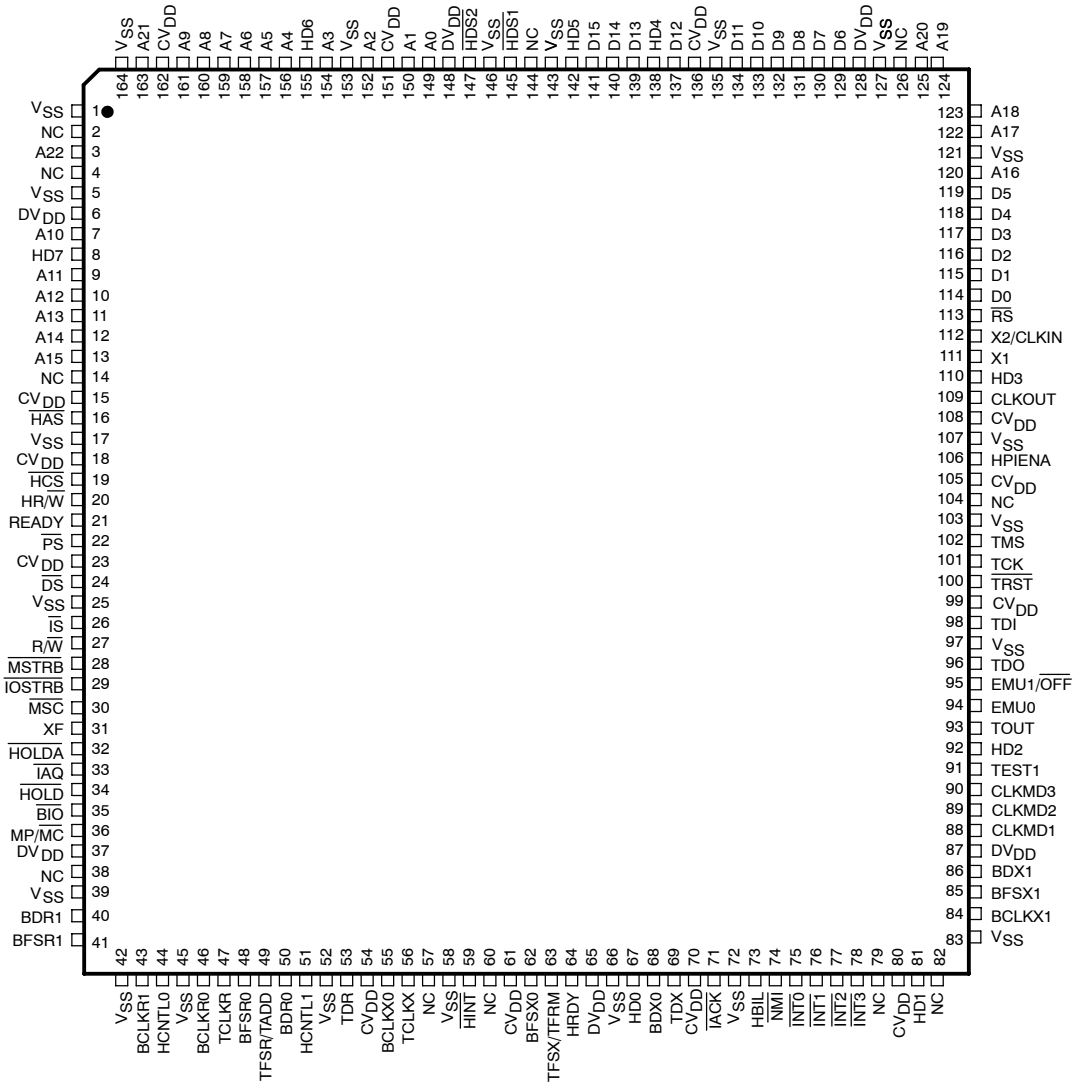
description

The SMJ320LC549 fixed-point, digital signal processor (DSP) (hereafter referred to as the 549) is based on an advanced modified Harvard architecture that has one program memory bus and three data memory buses. The processor also provides an arithmetic logic unit (ALU) that has a high degree of parallelism, application-specific hardware logic, on-chip memory, and additional on-chip peripherals. The 549 also utilizes a highly specialized instruction set, which is the basis of its operational flexibility and speed.

Separate program and data spaces allow simultaneous access to program instructions and data, providing the high degree of parallelism. Two reads and one write operation can be performed in a single cycle. Instructions with parallel store and application-specific instructions can fully utilize this architecture. In addition, data can be transferred between data and program spaces. Such parallelism supports a powerful set of arithmetic, logic, and bit-manipulation operations that can all be performed in a single machine cycle. In addition, the 549 includes the control mechanisms to manage interrupts, repeated operations, and function calls.

This data sheet contains the pin layouts, signal descriptions, and electrical specifications for the SMJ320LC549 DSP. For additional information, see the *TMS320C54x, TMS320LC54x, TMS320VC54x Fixed-Point Digital Signal Processors* data sheet (literature number SPRS039). The SPRS039 is considered a family functional overview and should be used in conjunction with this data sheet.

HFG PACKAGE†‡
(TOP VIEW)



NC – No internal connection

† NC = No connection

‡ DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU, and V_{SS} is the ground for both the I/O pins and the core CPU.

The 549 signal descriptions table lists each terminal name, function, and operating mode(s) for the 164-pin ceramic quad flatpack (CQFP).

The letter B in front of CLKRn, FSRn, DRn, CLKXn, FSXn, and DXn pin names denotes buffered serial port (BSP), where n = 0 or 1 port. The letter T in front of CLKR, FSR, DR, CLKX, FSX, and DX pin names denotes time-division multiplexed (TDM) serial port.

Pin Assignments for the 164-Pin HFG Package†

PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME
1	V_{SS}	42	V_{SS}	83	V_{SS}	124	A19
2	NC	43	BCLKR1	84	BCLKX1	125	A20
3	A22	44	HCNTL0	85	BFSX1	126	NC
4	NC	45	V_{SS}	86	BDX1	127	V_{SS}
5	V_{SS}	46	BCLKR0	87	DV_{DD}	128	DV_{DD}
6	DV_{DD}	47	TCLKR	88	CLKMD1	129	D6
7	A10	48	BFSR0	89	CLKMD2	130	D7
8	HD7	49	TFSR/TADD	90	CLKMD3	131	D8
9	A11	50	BDR0	91	TEST1	132	D9
10	A12	51	HCNTL1	92	HD2	133	D10
11	A13	52	V_{SS}	93	TOUT	134	D11
12	A14	53	TDR	94	EMU0	135	V_{SS}
13	A15	54	CV_{DD}	95	EMU1/$\overline{OFF}$	136	CV_{DD}
14	NC	55	BCLKX0	96	TDO	137	D12
15	CV_{DD}	56	TCLKX	97	V_{SS}	138	HD4
16	$\overline{HAS}$	57	NC	98	TDI	139	D13
17	V_{SS}	58	V_{SS}	99	CV_{DD}	140	D14
18	CV_{DD}	59	$\overline{HINT}$	100	$\overline{TRST}$	141	D15
19	$\overline{HCS}$	60	NC	101	TCK	142	HD5
20	HR/$\overline{W}$	61	CV_{DD}	102	TMS	143	V_{SS}
21	READY	62	BFSX0	103	V_{SS}	144	NC
22	$\overline{PS}$	63	TFSX/TFRM	104	NC	145	$\overline{HDS1}$
23	CV_{DD}	64	HRDY	105	CV_{DD}	146	V_{SS}
24	$\overline{DS}$	65	DV_{DD}	106	HPIENA	147	$\overline{HDS2}$
25	V_{SS}	66	V_{SS}	107	V_{SS}	148	DV_{DD}
26	$\overline{IS}$	67	HD0	108	CV_{DD}	149	A0
27	R/$\overline{W}$	68	BDX0	109	CLKOUT	150	A1
28	$\overline{MSTRB}$	69	TDX	110	HD3	151	CV_{DD}
29	$\overline{IOSTRB}$	70	CV_{DD}	111	X1	152	A2
30	$\overline{MSC}$	71	$\overline{IACK}$	112	X2/CLKIN	153	V_{SS}
31	XF	72	V_{SS}	113	$\overline{RS}$	154	A3
32	$\overline{HOLDA}$	73	HBIL	114	D0	155	HD6
33	$\overline{IAQ}$	74	$\overline{NMI}$	115	D1	156	A4
34	$\overline{HOLD}$	75	$\overline{INT0}$	116	D2	157	A5
35	$\overline{BIO}$	76	$\overline{INT1}$	117	D3	158	A6
36	MP/$\overline{MC}$	77	$\overline{INT2}$	118	D4	159	A7
37	DV_{DD}	78	$\overline{INT3}$	119	D5	160	A8
38	NC	79	NC	120	A16	161	A9
39	V_{SS}	80	CV_{DD}	121	V_{SS}	162	CV_{DD}
40	BDR1	81	HD1	122	A17	163	A21
41	BFSR1	82	NC	123	A18	164	V_{SS}

† DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU, and V_{SS} is the ground for both the I/O pins and the core CPU.

Signal Descriptions

TERMINAL NAME	TYPE†	DESCRIPTION
DATA SIGNALS		
A22 (MSB) A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 (LSB)	O/Z	Parallel port address bus A22 (MSB) through A0 (LSB). The sixteen LSBs (A15–A0) are multiplexed to address external data/program memory or I/O. A15–A0 are placed in the high-impedance state in the hold mode. A15–A0 also go into the high-impedance state when EMU1/$\overline{\text{OFF}}$ is low. The seven MSBs (A22 to A16) are used for extended program memory addressing. The address bus have a feature called bus holder that eliminates passive components and the power dissipation associated with it. The bus holders keep the address bus at the previous logic level when the bus goes into a high-impedance state. The bus holders on the address bus are always enabled.
D15 (MSB) D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 (LSB)	I/O/Z	Parallel port data bus D15 (MSB) through D0 (LSB). D15–D0 are multiplexed to transfer data between the core CPU and external data/program memory or I/O devices. D15–D0 are placed in the high-impedance state when not output or when $\overline{\text{RS}}$ or $\overline{\text{HOLD}}$ is asserted. D15–D0 also go into the high-impedance state when EMU1/$\overline{\text{OFF}}$ is low. The data bus has a feature called bus holder that eliminates passive components and the power dissipation associated with it. The bus holders keep the data bus at the previous logic level when the bus goes into a high-impedance state. These bus holders are enabled or disabled by the BH bit in the bank switching control register (BSCR).
INITIALIZATION, INTERRUPT AND RESET OPERATIONS		
$\overline{\text{IACK}}$	O/Z	Interrupt acknowledge signal. $\overline{\text{IACK}}$ indicates the receipt of an interrupt and that the program counter is fetching the interrupt vector location designated by A15–0. $\overline{\text{IACK}}$ also goes into the high-impedance state when EMU1/$\overline{\text{OFF}}$ is low.
$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ $\overline{\text{INT3}}$	I	External user interrupt inputs. $\overline{\text{INT0}}$–$\overline{\text{INT3}}$ are prioritized and are maskable by the interrupt mask register and the interrupt mode bit. $\overline{\text{INT0}}$ –$\overline{\text{INT3}}$ can be polled and reset by the interrupt flag register.

† I = Input, O = Output, Z = High impedance

Signal Descriptions (Continued)

TERMINAL NAME	TERMINAL TYPE†	DESCRIPTION
INITIALIZATION, INTERRUPT AND RESET OPERATIONS (CONTINUED)		
$\overline{NMI}$	I	Nonmaskable interrupt. $\overline{NMI}$ is an external interrupt that cannot be masked by way of the INTM or the IMR. When $\overline{NMI}$ is activated, the processor traps to the appropriate vector location.
$\overline{RS}$	I	Reset input. $\overline{RS}$ causes the DSP to terminate execution and forces the program counter to 0FF80h. When $\overline{RS}$ is brought to a high level, execution begins at location 0FF80h of the program memory. $\overline{RS}$ affects various registers and status bits.
MP/$\overline{MC}$	I	Microprocessor/microcomputer mode-select pin. If active-low at reset (microcomputer mode), MP/$\overline{MC}$ causes the internal program ROM to be mapped into the upper program memory space. In the microprocessor mode, off-chip memory and its corresponding addresses (instead of internal program ROM) are accessed by the DSP.
MULTIPROCESSING SIGNALS		
$\overline{BIO}$	I	Branch control input. A branch can be conditionally executed when $\overline{BIO}$ is active. If low, the processor executes the conditional instruction. The $\overline{BIO}$ condition is sampled during the decode phase of the pipeline for the XC instruction, and all other instructions sample $\overline{BIO}$ during the read phase of the pipeline.
XF	O/Z	External flag output (latched software-programmable signal). XF is set high by the SSBX XF instruction, set low by RSBX XF instruction or by loading the ST1 status register. XF is used for signaling other processors in multiprocessor configurations or as a general-purpose output pin. XF goes into the high-impedance state when $\overline{OFF}$ is low, and is set high at reset.
MEMORY CONTROL SIGNALS		
$\overline{DS}$ $\overline{PS}$ $\overline{IS}$	O/Z	Data, program, and I/O space select signals. $\overline{DS}$, $\overline{PS}$, and $\overline{IS}$ are always high unless driven low for communicating to a particular external space. Active period corresponds to valid address information. Placed into a high-impedance state in hold mode. $\overline{DS}$, $\overline{PS}$, and $\overline{IS}$ also go into the high-impedance state when EMU1/$\overline{OFF}$ is low.
$\overline{MSTRB}$	O/Z	Memory strobe signal. $\overline{MSTRB}$ is always high unless low-level asserted to indicate an external bus access to data or program memory. Placed in high-impedance state in hold mode. $\overline{MSTRB}$ also goes into the high-impedance state when $\overline{OFF}$ is low.
READY	I	Data-ready input. READY indicates that an external device is prepared for a bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again. Note that the processor performs ready-detection if at least two software wait states are programmed. The READY signal is not sampled until the completion of the software wait states.
R/$\overline{W}$	O/Z	Read/write signal. R/$\overline{W}$ indicates transfer direction during communication to an external device and is normally high (in read mode), unless asserted low when the DSP performs a write operation. Placed in the high-impedance state in hold mode, R/$\overline{W}$ also goes into the high-impedance state when EMU1/$\overline{OFF}$ is low.
$\overline{IOSTRB}$	O/Z	I/O strobe signal. $\overline{IOSTRB}$ is always high unless low level asserted to indicate an external bus access to an I/O device. Placed in high-impedance state in hold mode. $\overline{IOSTRB}$ also goes into the high-impedance state when EMU1/$\overline{OFF}$ is low.
$\overline{HOLD}$	I	Hold input. $\overline{HOLD}$ is asserted to request control of the address, data, and control lines. When acknowledged by the ’54x, these lines go into high-impedance state.
$\overline{HOLDA}$	O/Z	Hold acknowledge signal. $\overline{HOLDA}$ indicates to the external circuitry that the processor is in a hold state and that the address, data, and control lines are in a high-impedance state, allowing them to be available to the external circuitry. $\overline{HOLDA}$ also goes into the high-impedance state when EMU1/$\overline{OFF}$ is low.
$\overline{MSC}$	O/Z	Microstate complete signal. Goes low on CLKOUT falling at the start of the first software wait state. Remains low until one CLKOUT cycle before the last programmed software wait state. If connected to the READY line, $\overline{MSC}$ forces one external wait state after the last internal wait state has been completed. $\overline{MSC}$ also goes into the high-impedance state when EM1/$\overline{OFF}$ is low.

† I = Input, O = Output, Z = High impedance

Signal Descriptions (Continued)

TERMINAL NAME	TERMINAL TYPE†	DESCRIPTION
MEMORY CONTROL SIGNALS (CONTINUED)		
$\overline{IAQ}$	O/Z	Instruction acquisition signal. $\overline{IAQ}$ is asserted (active low) when there is an instruction address on the address bus and goes into the high-impedance state when EMU1/$\overline{OFF}$ is low.
OSCILLATOR/TIMER SIGNALS		
CLKOUT	O/Z	Master clock output signal. CLKOUT cycles at the machine-cycle rate of the CPU. The internal machine cycle is bounded by the falling edges of this signal. CLKOUT also goes into the high-impedance state when EMU1/$\overline{OFF}$ is low.
CLKMD1 CLKMD2 CLKMD3	I	Clock mode external/internal input signals. CLKMD1, CLKMD2, and CLKMD3 allow you to select and configure different clock modes, such as crystal, external clock, and various PLL factors. Refer to PLL section for a detailed functional description of these pins.
X2/CLKIN	I	Input pin to internal oscillator from the crystal. If the internal (crystal) oscillator is not being used, a clock can become input to the device using this pin. The internal machine cycle time is determined by the clock operating-mode pins (CLKMD1, CLKMD2 and CLKMD3).
X1	O	Output pin from the internal oscillator for the crystal. If the internal oscillator is not used, X1 should be left unconnected. X1 does not go into the high-impedance state when EMU1/$\overline{OFF}$ is low.
TOUT	O/Z	Timer output. TOUT signals a pulse when the on-chip timer counts down past zero. The pulse is a CLKOUT-cycle wide. TOUT also goes into the high-impedance state when EMU1/$\overline{OFF}$ is low.
BUFFERED SERIAL PORT 0 AND BUFFERED SERIAL PORT 1 SIGNALS		
BCLKR0 BCLKR1	I	Receive clocks. External clock signal for clocking data from the data-receive (DR) pin into the buffered serial port receive shift registers (RSRs). Must be present during buffered serial port transfers. If the buffered serial port is not being used, BCLKR0 and BCLKR1 can be sampled as an input by way of IN0 bit of the SPC register.
BCLKX0 BCLKX1	I/O/Z	Transmit clock. Clock signal for clocking data from the serial port transmit shift register (XSR) to the data transmit (DX) pin. BCLKX can be an input if MCM in the serial port control register is cleared to 0. It also can be driven by the device at 1/(CLKDV + 1) where CLKDV range is 0–31 CLKOUT frequency when MCM is set to 1. If the buffered serial port is not used, BCLKX can be sampled as an input by way of IN1 of the SPC register. BCLKX0 and BCLKX1 go into the high-impedance state when $\overline{OFF}$ is low.
BDR0 BDR1	I	Buffered serial-data-receive input. Serial data is received in the RSR by BDR0/BDR1.
BDX0 BDX1	O/Z	Buffered serial-port-transmit output. Serial data is transmitted from the XSR by way of BDX. BDX0 and BDX1 are placed in the high-impedance state when not transmitting and when EMU1/$\overline{OFF}$ is low.
BFSR0 BFSR1	I	Frame synchronization pulse for receive input. The falling edge of the BFSR pulse initiates the data-receive process, beginning the clocking of the RSR.
BFSX0 BFSX1	I/O/Z	Frame synchronization pulse for transmit input/output. The falling edge of the BFSX pulse initiates the data-transmit process, beginning the clocking of the XSR. Following reset, the default operating condition of BFSX is an input. BFSX0 and BFSX1 can be selected by software to be an output when TXM in the serial control register is set to 1. This pin goes into the high-impedance state when EMU1/$\overline{OFF}$ is low.
TDM SERIAL PORT SIGNALS		
TCLKR	I	TDM receive clock input
TDR	I	TDM serial data-receive input
TFSR/TADD	I/O	TDM receive frame synchronization or TDM address
TCLKX	I/O/Z	TDM transmit clock
TDX	O/Z	TDM serial data-transmit output
TFSX/TFRM	I/O/Z	TDM transmit frame synchronization

† I = Input, O = Output, Z = High impedance

Signal Descriptions (Continued)

TERMINAL NAME	TERMINAL TYPE†	DESCRIPTION
HOST-PORT INTERFACE SIGNALS		
HD0–HD7	I/O/Z	Parallel bidirectional data bus. HD0–HD7 are placed in the high-impedance state when not outputting data. The signals go into the high-impedance state when EMU1/$\overline{\text{OFF}}$ is low. These pins each have bus holders similar to those on the address/data bus, but which are always enabled.
HCNTL0 HCNTL1	I	Control inputs
HBIL	I	Byte-identification input
$\overline{\text{HCS}}$	I	Chip-select input
$\overline{\text{HDS1}}$ $\overline{\text{HDS2}}$	I	Data strobe inputs
$\overline{\text{HAS}}$	I	Address strobe input
HR/$\overline{\text{W}}$	I	Read/write input
HRDY	O/Z	Ready output. This signal goes into the high-impedance state when EMU1/$\overline{\text{OFF}}$ is low.
$\overline{\text{HINT}}$	O/Z	Interrupt output. When the DSP is in reset, this signal is driven high. The signal goes into the high-impedance state when EMU1/$\overline{\text{OFF}}$ is low.
HPIENA	I	HPI module select input. This signal must be tied to a logic 1 state to have HPI selected. If this input is left open or connected to ground, the HPI module will not be selected, internal pullup for the HPI input pins are enabled, and the HPI data bus has keepers set. This input is provided with an internal pull-down resistor which is active only when $\overline{\text{RS}}$ is low. HPIENA is sampled when $\overline{\text{RS}}$ goes high and ignored until $\overline{\text{RS}}$ goes low again. Refer to the Electrical Characteristics section for the input current requirements for this pin.
SUPPLY PINS		
CV_{DD}	Supply	$+V_{DD}$. CV_{DD} is the dedicated power supply for the core CPU.
DV_{DD}	Supply	$+V_{DD}$. DV_{DD} is the dedicated power supply for I/O pins.
V_{SS}	Supply	Ground. V_{SS} is the dedicated power ground for the device.
IEEE1149.1 TEST PINS		
TCK	I	IEEE standard 1149.1 test clock. Pin with internal pullup device. This is normally a free-running clock signal with a 50% duty cycle. The changes on the test-access port (TAP) of input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TDI	I	IEEE standard 1149.1 test data input. Pin with internal pullup device. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	O/Z	IEEE standard 1149.1 test data output. The contents of the selected register (instruction or data) is shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when the scanning of data is in progress. TDO also goes into the high-impedance state when EMU1/$\overline{\text{OFF}}$ is low.
TMS	I	IEEE standard 1149.1 test mode select. Pin with internal pullup device. This serial control input is clocked into the TAP controller on the rising edge of TCK.
$\overline{\text{TRST}}$	I	IEEE standard 1149.1 test reset. $\overline{\text{TRST}}$, when high, gives the IEEE standard 1149.1 scan system control of the operations of the device. If $\overline{\text{TRST}}$ is not connected or driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. Pin with internal pulldown device.
EMU0	I/O/Z	Emulator interrupt 0 pin. When $\overline{\text{TRST}}$ is driven low, EMU0 must be high for the activation of the EMU1/$\overline{\text{OFF}}$ condition. When $\overline{\text{TRST}}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output by way of IEEE standard 1149.1 scan system.

† I = Input, O = Output, Z = High impedance

Signal Descriptions (Continued)

TERMINAL NAME	TERMINAL TYPE†	DESCRIPTION
IEEE1149.1 TEST PINS (CONTINUED)		
EMU1/$\overline{\text{OFF}}$	I/O/Z	Emulator interrupt 1 pin/disable all outputs. When $\overline{\text{TRST}}$ is driven high, EMU1/$\overline{\text{OFF}}$ is used as an interrupt to or from the emulator system and is defined as input/output by way of IEEE standard 1149.1 scan system. When $\overline{\text{TRST}}$ is driven low, EMU1/$\overline{\text{OFF}}$ is configured as $\overline{\text{OFF}}$. The EMU1/$\overline{\text{OFF}}$ signal, when active low, puts all output drivers into the high-impedance state. Note that $\overline{\text{OFF}}$ is used exclusively for testing and emulation purposes (not for multiprocessing applications). Therefore, for the $\overline{\text{OFF}}$ condition, the following conditions apply: $\overline{\text{TRST}}$ = low, EMU0 = high EMU1/$\overline{\text{OFF}}$ = low
DEVICE TEST PIN		
TEST1	I	Test1 – Reserved for internal use only. **This pin must not be connected (NC).**

† I = Input, O = Output, Z = High impedance

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage, DV_{DD} and CV_{DD}‡ . . . . . –0.3 V to 4.6 V
Input voltage range . . . . . –0.3 V to 4.6 V
Output voltage range . . . . . –0.3 V to 4.6 V
Thermal resistance, Junction-to-Case, Θ_{JC} . . . . . 1.82°C/W
Operating case temperature range, T_C . . . . . –55°C to 115°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
DV_{DD}	Device supply voltage		3	3.3	3.6	V
CV_{DD}	Core supply voltage		3	3.3	3.6	V
V_{SS}	Supply voltage, GND			0		V
V_{IH}	High-level input voltage	Schmitt trigger inputs, DV_{DD} = 3.3±0.3 V§	2.5		DV_{DD} + 0.3*	V
		All other inputs	2		DV_{DD} + 0.3*	
V_{IL}	Low-level input voltage¶		–0.3*		0.8	V
I_{OH}	High-level output current				–300	μA
I_{OL}	Low-level output current				1.5	mA
T_C	Operating case temperature		–55		115	°C

*Not production tested.
§ The following pins have schmitt trigger inputs: $\overline{RS}$, $\overline{INTn}$, $\overline{NMI}$, X2/CLKIN, CLKMDn, TCK, HAS, HCS, HDSn, BCLKRn, TCLKR, BCLKXn, and TCLKX
¶ V_{IL} for TRST is not production tested.

See Figure 1 for 3.3-V device test load circuit values.

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

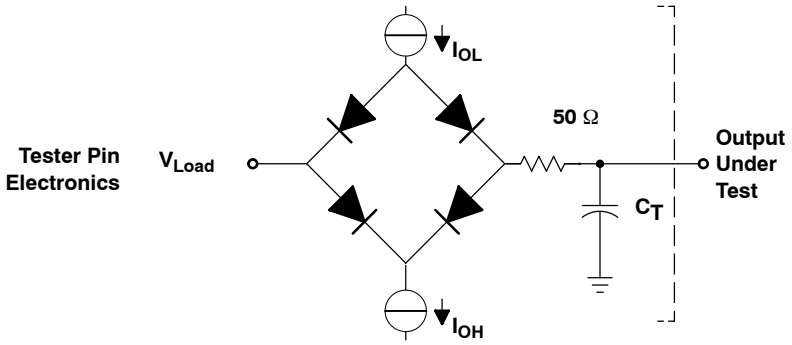
Timing parameter symbols used are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:	
a	access time
c	cycle time (period)
d	delay time
dis	disable time
en	enable time
f	fall time
h	hold time
r	rise time
su	setup time
t	transition time
v	valid time
w	pulse duration (width)
X	Unknown, changing, or don't care level

Letters and symbols and their meanings:	
H	High
L	Low
V	Valid
Z	High impedance

signal transition reference points

All timing references are made at a voltage of 1.5 volts, except rise and fall times which are referenced at the 10% and 90% points of the specified low and high logic levels, respectively.



Where: I_{OL} = 1.5 mA (all outputs)
I_{OH} = 300 μA (all outputs)
V_{Load} = 1.5 V
C_T = 40 pF typical load circuit capacitance.

Figure 1. 3.3-V Test Load Circuit

electrical characteristics and operating conditions

electrical characteristics over recommended operating case temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage‡		V_{DD} = 3.3±0.3 V, I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage‡		I_{OL} = MAX			0.4	V
I_{IZ}	Input current in high impedance	A[22:0]	V_{DD} = MAX§	–150		250	µA
		All other pins	V_{DD} = MAX, V_I = V_{SS} to V_{DD}	–10		10	
I_I	Input current (V_I = V_{SS} to V_{DD})	$\overline{TRST}$	With internal pulldown	–10		800	µA
		HPIENA	With internal pulldown, $\overline{RS}$ = 0	–20		400	
			$\overline{RS}$ = 1	–20		10	
		TMS, TCK, TDI, HPI¶	With internal pullups	–400		10	
		D[15:0], HD[7:0]	Bus holders enabled, V_{DD} = MAX§	–150		250	
		X2/CLKIN	Oscillator enabled	– 40		40	
		All other input-only pins		–10		10	
I_{DDC}	Supply current, core CPU		V_{DD} = 3.3 V, f_x = 40 MHz,# T_C = 25°C		28‖		mA
I_{DDP}	Supply current, pins		DV_{DD} = 3.3 V, f_x = 40 MHz,# T_C = 25°C		10.8☆		mA
I_{DD}	Supply current, standby	IDLE2	PLL × 1 mode, 40 MHz input		2		mA
		IDLE3	Divide-by-two mode, CLKIN stopped		15		µA
C_i	Input capacitance					15	pF
C_o	Output capacitance					15	pF

† All values are typical unless otherwise specified.
‡ All input and output voltage levels except $\overline{RS}$, $\overline{INT0}$–$\overline{INT3}$, $\overline{NMI}$, X2/CLKIN, CLKMD1–CLKMD3 are LVTTL-compatible. Not applicable to X1 which is an analog signal to a crystal oscillator.
§ $V_{IL(MIN)} \le V_I \le V_{IL(MAX)}$ or $V_{IH(MIN)} \le V_I \le V_{IH(MAX)}$
¶ HPI input signals except for HPIENA.
# Clock mode: PLL × 1 with external source
‖ This value was obtained with 50% usage of MAC and 50% usage of NOP instructions. Actual operating current varies with program being executed.
☆ This value was obtained with single-cycle external writes, CLKOFF = 0 and load = 15 pF. For more details on how this calculation is performed, refer to the *Calculation of TMS320C54x Power Dissipation* application report (literature number SPRA164).

internal oscillator with external crystal

The internal oscillator is enabled by selecting the appropriate clock mode at reset (this is device-dependent – see PLL section) and connecting a crystal or ceramic resonator across X1 and X2/CLKIN. The CPU clock frequency is one-half the crystal's oscillation frequency following reset. After reset, the clock mode of the devices with the software PLL can also be changed to divide-by-four. Since the internal oscillator can be used as a clock source to the PLL, the crystal oscillation frequency can be multiplied to generate the CPU clock if desired.

The crystal should be in fundamental mode operation and parallel resonant with an effective series resistance of 30ohms and power dissipation of 1 mW. The connection of the required circuit, consisting of the crystal and two load capacitors, is shown in Figure 2. The load capacitors, C_1 and C_2, should be chosen such that the equation below is satisfied. C_L in the equation is the load specified for the crystal.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

recommended operating conditions (see Figure 2)

		549-60		UNIT
		MIN	MAX	
f_x	Input clock frequency	10†*	20‡*	MHz

*Not production tested.
† This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞.
‡ It is recommended that the PLL clocking option be used for maximum frequency operation.

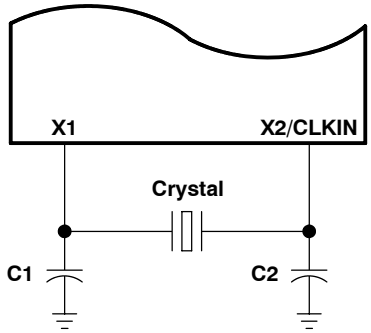


Figure 2. Internal Divide-by-Two Clock Option With External Crystal

divide-by-two/divide-by-four clock option – PLL disabled

The frequency of the reference clock provided at the X2/CLKIN pin can be divided by a factor of two or four to generate the internal machine cycle. The selection of the clock mode is described in the clock generator section.

When an external clock source is used, the frequency injected must conform to specifications listed in the timing requirements table.

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 2 and Figure 3, and the recommended operating conditions table)

PARAMETER		549-60			UNIT
		MIN	TYP	MAX	
$t_{c(CO)}$	Cycle time, CLKOUT		$2t_{c(CI)}$	†	ns
$t_{d(CIH-CO)}$	Delay time, X2/CLKIN high to CLKOUT high/low	3*	6	10*	ns
$t_{f(CO)}$	Fall time, CLKOUT†		2		ns
$t_{r(CO)}$	Rise time, CLKOUT†		2		ns
$t_{w(COL)}$	Pulse duration, CLKOUT low†	H–4*	H–2	H*	ns
$t_{w(COH)}$	Pulse duration, CLKOUT high†	H–4*	H–2	H*	ns

*Not production tested.
† This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞.

timing requirements (see Figure 3)

		549-60		UNIT
		MIN	MAX	
$t_{c(CI)}$	Cycle time, X2/CLKIN	20‡	†	ns
$t_{f(CI)}$	Fall time, X2/CLKIN		8*	ns
$t_{r(CI)}$	Rise time, X2/CLKIN		8*	ns
$t_{w(CIL)}$	Pulse duration, X2/CLKIN low	7*	†	ns
$t_{w(CIH)}$	Pulse duration, X2/CLKIN high	7*	†	ns

*Not production tested.
† This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞.
‡ It is recommended that the PLL clocking option be used for maximum frequency operation.

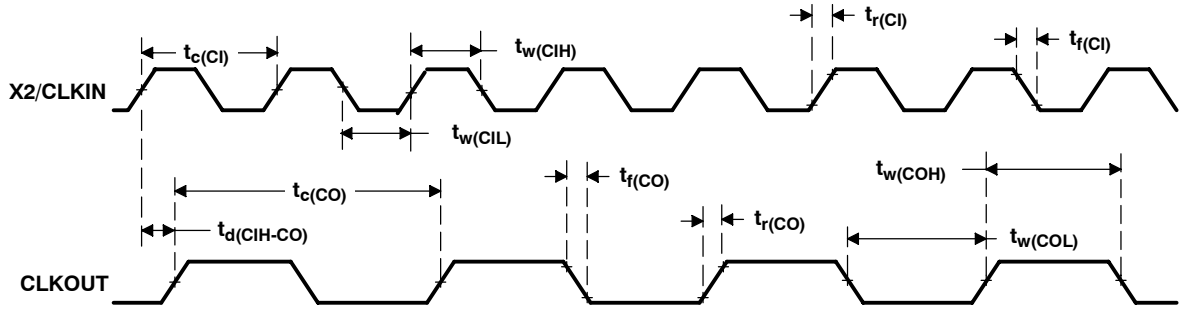


Figure 3. External Divide-by-Two Clock Timing

multiply-by-N clock option – PLL enabled

The frequency of the reference clock provided at the X2/CLKIN pin can be multiplied by a factor of N to generate the internal machine cycle. The selection of the clock mode and the value of N is described in the clock generator section.

When an external clock source is used, the frequency injected must conform to specifications listed in the timing requirements table.

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 2 and Figure 4, and the recommended operating conditions table)

PARAMETER		549-60			UNIT
		MIN	TYP	MAX	
$t_{c(CO)}$	Cycle time, CLKOUT	16.7†	$t_{c(CI)/N}$		ns
$t_{d(CIH-CO)}$	Delay time, X2/CLKIN high/low to CLKOUT high/low		6		ns
$t_{f(CO)}$	Fall time, CLKOUT		2		ns
$t_{r(CO)}$	Rise time, CLKOUT		2		ns
$t_{w(COL)}$	Pulse duration, CLKOUT low		H–2		ns
$t_{w(COH)}$	Pulse duration, CLKOUT high		H–2		ns
t_p	Transitory phase, PLL lock-up time			50*	µs

*Not production tested.
† Tested with N = 3 only.

timing requirements (see Figure 4)

			549-60		UNIT
			MIN	MAX	
$t_{c(CI)}$	Cycle time, X2/CLKIN	Integer PLL multiplier N (N = 1–15)	20‡*	200*	ns
		PLL multiplier N = x.5	20‡*	100*	
		PLL multiplier N = x.25, x.75	20‡*	50*	
$t_{f(CI)}$	Fall time, X2/CLKIN			8*	ns
$t_{r(CI)}$	Rise time, X2/CLKIN			8*	ns
$t_{w(CIL)}$	Pulse duration, X2/CLKIN low		5*		ns
$t_{w(CIH)}$	Pulse duration, X2/CLKIN high		5*		ns

*Not production tested.
‡ Note that for all values of $t_{c(CI)}$, the minimum $t_{c(CO)}$ period must not be exceeded.

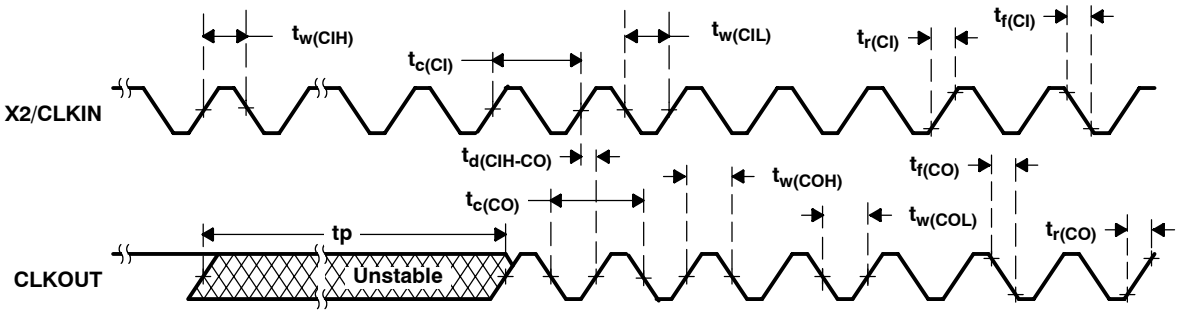


Figure 4. External Multiply-by-One Clock Timing

memory and parallel I/O interface timing

switching characteristics over recommended operating conditions for a memory read ($\overline{MSTRB}$ = 0)†‡ (see Figure 5)

PARAMETER		549-60		UNIT
		MIN	MAX	
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low§	–1.5*	7	ns
$t_{d(CLKH-A)}$	Delay time, address valid from CLKOUT high (transition)¶	–1.5*	6.5	ns
$t_{d(CLKL-MSL)}$	Delay time, $\overline{MSTRB}$ low from CLKOUT low	–1.5*	6	ns
$t_{d(CLKL-MSH)}$	Delay time, $\overline{MSTRB}$ high from CLKOUT low	–1.5*	6	ns
$t_{h(CLKL-A)R}$	Hold time, address valid after CLKOUT low§	–1.5*	7	ns
$t_{h(CLKH-A)R}$	Hold time, address valid after CLKOUT high¶	–1.5*	6.5	ns

*Not production tested.
† Address, $\overline{PS}$, and $\overline{DS}$ timings are all included in timings referenced as address.
‡ See Table 1, Table 2, and Table 3 for address bus timing variation with load capacitance.
§ In the case of a memory read preceded by a memory read
¶ In the case of a memory read preceded by a memory write

timing requirements for a memory read ($\overline{MSTRB}$ = 0) [H = 0.5 $t_{c(CO)}$]†‡ (see Figure 5)

		549-60		UNIT
		MIN	MAX	
$t_{a(A)M}$	Access time, read data access from address valid		2H–10*	ns
$t_{a(MSTRBL)}$	Access time, read data access from $\overline{MSTRB}$ low		2H–10*	ns
$t_{su(D)R}$	Setup time, read data before CLKOUT low	5		ns
$t_{h(D)R}$	Hold time, read data after CLKOUT low	2		ns
$t_{h(A-D)R}$	Hold time, read data after address invalid	1*		ns
$t_{h(D)MSTRBH}$	Hold time, read data after $\overline{MSTRB}$ high	0*		ns

*Not production tested.
† Address, $\overline{PS}$, and $\overline{DS}$ timings are all included in timings referenced as address.
‡ See Table 1, Table 2, and Table 3 for address bus timing variation with load capacitance.

memory and parallel I/O interface timing (continued)

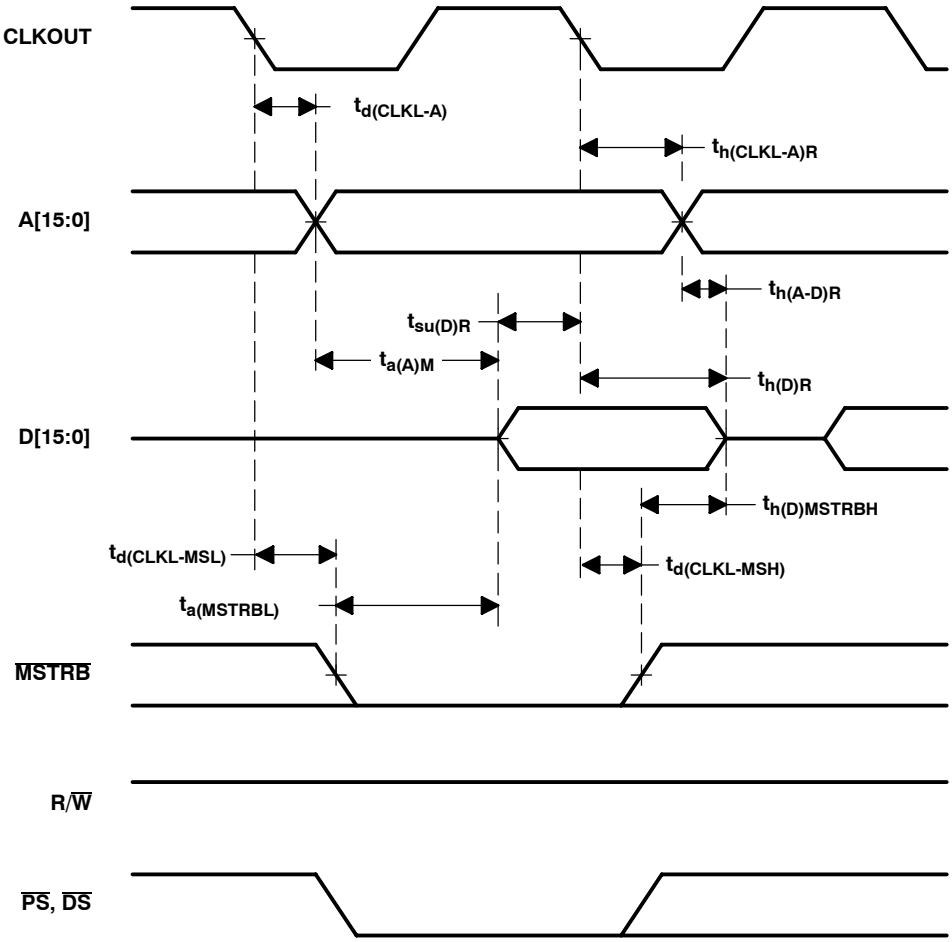


Figure 5. Memory Read (MSTRB = 0)

memory and parallel I/O interface timing (continued)

switching characteristics over recommended operating conditions for a memory write ($\overline{MSTRB}$ = 0) [H = 0.5 $t_{c(CO)}$]†‡ (see Figure 6)

PARAMETER		549-60		UNIT
		MIN	MAX	
$t_{d(CLKH-A)}$	Delay time, address valid from CLKOUT high§	–1.5*	6.5	ns
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low¶	–1.5*	7	ns
$t_{d(CLKL-MSL)}$	Delay time, $\overline{MSTRB}$ low from CLKOUT low	–1.5*	6	ns
$t_{d(CLKL-D)W}$	Delay time, data valid from CLKOUT low	0*	9	ns
$t_{d(CLKL-MSH)}$	Delay time, $\overline{MSTRB}$ high from CLKOUT low	–1.5*	6	ns
$t_{d(CLKH-RWL)}$	Delay time, R/$\overline{W}$ low from CLKOUT high	–1*	6	ns
$t_{d(CLKH-RWH)}$	Delay time, R/$\overline{W}$ high from CLKOUT high	–1*	5.5	ns
$t_{d(RWL-MSTRBL)}$	Delay time, $\overline{MSTRB}$ low after R/$\overline{W}$ low	H – 4*	H + 3*	ns
$t_{h(A)W}$	Hold time, address valid after CLKOUT high§	–1.5*	7*	ns
$t_{h(D)MSH}$	Hold time, write data valid after $\overline{MSTRB}$ high	H–5*	H+5*¶	ns
$t_{w(SL)MS}$	Pulse duration, $\overline{MSTRB}$ low	2H–5*		ns
$t_{su(A)W}$	Setup time, address valid before $\overline{MSTRB}$ low	2H–5*		ns
$t_{su(D)MSH}$	Setup time, write data valid before $\overline{MSTRB}$ high	2H–10	2H+8*§	ns

*Not production tested.
† Address, $\overline{PS}$, and $\overline{DS}$ timings are all included in timings referenced as address.
‡ See Table 1, Table 2, and Table 3 for address bus timing variation with load capacitance.
§ In the case of a memory write preceded by a memory write.
¶ In the case of a memory write preceded by an I/O cycle.

memory and parallel I/O interface timing (continued)

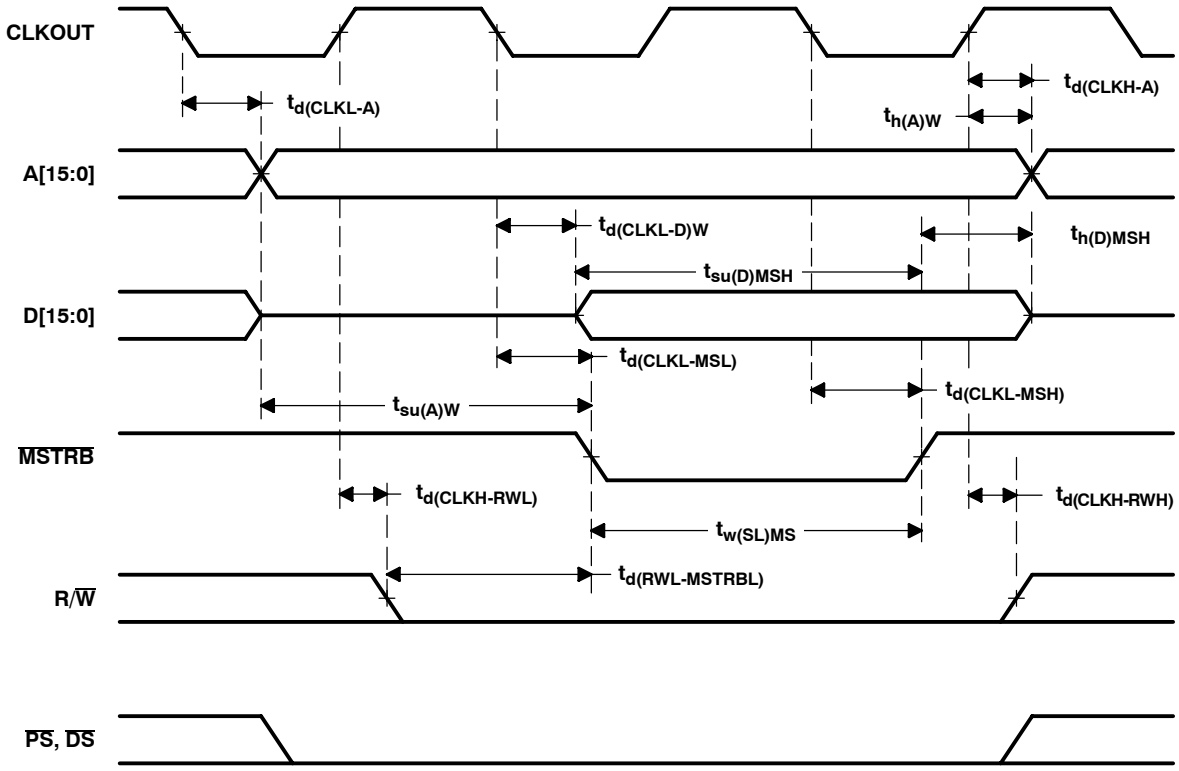


Figure 6. Memory Write ($\overline{\text{MSTRB}}$ = 0)

memory and parallel I/O interface timing (continued)

switching characteristics over recommended operating conditions for a parallel I/O port read ($\overline{IOSTRB}$ = 0)†‡ (see Figure 7)

PARAMETER		549-60 MIN	549-60 MAX	UNIT
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low	–1.5*	7	ns
$t_{d(CLKH-ISTRBL)}$	Delay time, $\overline{IOSTRB}$ low from CLKOUT high	–0.5*	6	ns
$t_{d(CLKH-ISTRBH)}$	Delay time, $\overline{IOSTRB}$ high from CLKOUT high	–1*	6	ns
$t_{h(A)IOR}$	Hold time, address after CLKOUT low	–1.5*	7*	ns

*Not production tested.
† Address and $\overline{IS}$ timings are included in timings referenced as address.
‡ See Table 1, Table 2, and Table 3 for address bus timing variation with load capacitance.

timing requirements for a parallel I/O port read ($\overline{IOSTRB}$ = 0) [H = 0.5 $t_{c(CO)}$]†‡ (see Figure 7)

		549-60 MIN	549-60 MAX	UNIT
$t_{a(A)IO}$	Access time, read data access from address valid		3H–10*	ns
$t_{a(ISTRBL)IO}$	Access time, read data access from $\overline{IOSTRB}$ low		2H–10*	ns
$t_{su(D)IOR}$	Setup time, read data before CLKOUT high	5*		ns
$t_{h(D)IOR}$	Hold time, read data after CLKOUT high	2*		ns
$t_{h(ISTRBH-D)R}$	Hold time, read data after $\overline{IOSTRB}$ high	0*		ns

*Not production tested.
† Address and $\overline{IS}$ timings are included in timings referenced as address.
‡ See Table 1, Table 2, and Table 3 for address bus timing variation with load capacitance.

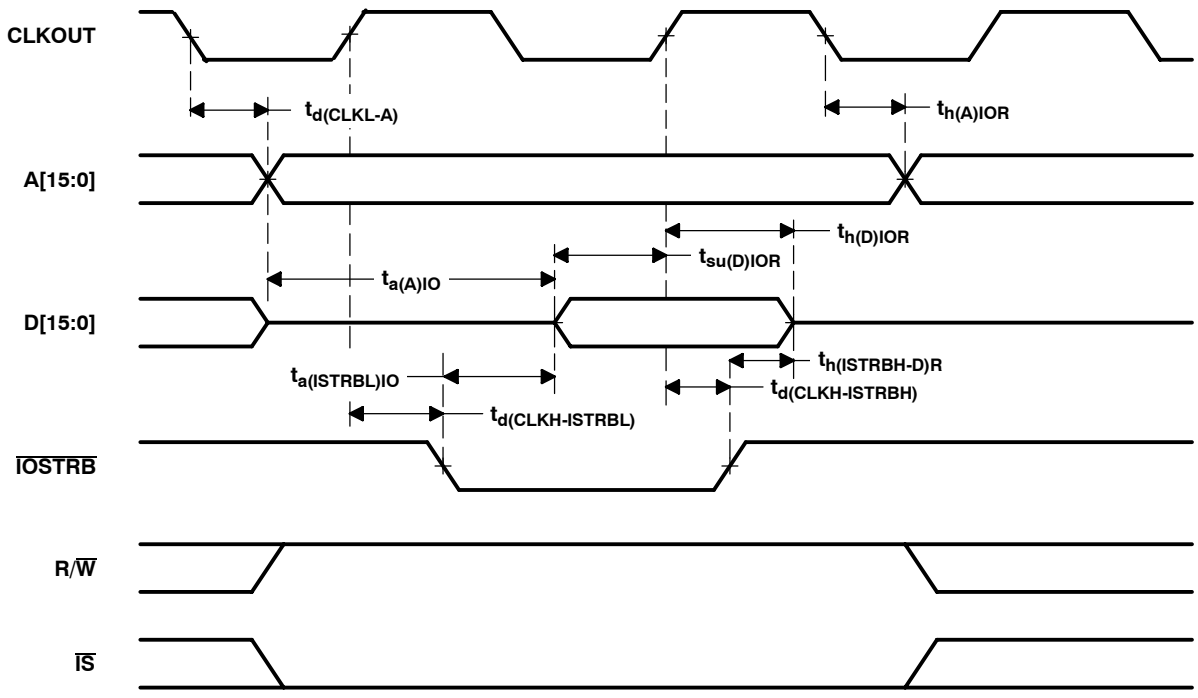


Figure 7. Parallel I/O Port Read ($\overline{IOSTRB}$ = 0)

memory and parallel I/O interface timing (continued)

switching characteristics over recommended operating conditions for a parallel I/O port write ($\overline{IOSTRB}$ = 0) [H = 0.5 $t_{c(CO)}$] (see Figure 8)†

PARAMETER		549-60		UNIT
		MIN	MAX	
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low‡	–1.5*	7	ns
$t_{d(CLKH-ISTRBL)}$	Delay time, $\overline{IOSTRB}$ low from CLKOUT high	–0.5*	6	ns
$t_{d(CLKH-D)IOW}$	Delay time, write data valid from CLKOUT high	H–5*	H+8.5	ns
$t_{d(CLKH-ISTRBH)}$	Delay time, $\overline{IOSTRB}$ high from CLKOUT high	–1*	6	ns
$t_{d(CLKL-RWL)}$	Delay time, R/$\overline{W}$ low from CLKOUT low	–0.5*	6	ns
$t_{d(CLKL-RWH)}$	Delay time, R/$\overline{W}$ high from CLKOUT low	–1*	6	ns
$t_{h(A)IOW}$	Hold time, address valid from CLKOUT low‡	–1.5*	7*	ns
$t_{h(D)IOW}$	Hold time, write data after $\overline{IOSTRB}$ high	H–5*	H+5*	ns
$t_{su(D)IOSTRBH}$	Setup time, write data before $\overline{IOSTRB}$ high	H–5*	H+2*	ns
$t_{su(A)IOSTRBL}$	Setup time, address valid before $\overline{IOSTRB}$ low	H–5*	H+5*	ns

*Not production tested.
† See Table 1, Table 2, and Table 3 for address bus timing variation with load capacitance.
‡ Address and $\overline{IS}$ timings are included in timings referenced as address.

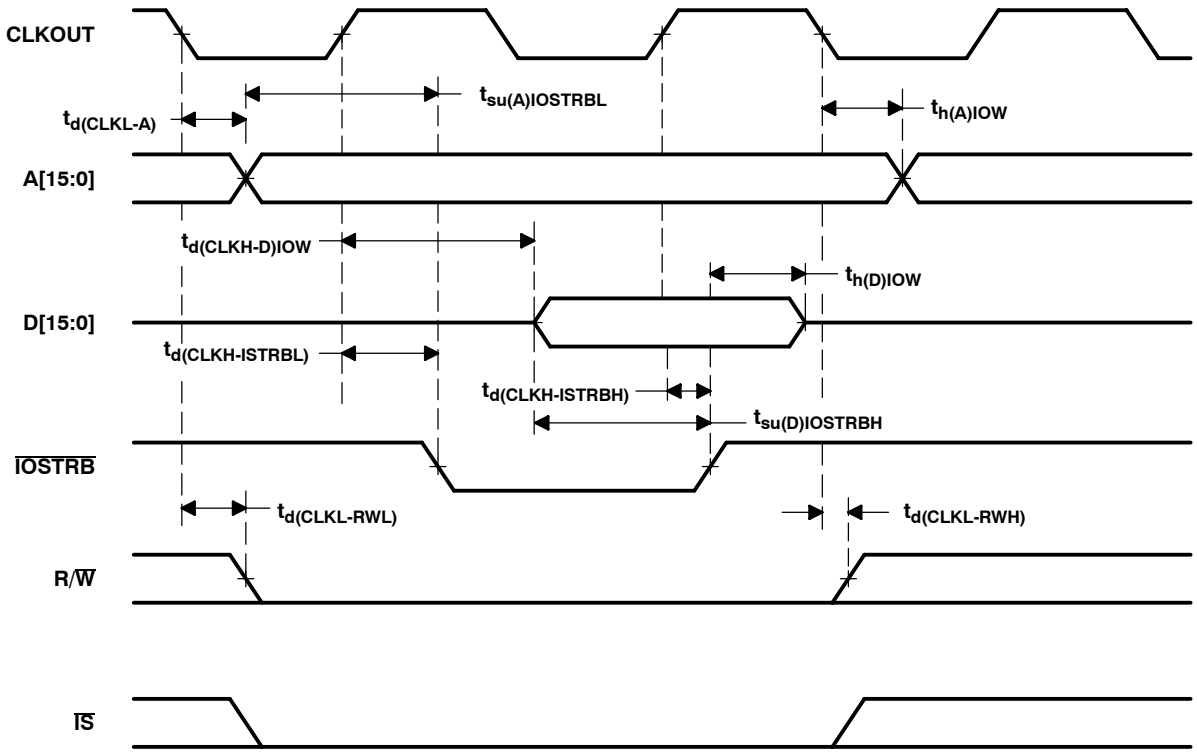


Figure 8. Parallel I/O Port Write ($\overline{IOSTRB}$ = 0)

I/O timing variation with load capacitance: SPICE simulation results

Condition: **Temperature : 125° C**
Capacitance : 0–100pF
Voltage : 2.7/3.0/3.3 V
Model : Weak/Nominal/Strong

Figure 9. Rise and Fall Time Diagram

Table 1. Timing Variation With Load Capacitance: [2.7 V] 10% – 90%

	WEAK		NOMINAL		STRONG	
	RISE	FALL	RISE	FALL	RISE	FALL
0 pF	0.476 ns	0.457 ns	0.429 ns	0.391 ns	0.382 ns	0.323 ns
10 pF	1.511 ns	1.278 ns	1.386 ns	1.148 ns	1.215 ns	1.049 ns
20 pF	2.551 ns	2.133 ns	2.350 ns	1.956 ns	2.074 ns	1.779 ns
30 pF	3.614 ns	3.011 ns	3.327 ns	2.762 ns	2.929 ns	2.512 ns
40 pF	4.664 ns	3.899 ns	4.394 ns	3.566 ns	3.798 ns	3.264 ns
50 pF	5.752 ns	4.786 ns	5.273 ns	4.395 ns	4.655 ns	4.010 ns
60 pF	6.789 ns	5.656 ns	6.273 ns	5.206 ns	5.515 ns	4.750 ns
70 pF	7.817 ns	6.598 ns	7.241 ns	6.000 ns	6.442 ns	5.487 ns
80 pF	8.897 ns	7.531 ns	8.278 ns	6.928 ns	7.262 ns	6.317 ns
90 pF	10.021 ns	8.332 ns	9.152 ns	7.735 ns	8.130 ns	7.066 ns
100 pF	11.072 ns	9.299 ns	10.208 ns	8.537 ns	8.997 ns	7.754 ns

Table 2. Timing Variation With Load Capacitance: [3 V] 10% – 90%

	WEAK		NOMINAL		STRONG	
	RISE	FALL	RISE	FALL	RISE	FALL
0 pF	0.436 ns	0.387 ns	0.398 ns	0.350 ns	0.345 ns	0.290 ns
10 pF	1.349 ns	1.185 ns	1.240 ns	1.064 ns	1.092 ns	0.964 ns
20 pF	2.273 ns	1.966 ns	2.098 ns	1.794 ns	1.861 ns	1.634 ns
30 pF	3.226 ns	2.765 ns	2.974 ns	2.539 ns	2.637 ns	2.324 ns
40 pF	4.168 ns	3.573 ns	3.849 ns	3.292 ns	3.406 ns	3.013 ns
50 pF	5.110 ns	4.377 ns	4.732 ns	4.052 ns	4.194 ns	3.710 ns
60 pF	6.033 ns	5.230 ns	5.660 ns	4.811 ns	5.005 ns	4.401 ns
70 pF	7.077 ns	5.997 ns	6.524 ns	5.601 ns	5.746 ns	5.117 ns
80 pF	8.020 ns	6.899 ns	7.416 ns	6.336 ns	6.559 ns	5.861 ns
90 pF	8.917 ns	7.709 ns	8.218 ns	7.124 ns	7.323 ns	6.498 ns
100 pF	9.885 ns	8.541 ns	9.141 ns	7.830 ns	8.101 ns	7.238 ns

I/O timing variation with load capacitance: SPICE simulation results (continued)

Table 3. Timing Variation With Load Capacitance: [3.3 V] 10% – 90%

	WEAK		NOMINAL		STRONG	
	RISE	FALL	RISE	FALL	RISE	FALL
0 pF	0.404 ns	0.361 ns	0.371 ns	0.310 ns	0.321 ns	0.284 ns
10 pF	1.227 ns	1.081 ns	1.133 ns	1.001 ns	1.000 ns	0.892 ns
20 pF	2.070 ns	1.822 ns	1.915 ns	1.675 ns	1.704 ns	1.530 ns
30 pF	2.931 ns	2.567 ns	2.719 ns	2.367 ns	2.414 ns	2.169 ns
40 pF	3.777 ns	3.322 ns	3.515 ns	3.072 ns	3.120 ns	2.823 ns
50 pF	4.646 ns	4.091 ns	4.319 ns	3.779 ns	3.842 ns	3.466 ns
60 pF	5.487 ns	4.859 ns	5.145 ns	4.503 ns	4.571 ns	4.142 ns
70 pF	6.405 ns	5.608 ns	5.980 ns	5.234 ns	5.301 ns	4.767 ns
80 pF	7.284 ns	6.463 ns	6.723 ns	5.873 ns	5.941 ns	5.446 ns
90 pF	8.159 ns	7.097 ns	7.560 ns	6.692 ns	6.740 ns	6.146 ns
100 pF	8.994 ns	7.935 ns	8.300 ns	7.307 ns	7.431 ns	6.822 ns

ready timing for externally generated wait states

timing requirements for externally generated wait states [H = 0.5 $t_{c(CO)}$]† (see Figure 10, Figure 11, Figure 12, and Figure 13)

		549-60		UNIT
		MIN	MAX	
$t_{su(RDY)}$	Setup time, READY before CLKOUT low	7		ns
$t_{h(RDY)}$	Hold time, READY after CLKOUT low	2		ns
$t_{v(RDY)MSTRB}$	Valid time, READY after $\overline{MSTRB}$ low‡		4H–10*	ns
$t_{h(RDY)MSTRB}$	Hold time, READY after $\overline{MSTRB}$ low‡	4H+1*		ns
$t_{v(RDY)IOSTRB}$	Valid time, READY after $\overline{IOSTRB}$ low‡		5H–10*	ns
$t_{h(RDY)IOSTRB}$	Hold time, READY after $\overline{IOSTRB}$ low‡	5H*		ns
$t_{v(MSCL)}$	Valid time, $\overline{MSC}$ low after CLKOUT low	–1*	6	ns
$t_{v(MSCH)}$	Valid time, $\overline{MSC}$ high after CLKOUT low	–1*	6	ns

*Not production tested.
† The hardware wait states can be used only in conjunction with the software wait states to extend the bus cycles. To generate wait states by READY, at least two software wait states must be programmed. READY is not sampled until the completion of the internal software wait states.
‡ These timings are included for reference only. The critical timings for READY are those referenced to CLKOUT.

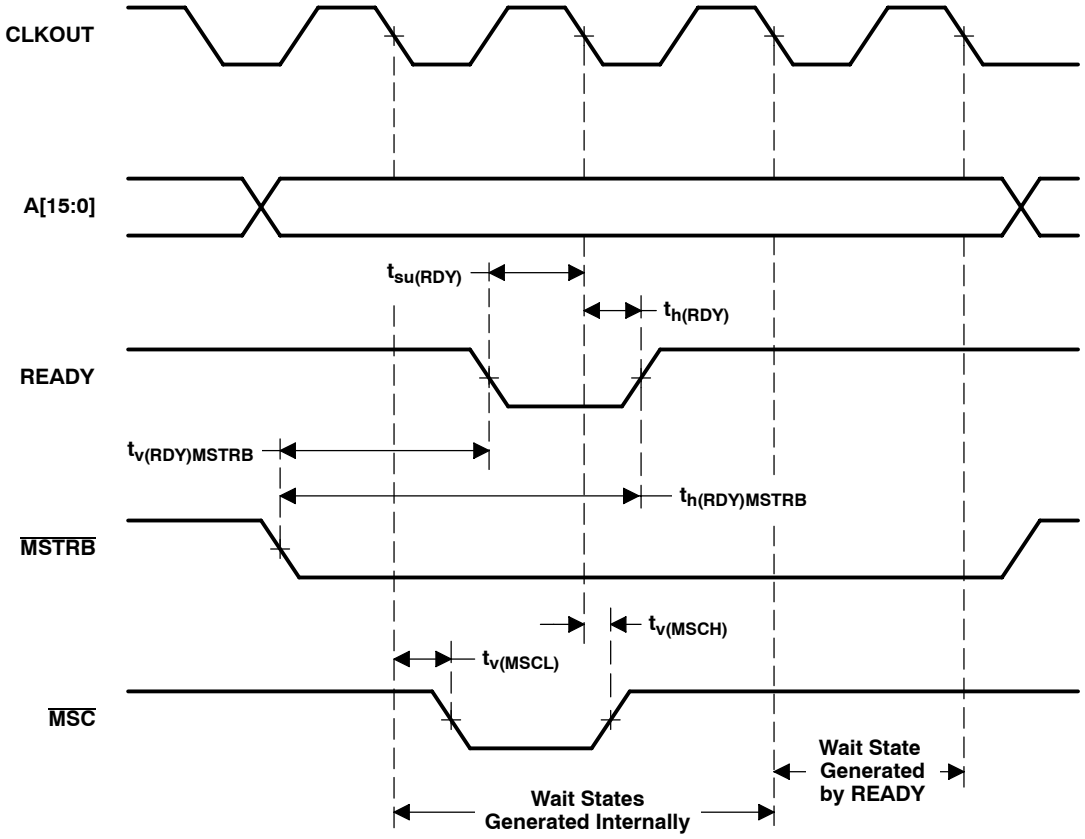


Figure 10. Memory Read With Externally Generated Wait States

ready timing for externally generated wait states (continued)

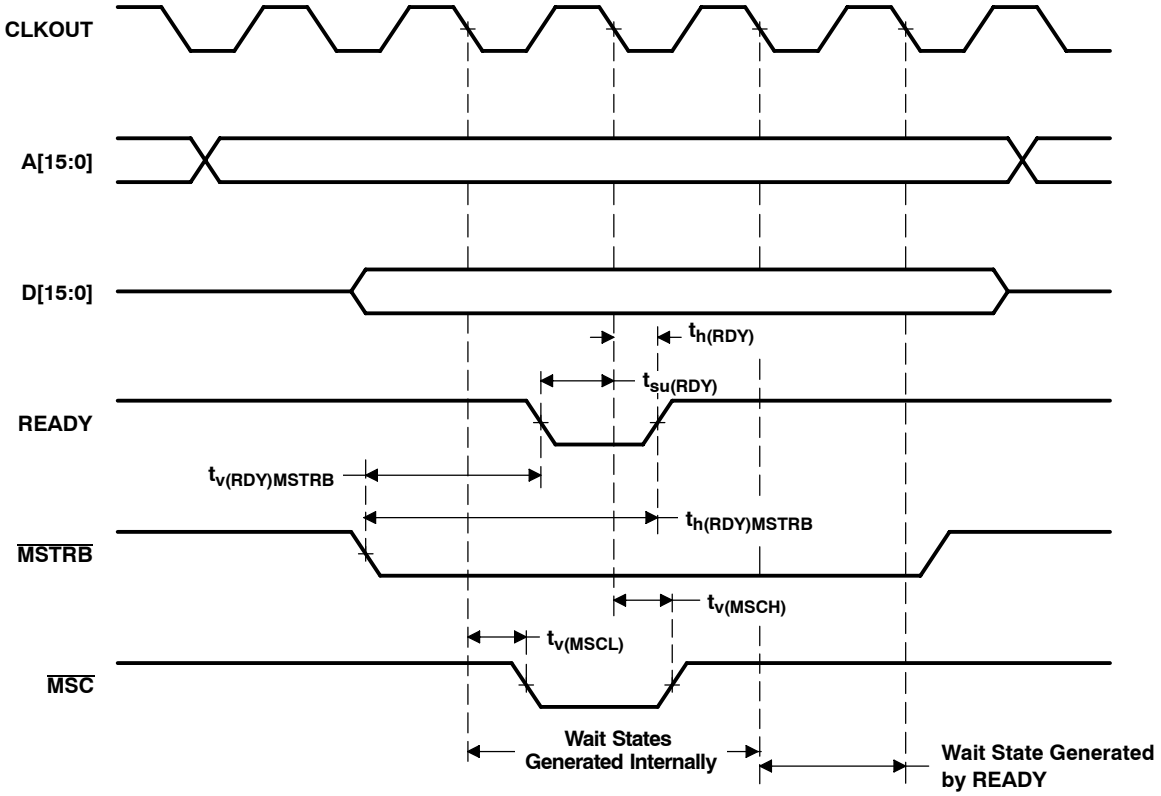


Figure 11. Memory Write With Externally Generated Wait States

ready timing for externally generated wait states (continued)

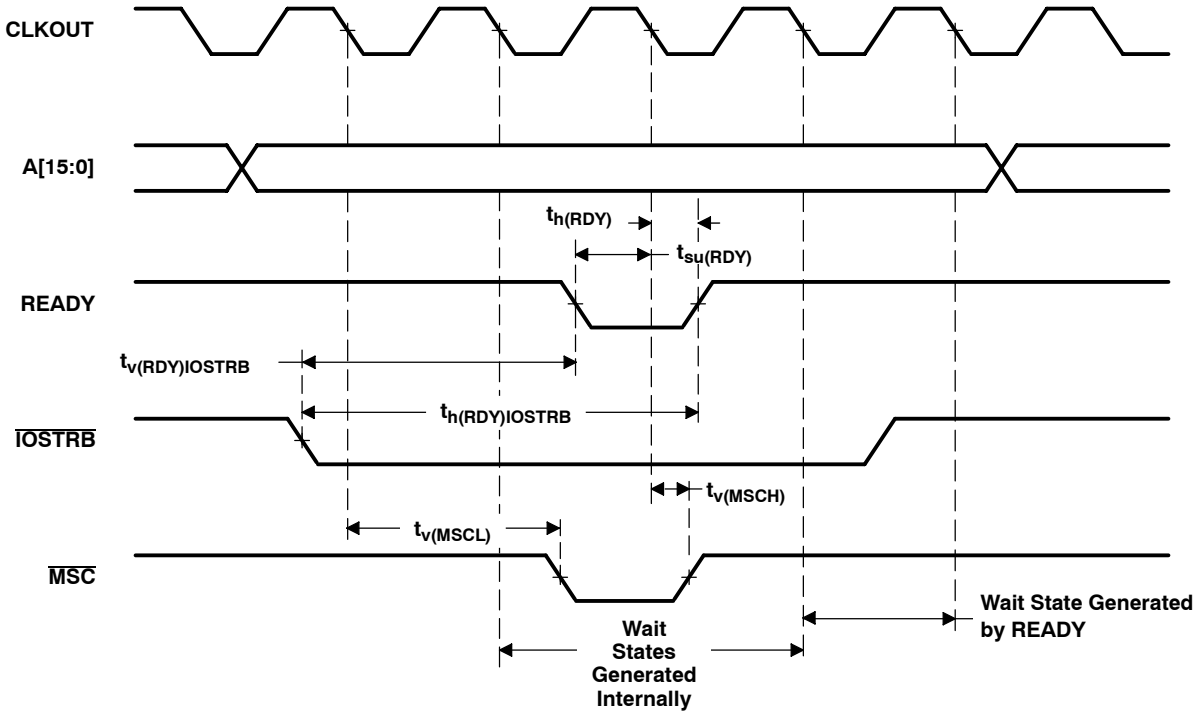


Figure 12. I/O Read With Externally Generated Wait States

ready timing for externally generated wait states (continued)

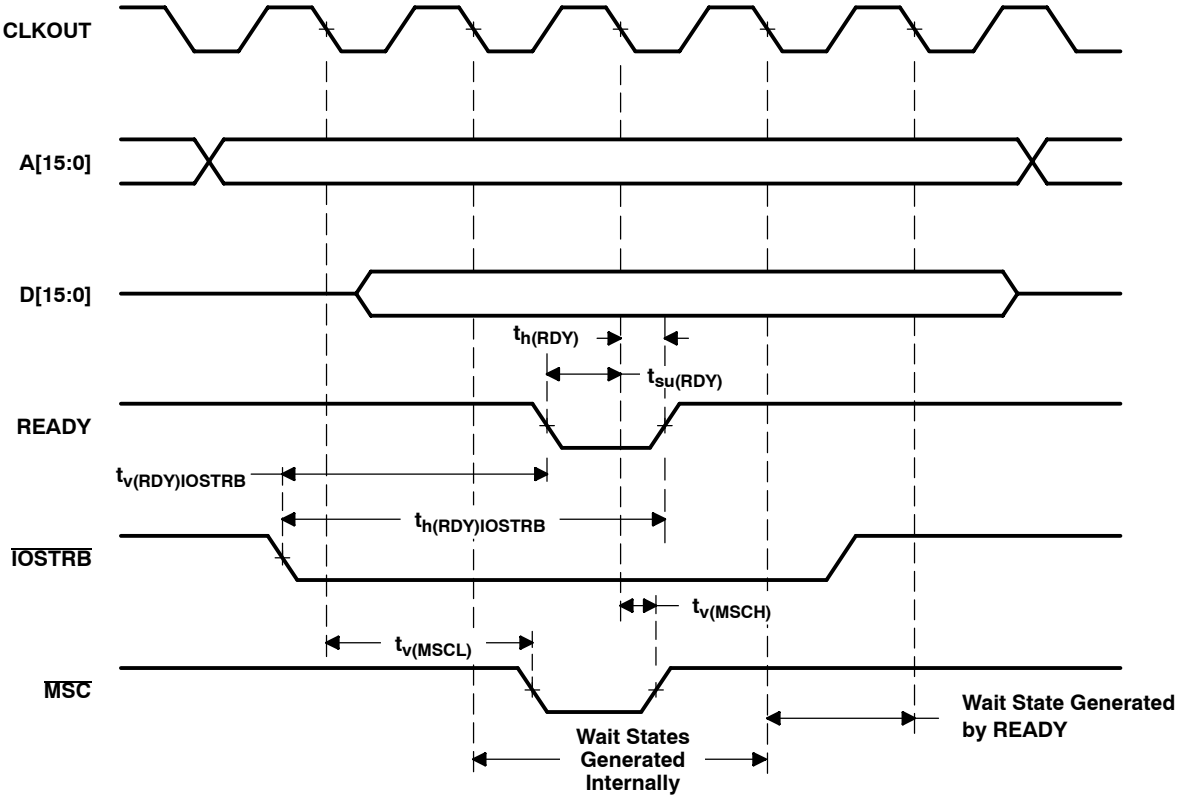


Figure 13. I/O Write With Externally Generated Wait States

$\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ timings

switching characteristics over recommended operating conditions for memory control signals and $\overline{\text{HOLDA}}$ [H = 0.5 $t_{c(CO)}$] (see Figure 14)

PARAMETER		549-60 MIN	549-60 MAX	UNIT
$t_{dis(CLKL-A)}$	Disable time, CLKOUT low to address, $\overline{\text{PS}}$, $\overline{\text{DS}}$, $\overline{\text{IS}}$ high impedance		5*	ns
$t_{dis(CLKL-RW)}$	Disable time, CLKOUT low to R/$\overline{\text{W}}$ high impedance		5*	ns
$t_{dis(CLKL-S)}$	Disable time, CLKOUT low to $\overline{\text{MSTRB}}$, $\overline{\text{IOSTRB}}$ high impedance		5*	ns
$t_{en(CLKL-A)}$	Enable time, CLKOUT low to address, $\overline{\text{PS}}$, $\overline{\text{DS}}$, $\overline{\text{IS}}$		2H+5*	ns
$t_{en(CLKL-RW)}$	Enable time, CLKOUT low to R/$\overline{\text{W}}$ enabled		2H+5*	ns
$t_{en(CLKL-S)}$	Enable time, CLKOUT low to $\overline{\text{MSTRB}}$, $\overline{\text{IOSTRB}}$ enabled		2H+5*	ns
$t_{v(HOLDA)}$	Valid time, $\overline{\text{HOLDA}}$ low after CLKOUT low	0*	5*	ns
	Valid time, $\overline{\text{HOLDA}}$ high after CLKOUT low	0*	5*	ns
$t_{w(HOLDA)}$	Pulse duration, $\overline{\text{HOLDA}}$ low duration	2H–3*		ns

*Not production tested.

timing requirements for $\overline{\text{HOLD}}$ [H = 0.5 $t_{c(CO)}$] (see Figure 14)

		549-60 MIN	549-60 MAX	UNIT
$t_{w(HOLD)}$	Pulse duration, $\overline{\text{HOLD}}$ low duration	4H+10*		ns
$t_{su(HOLD)}$	Setup time, $\overline{\text{HOLD}}$ before CLKOUT low	10*		ns

*Not production tested.

$\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ timings (continued)

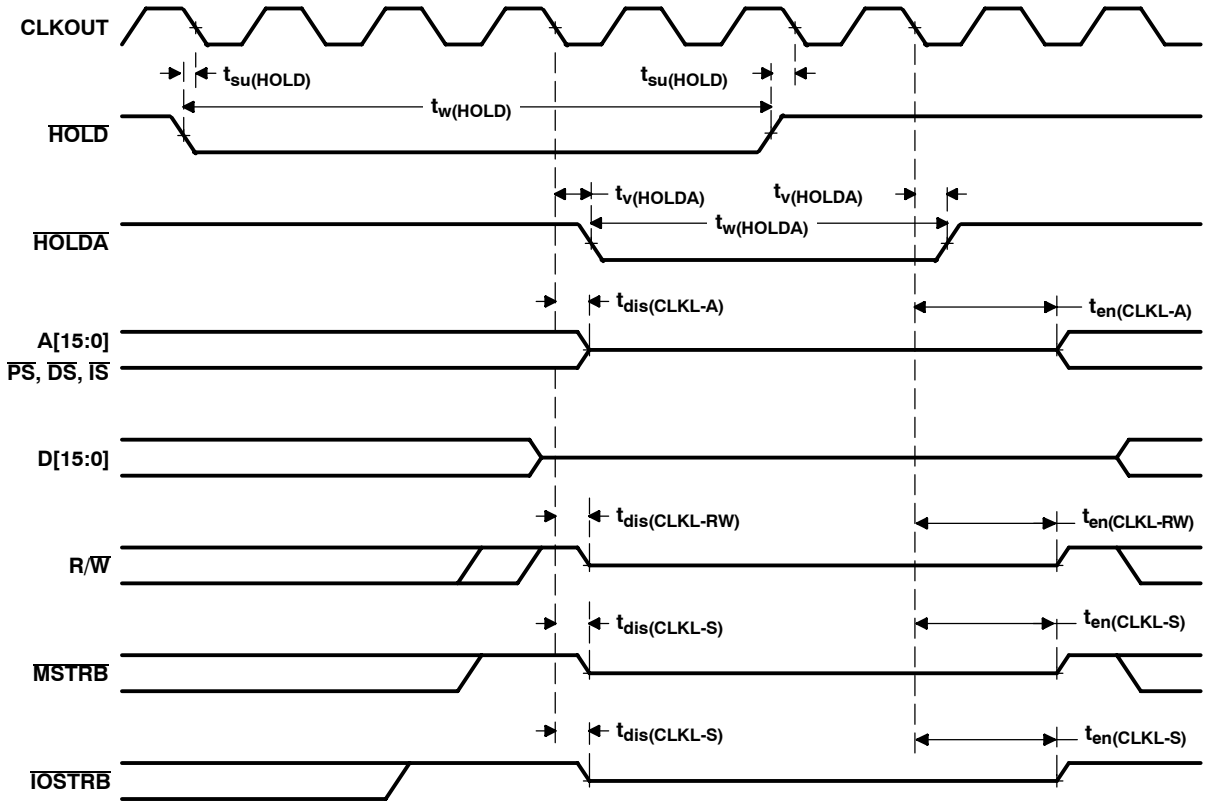


Figure 14. $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Timing (HM = 1)

reset, $\overline{BIO}$, interrupt, and MP/$\overline{MC}$ timings

timing requirements for reset, interrupt, $\overline{BIO}$, and MP/$\overline{MC}$ [H = 0.5 $t_{c(CO)}$] (see Figure 15, Figure 16, and Figure 17)

		549-60		UNIT
		MIN	MAX	
$t_{h(RS)}$	Hold time, $\overline{RS}$ after CLKOUT low	0*		ns
$t_{h(BIO)}$	Hold time, $\overline{BIO}$ after CLKOUT low	0		ns
$t_{h(INT)}$	Hold time, $\overline{INTn}$, $\overline{NMI}$, after CLKOUT low†	0		ns
$t_{h(MPMC)}$	Hold time, MP/$\overline{MC}$ after CLKOUT low	0*		ns
$t_{w(RSL)}$	Pulse duration, $\overline{RS}$ low‡§¶	4H+10*		ns
$t_{w(BIO)S}$	Pulse duration, $\overline{BIO}$ low, synchronous	2H+10*		ns
$t_{w(BIO)A}$	Pulse duration, $\overline{BIO}$ low, asynchronous	4H*		ns
$t_{w(INTH)S}$	Pulse duration, $\overline{INTn}$, $\overline{NMI}$ high (synchronous)	2H+10*		ns
$t_{w(INTH)A}$	Pulse duration, $\overline{INTn}$, $\overline{NMI}$ high (asynchronous)	4H*		ns
$t_{w(INTL)S}$	Pulse duration, $\overline{INTn}$, $\overline{NMI}$ low (synchronous)	2H+10*		ns
$t_{w(INTL)A}$	Pulse duration, $\overline{INTn}$, $\overline{NMI}$ low (asynchronous)	4H*		ns
$t_{w(INTL)WKP}$	Pulse duration, $\overline{INTn}$, $\overline{NMI}$ low for IDLE2/IDLE3 wakeup	10*		ns
$t_{su(RS)}$	Setup time, $\overline{RS}$ before X2/CLKIN low§	5*		ns
$t_{su(BIO)}$	Setup time, $\overline{BIO}$ before CLKOUT low	10	2H*	ns
$t_{su(INT)}$	Setup time, $\overline{INTn}$, $\overline{NMI}$, $\overline{RS}$ before CLKOUT low	10	2H*	ns
$t_{su(MPMC)}$	Setup time, MP/$\overline{MC}$ before CLKOUT low	10*		ns

*Not production tested.

† The external interrupts ($\overline{INT0}$–$\overline{INT3}$, $\overline{NMI}$) are synchronized to the core CPU by way of a two flip-flop synchronizer which samples these inputs with consecutive falling edges of CLKOUT. The input to the interrupt pins is required to represent a 1–0–0 sequence at the timing that is corresponding to three CLKOUTs sampling sequence.

‡ If the PLL mode is selected, then at power-on sequence, or at wakeup from IDLE3, $\overline{RS}$ must be held low for at least 50 μs to ensure synchronization and lock-in of the PLL.

§ Divide-by-two mode

¶ Note that $\overline{RS}$ may cause a change in clock frequency, therefore changing the value of H (see the PLL section).

reset, $\overline{\text{BIO}}$, interrupt, and MP/$\overline{\text{MC}}$ timings (continued)

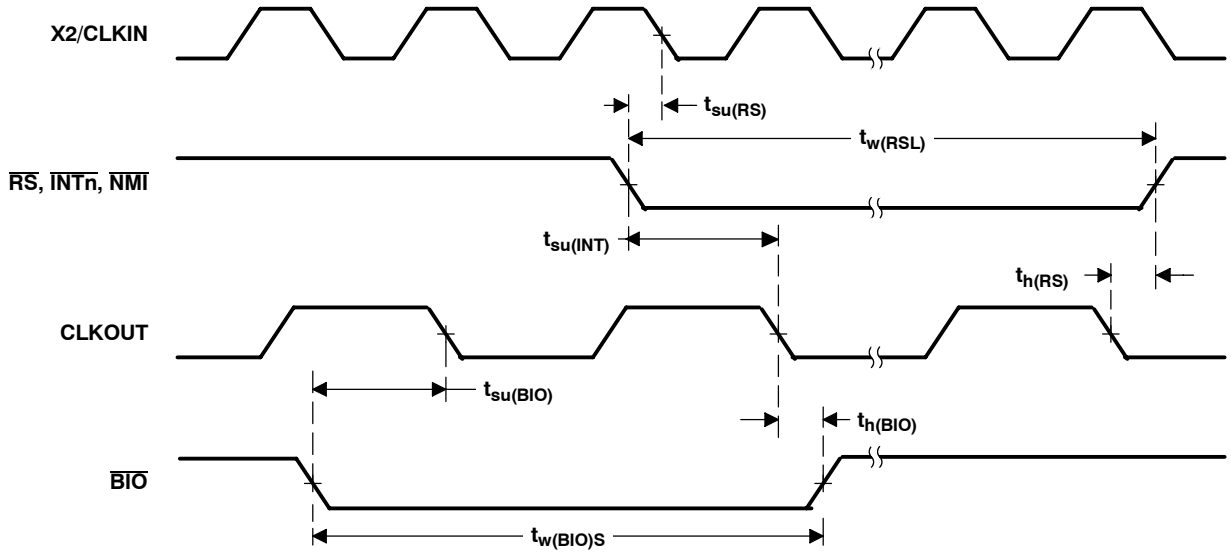


Figure 15. Reset and $\overline{\text{BIO}}$ Timings

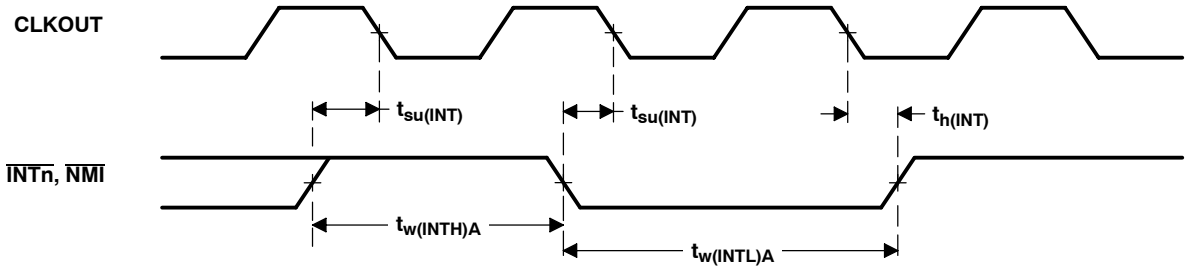


Figure 16. Interrupt Timing

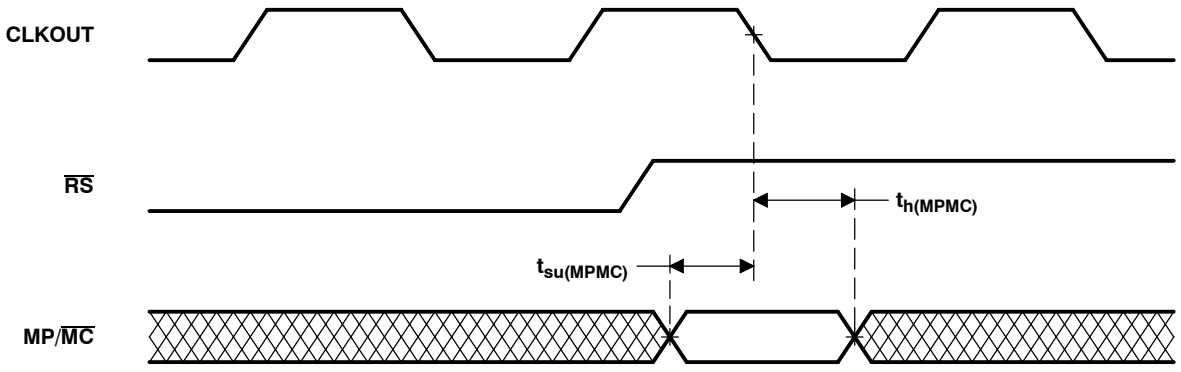


Figure 17. MP/$\overline{\text{MC}}$ Timing

instruction acquisition ($\overline{IAQ}$), interrupt acknowledge ($\overline{IACK}$), external flag (XF), and TOUT timings

switching characteristics over recommended operating conditions for $\overline{IAQ}$ and $\overline{IACK}$ [H = 0.5 $t_{c(CO)}$] (see Figure 18)

PARAMETER		549-60		UNIT
		MIN	MAX	
$t_{d(CLKL-IAQL)}$	Delay time, $\overline{IAQ}$ low from CLKOUT low	–1*	5	ns
$t_{d(CLKL-IAQH)}$	Delay time, $\overline{IAQ}$ high from CLKOUT low	–1*	5	ns
$t_{d(A)IAQ}$	Delay time, address valid before $\overline{IAQ}$ low		4*	ns
$t_{d(CLKL-IACKL)}$	Delay time, $\overline{IACK}$ low from CLKOUT low	–0.5*	7	ns
$t_{d(CLKL-IACKH)}$	Delay time , $\overline{IACK}$ high from CLKOUT low	–0.5*	7	ns
$t_{d(A)IACK}$	Delay time, address valid before $\overline{IACK}$ low		5*	ns
$t_{h(A)IAQ}$	Hold time, address valid after $\overline{IAQ}$ high	–3*		ns
$t_{h(A)IACK}$	Hold time, address valid after $\overline{IACK}$ high	–5*		ns
$t_{w(IAQL)}$	Pulse duration, $\overline{IAQ}$ low	2H–3*		ns
$t_{w(IACKL)}$	Pulse duration, $\overline{IACK}$ low	2H–3*		ns

*Not production tested.

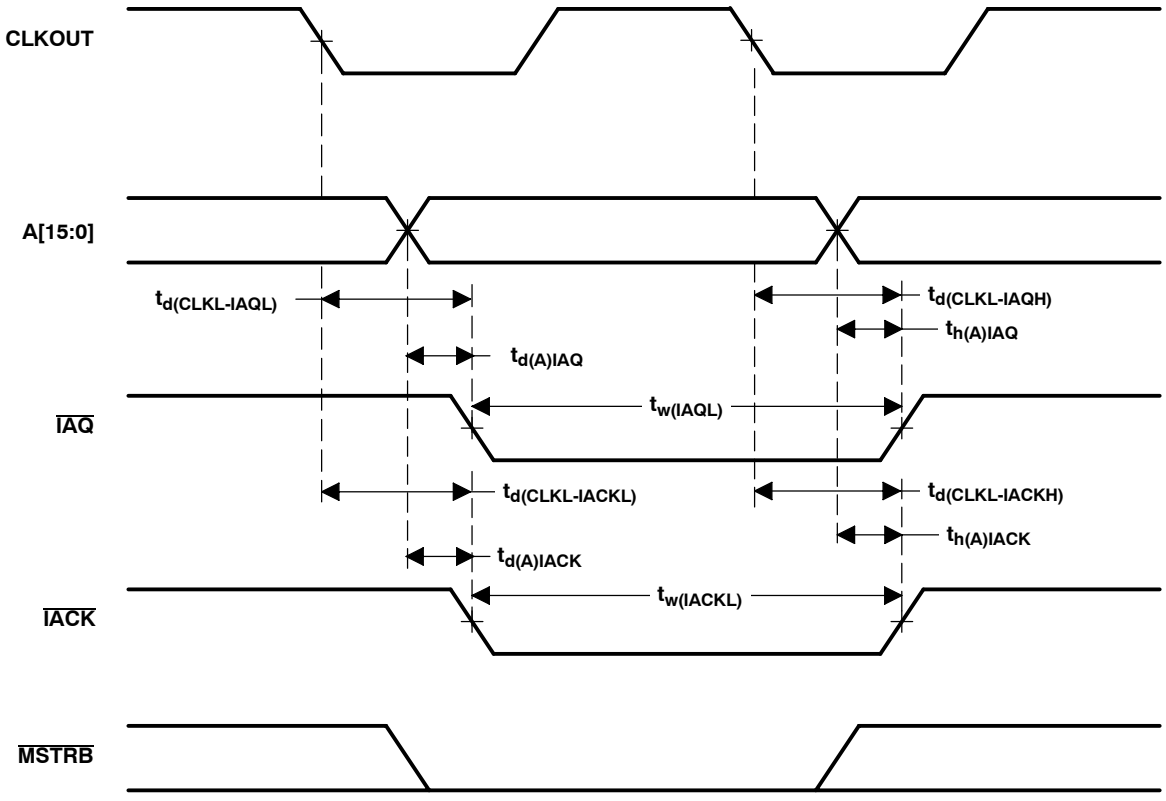


Figure 18. Instruction Acquisition ($\overline{IAQ}$) and Interrupt Acknowledge ($\overline{IACK}$) Timing

instruction acquisition ($\overline{IAQ}$), interrupt acknowledge ($\overline{IACK}$), external flag (XF), and TOUT timings (continued)

switching characteristics over recommended operating conditions for external flag (XF) and TOUT [H = 0.5 $t_{c(CO)}$] (see Figure 19 and Figure 20)

PARAMETER		549-60		UNIT
		MIN	MAX	
$t_{d(XF)}$	Delay time, XF high after CLKOUT low	–1*	6	ns
	Delay time, XF low after CLKOUT low	–1*	6	
$t_{d(TOUTH)}$	Delay time, TOUT high after CLKOUT low	–1*	6	ns
$t_{d(TOUTL)}$	Delay time, TOUT low after CLKOUT low	–1*	5	ns
$t_{w(TOUT)}$	Pulse duration, TOUT	2H–3*		ns

*Not production tested.

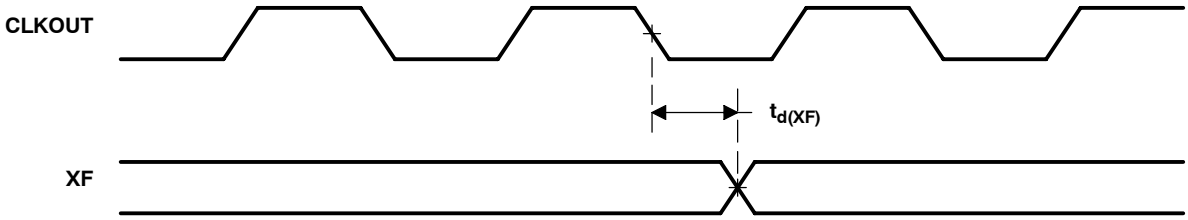


Figure 19. External Flag (XF) Timing

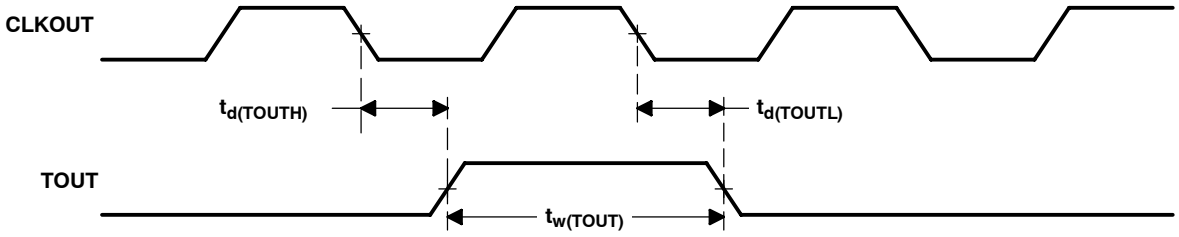


Figure 20. TOUT Timing

serial port receive timing

timing requirements for serial port receive [H = 0.5 $t_{c(CO)}$] (see Figure 21)

		549-60		UNIT
		MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial port clock	6H*	†	ns
$t_{f(SCK)}$	Fall time, serial port clock		6*	ns
$t_{r(SCK)}$	Rise time, serial port clock		6*	ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high	3H*		ns
$t_{su(FSR)}$	Setup time, TFSR/TADD before TCLKR falling edge	6		ns
$t_{h(FSR)}$	Hold time, TFSR/TADD after TCLKR falling edge	6*		ns
$t_{h(DR)}$	Hold time, TDR after TCLKR falling edge	6		ns
$t_{su(DR)}$	Setup time, TDR before TCLKR falling edge	6		ns

*Not production tested.
† The serial port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching ∞.

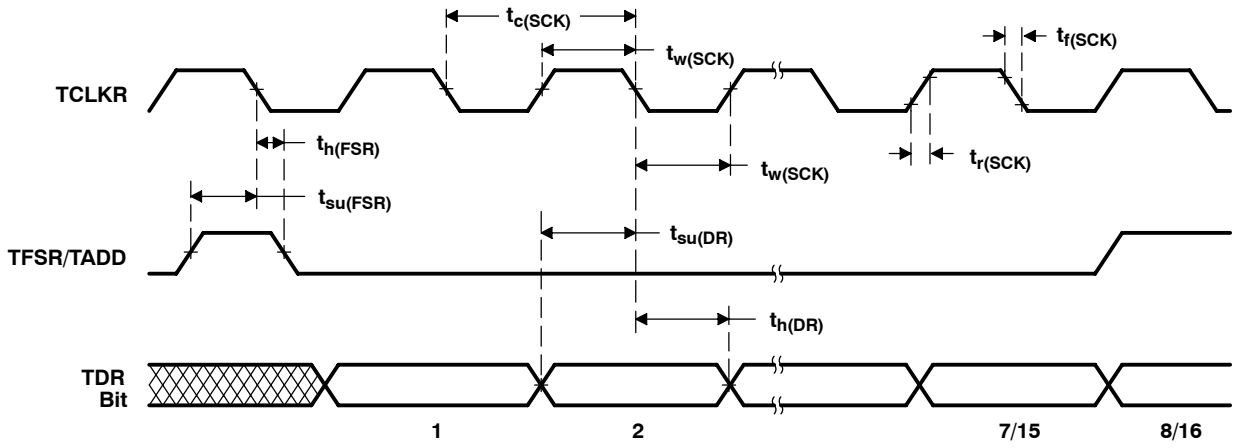


Figure 21. Serial Port Receive Timing

serial port transmit timing

switching characteristics over recommended operating conditions for serial port transmit with external clocks and frames (see Figure 22)

PARAMETER		549-60		UNIT
		MIN	MAX	
$t_{d(DX)}$	Delay time, TDX valid after TCLKX rising		25	ns
$t_{h(DX)}$	Hold time, TDX valid after TCLKX rising	-5*		ns
$t_{dis(DX)}$	Disable time, TDX after TCLKX rising		40*	ns

*Not production tested.

timing requirements for serial port transmit with external clocks and frames [H = $0.5t_{c(CO)}$] (see Figure 22)

		549-60		UNIT
		MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial port clock	6H*	†	ns
$t_{d(FSX)}$	Delay time, TFSX/TFRM after TCLKX rising edge		2H-5	ns
$t_{h(FSX)}$	Hold time, TFSX/TFRM after TCLKX falling edge (see Note 1)	6*		ns
$t_{h(FSX)H}$	Hold time, TFSX/TFRM after TCLKX rising edge (see Note 1)		2H-5*‡	ns
$t_{f(SCK)}$	Fall time, serial port clock		6*	ns
$t_{r(SCK)}$	Rise time, serial port clock		6*	ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high	3H*		ns

*Not production tested.

† The serial port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching ∞.

‡ If the TFSX/TFRM pulse does not meet this specification, the first bit of serial data is driven on TDX until the falling edge of TFSX/TFRM. After the falling edge of TFSX/TFRM, data is shifted out on TDX pin. The transmit buffer-empty interrupt is generated when the $t_{h(FSX)}$ and $t_{h(FSX)H}$ specification is met.

NOTE 1: Internal clock with external TFSX/TFRM and vice versa are also allowable. However, TFSX/TFRM timings to TCLKX always are defined depending on the source of TFSX/TFRM, and CLKX timings always are dependent upon the source of CLKX. Specifically, the relationship of TFSX/TFRM to TCLKX is independent of the source of TCLKX.

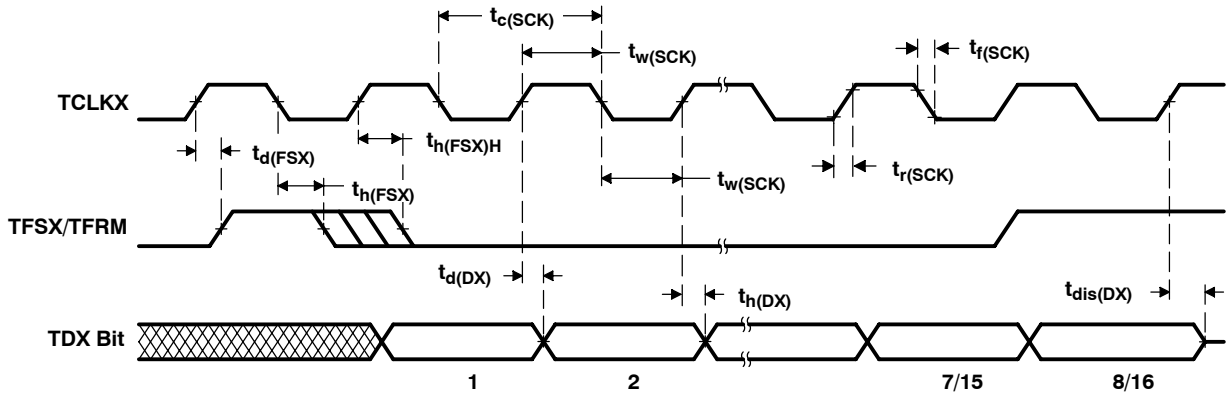


Figure 22. Serial Port Transmit Timing With External Clocks and Frames

serial port transmit timing (continued)

switching characteristics over recommended operating conditions for serial port transmit with internal clocks and frames [H = 0.5$t_{c(CO)}$] (see Figure 23)

PARAMETER		549-60			UNIT
		MIN	TYP	MAX	
$t_{c(SCK)}$	Cycle time, serial port clock		8H		ns
$t_{d(FSX)}$	Delay time, TCLKX rising to TFSX/TFRM			15	ns
$t_{d(DX)}$	Delay time, TCLKX rising to TDX			15	ns
$t_{dis(DX)}$	Disable time, TCLKX rising to TDX			20*	ns
$t_{h(DX)}$	Hold time, TDX valid after TCLKX rising edge	– 5*			ns
$t_{f(SCK)}$	Fall time, serial port clock		4		ns
$t_{r(SCK)}$	Rise time, serial port clock		4		ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high	4H–8*			ns

*Not production tested.

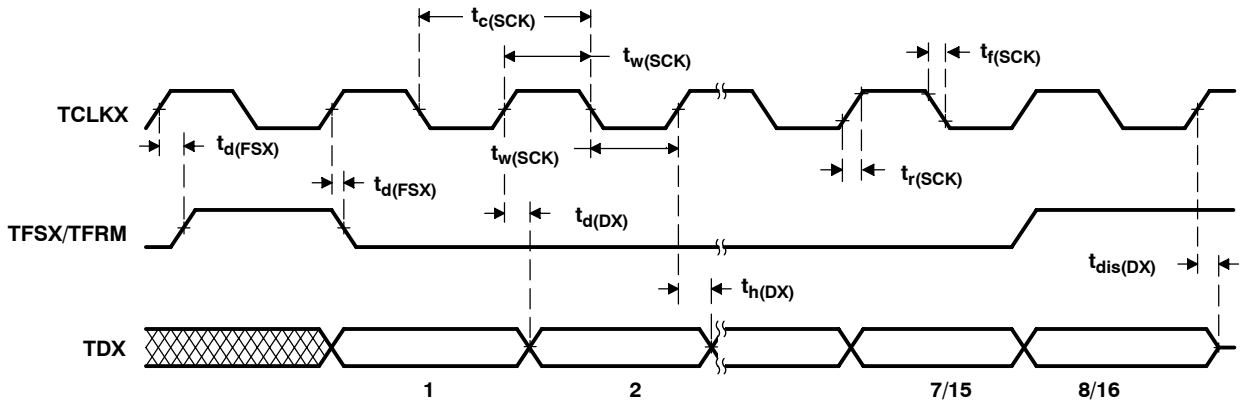


Figure 23. Serial Port Transmit Timing With Internal Clocks and Frames

buffered serial port receive timing

timing requirements (see Figure 24)

		549-60		UNIT
		MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial port clock	20*	†	ns
$t_{f(SCK)}$	Fall time, serial port clock		4*	ns
$t_{r(SCK)}$	Rise time, serial port clock		4*	ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high	6*		ns
$t_{su(BFSR)}$	Setup time, BFSR before BCLKR falling edge (see Note 2)	2		ns
$t_{h(BFSR)}$	Hold time, BFSR after BCLKR falling edge (see Note 2)	7*	$t_{c(SCK)}-2$*‡	ns
$t_{su(BDR)}$	Setup time, BDR before BCLKR falling edge	0.5*		ns
$t_{h(BDR)}$	Hold time, BDR after BCLKR falling edge	7*		ns

*Not production tested.
† The serial port design is fully static and therefore can operate with $t_{c(SCK)}$ approaching infinity.
‡ First bit is read when BFSR is sampled low by BCLKR clock.
NOTE 2: Timings for BCLKR and BFSR are given with polarity bits (BCLKP and BFSP) set to 0.

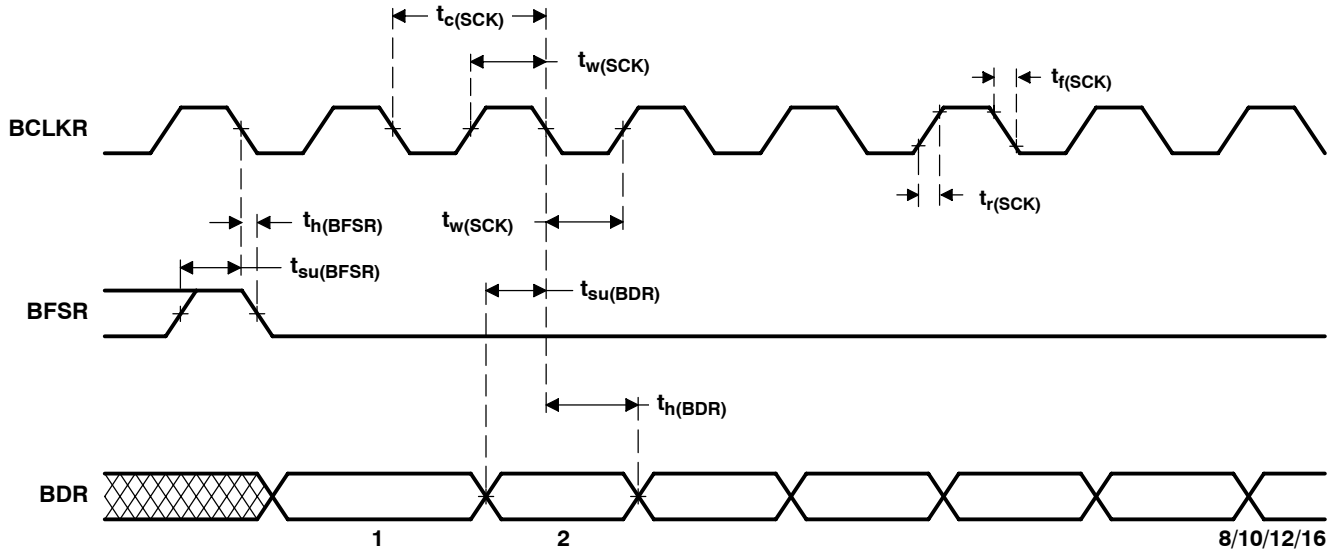


Figure 24. Buffered Serial Port Receive Timing

buffered serial port transmit timing of external frames

switching characteristics over recommended operating conditions (see Figure 25)

PARAMETER		549-60		UNIT
		MIN	MAX	
$t_{d(BDX)}$	Delay time, BDX valid after BCLKX rising		18*	ns
$t_{dis(BDX)}$	Disable time, BDX after BCLKX rising	4*	6*	ns
$t_{dis(BDX)pcm}$	Disable time, PCM mode, BDX after BCLKX rising		6*	ns
$t_{en(BDX)pcm}$	Enable time, PCM mode, BDX after BCLKX rising	8*		ns
$t_{h(BDX)}$	Hold time, BDX valid after BCLKX rising	2*		ns

*Not production tested.

timing requirements (see Figure 25)

		549-60		UNIT
		MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial port clock	20*	†	ns
$t_{f(SCK)}$	Fall time, serial port clock		4*	ns
$t_{r(SCK)}$	Rise time, serial port clock		4*	ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high	6*		ns
$t_{h(BFSX)}$	Hold time, BFSX after BCLKX falling edge (see Notes 3 and 4)	6*	$t_{c(SCK)}$ – 6*‡	ns
$t_{su(BFSX)}$	Setup time, BFSX before BCLKX falling edge (see Notes 3 and 4)	6*		ns

*Not production tested.
† The serial port design is fully static and therefore can operate with $t_{c(SCK)}$ approaching infinity.
‡ If BFSX does not meet this specification, the first bit of the serial data is driven on BDX until BFSX goes low (sampled on falling edge of BCLKX). After falling edge of the BFSX, data is shifted out on the BDX pin.

NOTES: 3. Internal clock with external BFSX and vice versa are also allowable. However, BFSX timings to BCLKX always are defined depending on the source of BFSX, and BCLKX timings always are dependent upon the source of BCLKX.
4. Timings for BCLKX and BFSX are given with polarity bits (BCLKP and BFSP) set to 0.

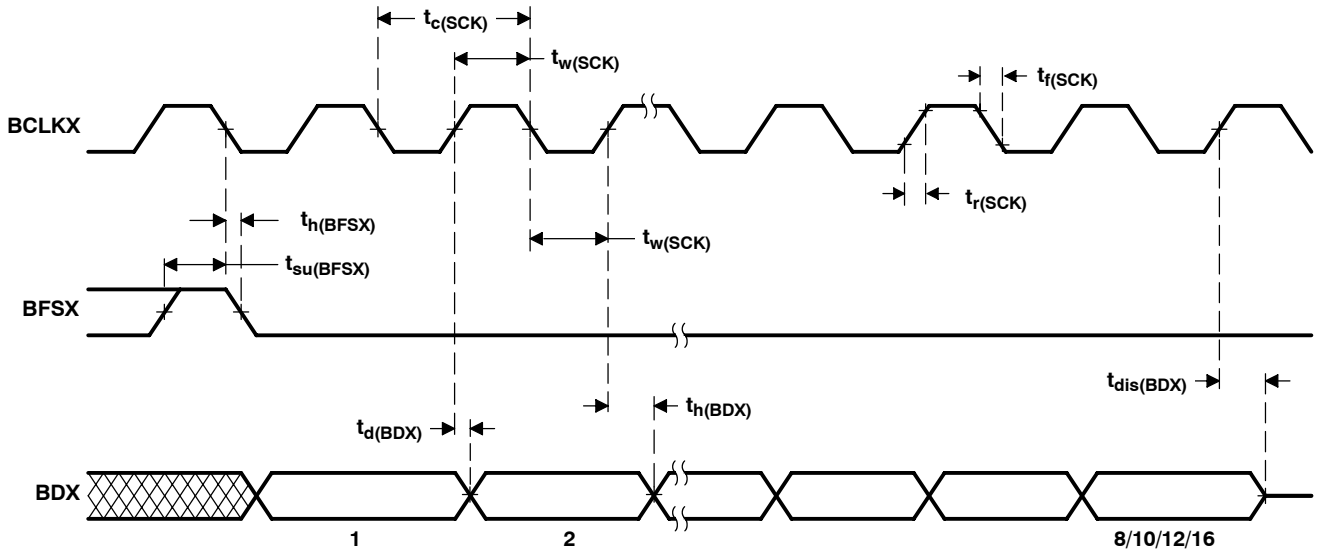


Figure 25. Buffered Serial Port Transmit Timing of External Clocks and External Frames

buffered serial port transmit timing of internal frame and internal clock

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 26)

PARAMETER		549-60		UNIT
		MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial port clock, internal clock		62H*	ns
$t_{d(BFSX)}$	Delay time, BFSX after BCLKX rising edge (see Notes 3 and 4)	0*	10*	ns
$t_{d(BDX)}$	Delay time, BDX valid after BCLKX rising edge		11*	ns
$t_{dis(BDX)}$	Disable time, BDX after BCLKX rising edge	0*	5*	ns
$t_{dis(BDX)pcm}$	Disable time, PCM mode, BDX after BCLKX rising edge		5*	ns
$t_{en(BDX)pcm}$	Enable time, PCM mode, BDX after BCLKX rising edge	7*		ns
$t_{h(BDX)}$	Hold time, BDX valid after BCLKX rising edge	-3*		ns
$t_{f(SCK)}$	Fall time, serial port clock		3.5*	ns
$t_{r(SCK)}$	Rise time, serial port clock		3.5*	ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high	6*		ns

*Not production tested.

NOTES: 3. Internal clock with external BFSX and vice versa are also allowable. However, BFSX timings to BCLKX always are defined depending on the source of BFSX, and BCLKX timings always are dependent upon the source of BCLKX.
4. Timings for BCLKX and BFSX are given with polarity bits (BCLKP and BFSP) set to 0.

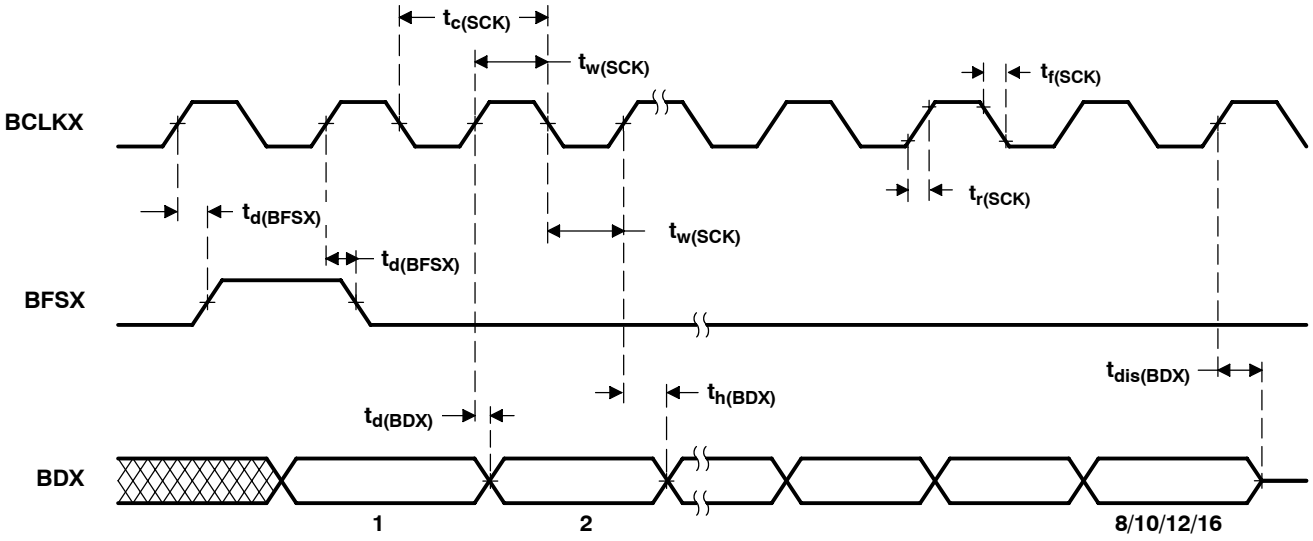


Figure 26. Buffered Serial Port Transmit Timing of Internal Clocks and Internal Frames

serial-port receive timing in TDM mode

timing requirements [H = 0.5$t_{c(CO)}$] (see Figure 27)

		549-60		UNIT
		MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial-port clock	16H*	†	ns
$t_{f(SCK)}$	Fall time, serial-port clock		6*	ns
$t_{r(SCK)}$	Rise time, serial-port clock		6*	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	8H*		ns
$t_{su(TD-TCH)}$	Setup time, TDR/TADD before TCLK rising edge	10*		ns
$t_{h(TCH-TD)}$	Hold time, TDR/TADD after TCLK rising edge	2*		ns
$t_{su(TF-TCH)}$	Setup time, TFRM before TCLK rising edge‡	10*		ns
$t_{h(TCH-TF)}$	Hold time, TFRM after TCLK rising edge‡	10*		ns

*Not production tested.
† The serial-port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching infinity.
‡ TFRM timing and waveforms shown in Figure 27 are for external TFRM. TFRM can also be configured as internal. The TFRM internal case is illustrated in the transmit timing diagram in Figure 28.

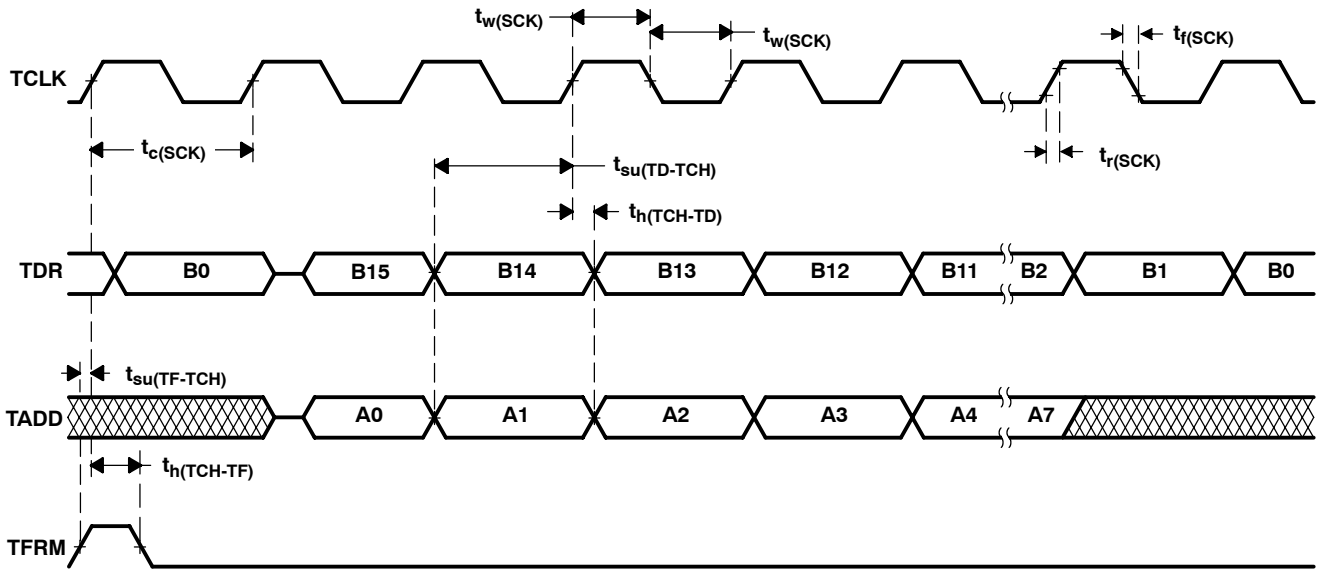


Figure 27. Serial-Port Receive Timing in TDM Mode

serial-port transmit timing in TDM mode

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 28)

PARAMETER		549-60 MIN	549-60 MAX	UNIT
$t_{h(TCH-TDV)}$	Hold time, TDX/TADD valid after TCLK rising edge, TCLK external	-3.5*		ns
$t_{h(TCH-TDV)}$	Hold time, TDX/TADD valid after TCLK rising edge, TCLK internal	0.5*		ns
$t_{d(TCH-TFV)}$	Delay time, TFRM valid after TCLK rising edge TCLK ext†	H – 3*	3H + 22*	ns
	Delay time, TFRM valid after TCLK rising edge, TCLK int†	H – 3*	3H + 12*	
$t_{d(TC-TDV)}$	Delay time, TCLK to valid TDX/TADD, TCLK ext		25*	ns
	Delay time, TCLK to valid TDX/TADD, TCLK int		18*	

*Not production tested.
† TFRM timing and waveforms shown in Figure 28 are for internal TFRM. TFRM can also be configured as external. The TFRM external case is illustrated in the receive timing diagram in Figure 27.

timing requirements [H = 0.5$t_{c(CO)}$] (see Figure 28)

		549-60 MIN	549-60 MAX	UNIT
$t_{c(SCK)}$	Cycle time, serial-port clock	16H*‡	§	ns
$t_{f(SCK)}$	Fall time, serial-port clock		6*	ns
$t_{r(SCK)}$	Rise time, serial-port clock		6*	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	8H*‡		ns

*Not production tested.
‡ When SCK is generated internally, this value is typical.
§ The serial-port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching ∞.

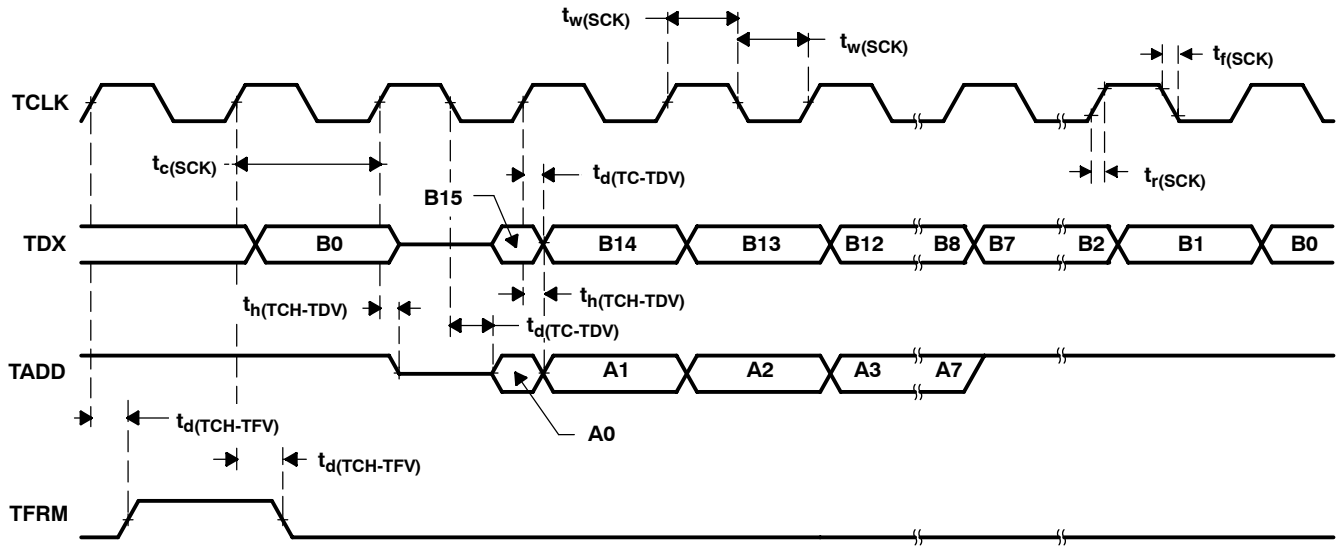


Figure 28. Serial-Port Transmit Timing in TDM Mode

host-port interface timing

switching characteristics over recommended operating conditions [H = $0.5t_{c(CO)}$] (see Notes 5 and 6) (see Figure 29 through Figure 32)

PARAMETER			549-60 MIN	549-60 MAX	UNIT
$t_{d(DSL-HDV)}$	Delay time, $\overline{DS}$ low to HD driven		5*	12*	ns
$t_{d(HEL-HDV1)}$	Delay time, HDS falling to HD valid for first byte of a non-subsequent read: → max 20 ns†‡	Case 1: Shared-access mode if $t_{w(DSH)}$ < 7H		7H+20–$t_{w(DSH)}$*	ns
		Case 2: Shared-access mode if $t_{w(DSH)}$ > 7H		20*	
		Case 3: Host-only mode if $t_{w(DSH)}$ < 20 ns		40–$t_{w(DSH)}$*	
		Case 4: Host-only mode if $t_{w(DSH)}$ > 20 ns		20*	
$t_{d(DSL-HDV2)}$	Delay time, $\overline{DS}$ low to HD valid, second byte		5*‡	20*	ns
$t_{d(DSH-HYH)}$	Delay time, $\overline{DS}$ high to HRDY high			10H+10*	ns
$t_{su(HDV-HYH)}$	Setup time, HD valid before HRDY rising edge		3H–10*		ns
$t_{h(DSH-HDV)R}$	Hold time, HD valid after $\overline{DS}$ rising edge, read		0*	14	ns
$t_{d(COH-HYH)}$	Delay time, CLKOUT rising edge to HRDY high			10*	ns
$t_{d(DSH-HYL)}$	Delay time, $\overline{HDS}$ or $\overline{HCS}$ high to HRDY low			12*	ns
$t_{d(COH-HTX)}$	Delay time, CLKOUT rising edge to $\overline{HINT}$ change			15*	ns

*Not production tested.

† Host-only mode timings apply for read accesses to HPIC or HPIA, write accesses to BOB, and resetting DSPINT or HINT to 0 in shared-access mode. HRDY does not go low for these accesses.

‡ Shared-access mode timings are met automatically if HRDY is used.

NOTES: 5. SAM = shared-access mode, HOM = host-only mode
HAD stands for HCNTRL0, HCNTRL1, and HR/$\overline{W}$.
$\overline{HDS}$ refers to either $\overline{HDS1}$ or $\overline{HDS2}$.
$\overline{DS}$ refers to the logical OR of $\overline{HCS}$ and $\overline{HDS}$.

6. On host read accesses to the HPI, the setup time of HD before $\overline{DS}$ rising edge depends on the host waveforms and cannot be specified here.

host-port interface timing (continued)

timing requirements [H = 0.5$t_{c(CO)}$] (see Note 5, Figure 29 through Figure 32)

			549-60		UNIT
			MIN	MAX	
$t_{su(HBV-DSL)}$	Setup time, HAD/HBIL valid before $\overline{DS}$ or $\overline{HAS}$ falling edge		10*		ns
$t_{h(DSL-HBV)}$	Hold time, HAD/HBIL valid after $\overline{DS}$ or $\overline{HAS}$ falling edge		5*		ns
$t_{su(HSL-DSL)}$	Setup time, $\overline{HAS}$ low before $\overline{DS}$ falling edge		12*		ns
$t_{w(DSL)}$	Pulse duration, $\overline{DS}$ low		30*†		ns
$t_{w(DSH)}$	Pulse duration, $\overline{DS}$ high		10*		ns
$t_{c(DSH-DSH)}$†	Cycle time, $\overline{DS}$ rising edge to next $\overline{DS}$ rising edge	Case 1: HOM access timings (see Access Timings Without HRDY)	50*		ns
		Case 2a: SAM accesses and HOM active writes to DSPINT or HINT. (see Access Timings With HRDY)	10H*		
$t_{su(HDV-DSH)}$	Setup time, HD valid before $\overline{DS}$ rising edge		12*		ns
$t_{d(DSH-HSL)}$‡	Delay time, $\overline{DS}$ high to next $\overline{HAS}$ low		10H*		ns
$t_{h(DSH-HDV)W}$	Hold time, HD valid after $\overline{DS}$ rising edge, write		3.5*		ns

*Not production tested.

† A host not using HRDY should meet the 10H requirement all the time unless a software handshake is used to change the access rate according to the HPI mode.

‡ Must only be met if $\overline{HAS}$ is going low when not accessing the HPI (as would be the case where multiple devices are being driven by one host).

NOTE 5: SAM = shared-access mode, HOM = host-only mode
HAD stands for HCNTRL0, HCNTRL1, and HR/$\overline{W}$.
$\overline{HDS}$ refers to either $\overline{HDS1}$ or $\overline{HDS2}$.
$\overline{DS}$ refers to the logical OR of $\overline{HCS}$ and $\overline{HDS}$.

host-port interface timing (continued)

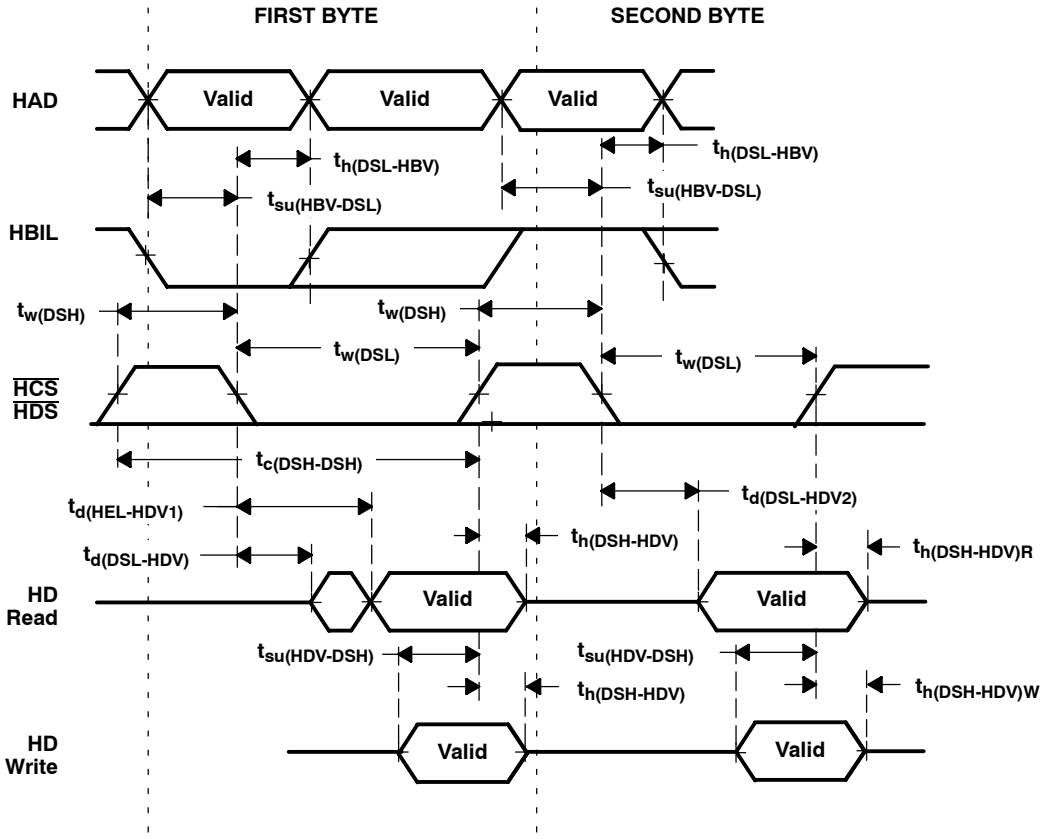
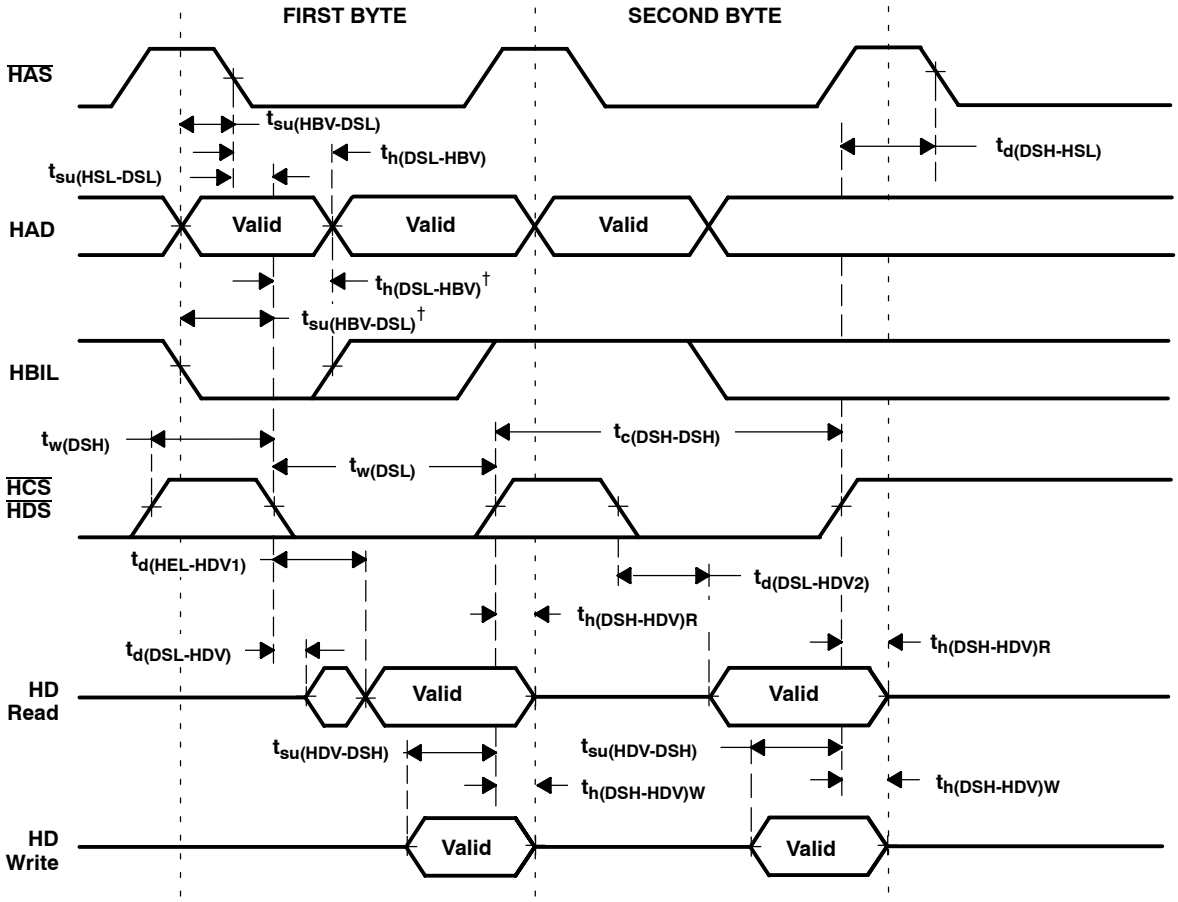


Figure 29. Read/Write Access Timings Without HRDY or $\overline{HAS}$

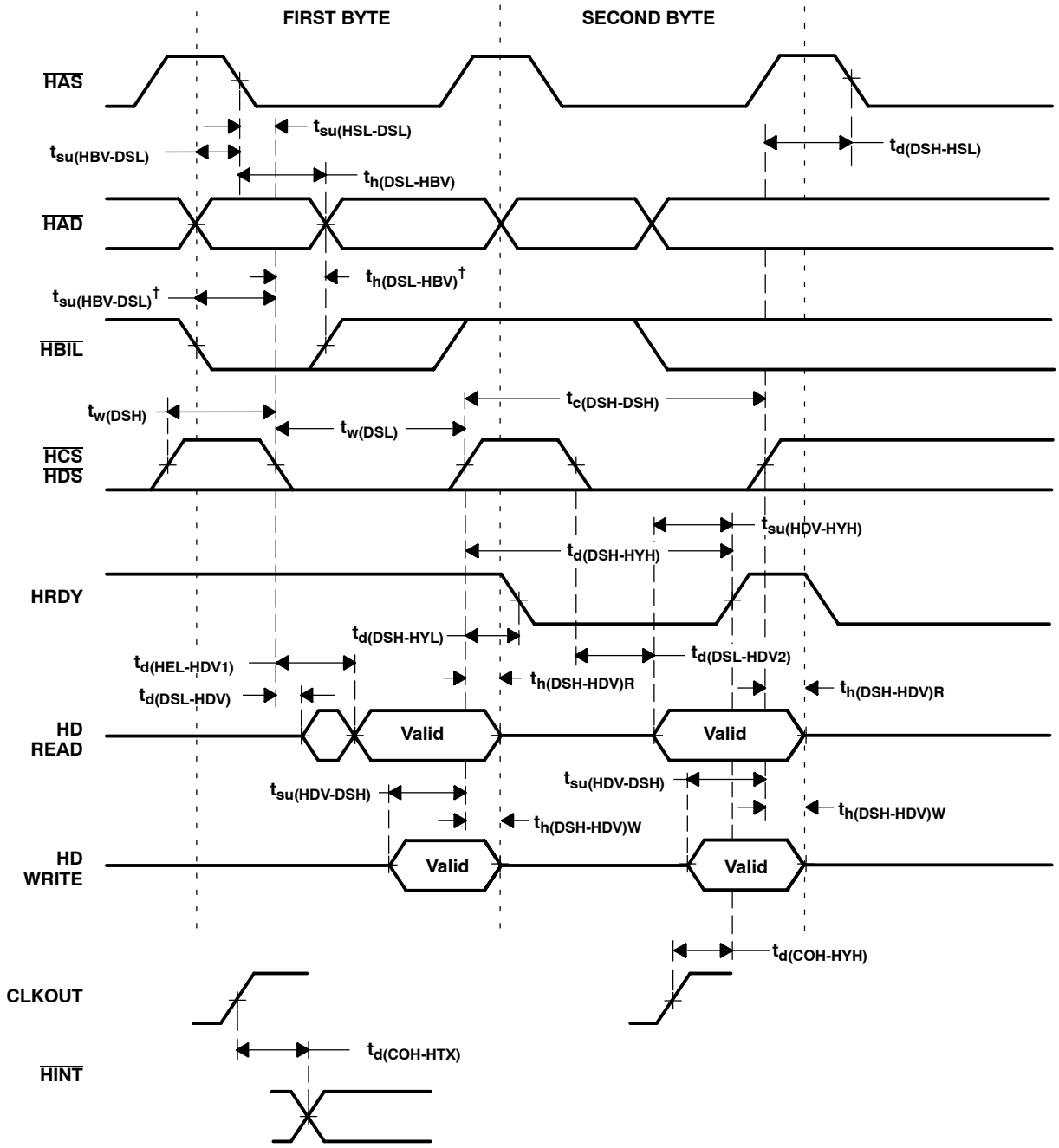
host-port interface timing (continued)



† When $\overline{\text{HAS}}$ is tied to V_{DD}

Figure 30. Read/Write Access Timings Using $\overline{\text{HAS}}$ Without HRDY

host-port interface timing (continued)



† When $\overline{\text{HAS}}$ is tied to V_{DD}

Figure 31. Read/Write Access Timing With HRDY

host-port interface timing (continued)

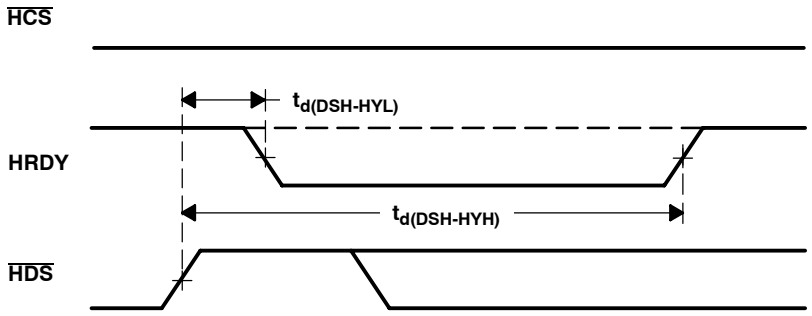


Figure 32. HRDY Signal When $\overline{\text{HCS}}$ is Always Low

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
5962-0251201QXA	NRND	CFP	HFG	164	1	TBD	Call TI	Call TI	
SMJ320LC549HFGW60	NRND	CFP	HFG	164	1	TBD	Call TI	N / A for Pkg Type	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

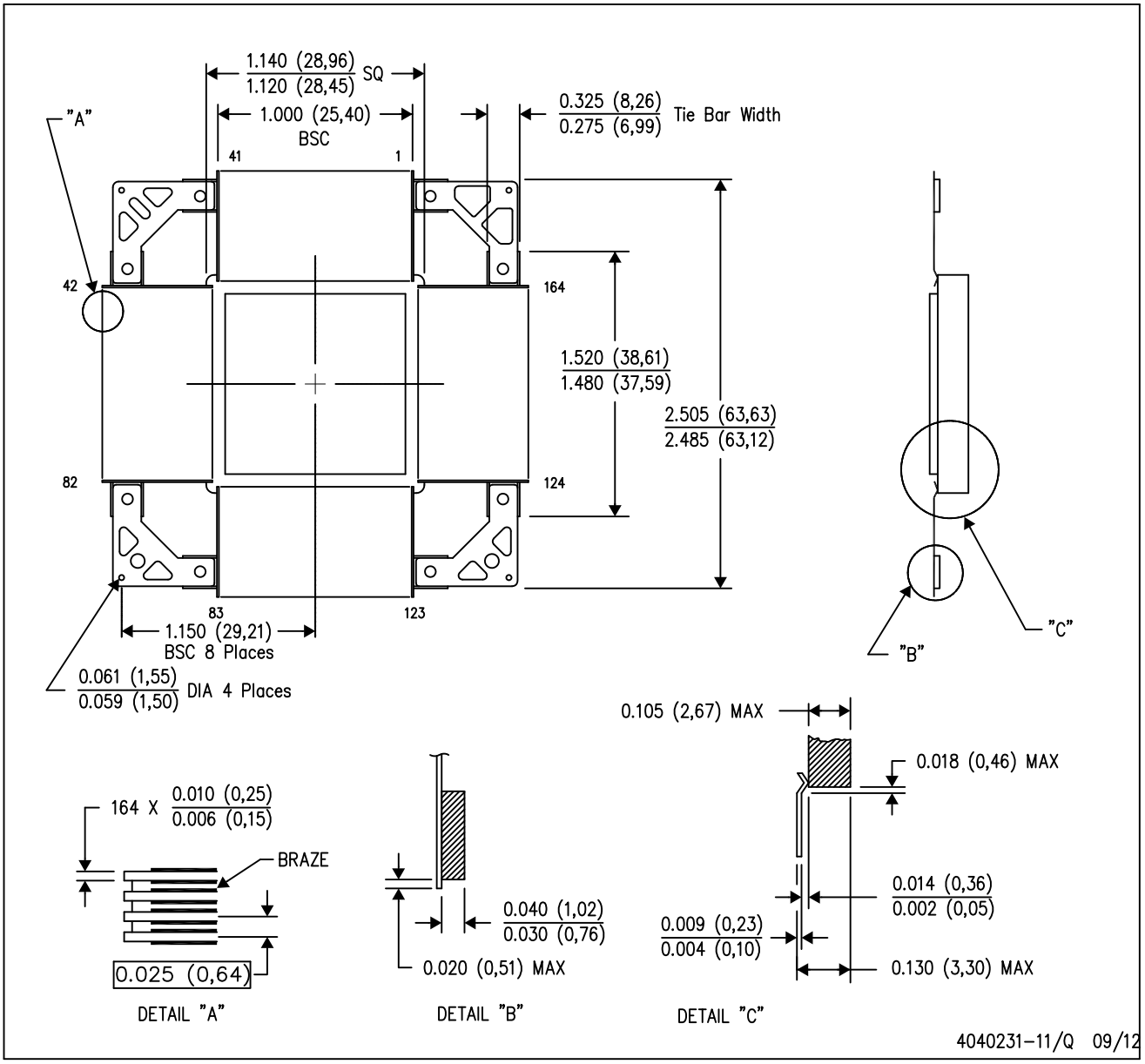
OTHER QUALIFIED VERSIONS OF SMJ320LC549 :

- Catalog: TMS320LC549

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

HFG (S–CQFP–F164) CERAMIC QUAD FLATPACK WITH NCTB



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.
G. Falls within JEDEC MO–113AA (REV D)

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