

# SN54276, SN74276 QUADRUPLE J-K FLIP-FLOPS

SDLS091

OCTOBER 1976 — REVISED MARCH 1988

- Four J-K Flip-Flops in a Single Package . . . Can Reduce FF Package Count by 50%
- Separate Negative-Edge-Triggered Clocks with Hysteresis . . . Typically 200 mV
- Typical Clock Input Frequency . . . 50 MHz
- Fully Buffered Outputs

## description

These quadruple TTL J-K flip-flops incorporate a number of third-generation IC features that can simplify system design and reduce flip-flop package count by up to 50%. They feature hysteresis at each clock input, fully buffered outputs, and direct clear capability, and are presettable through a buffer that also features an input hysteresis loop. The negative-edge-triggering clocks are directly compatible with earlier Series 54/74 single and dual pulse-triggered flip-flops. These circuits can be used to emulate D- or T-type flip-flops by hard-wiring the inputs, or to implement asynchronous sequential functions.

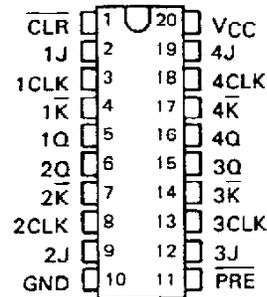
The SN54276 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ; the SN74276 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE (EACH FLIP-FLOP)

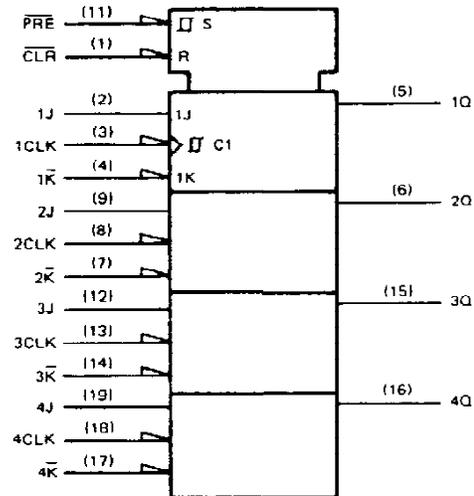
| COMMON INPUTS |     | INPUTS |   |   | OUTPUT         |
|---------------|-----|--------|---|---|----------------|
| PRE           | CLR | CLK    | J | K | Q              |
| L             | H   | X      | X | X | H              |
| H             | L   | X      | X | X | L              |
| L             | L   | X      | X | X | H <sup>†</sup> |
| H             | H   | ↓      | L | H | Q <sub>0</sub> |
| H             | H   | ↓      | H | H | H              |
| H             | H   | ↓      | L | L | L              |
| H             | H   | ↓      | H | L | TOGGLE         |
| H             | H   | H      | X | X | Q <sub>0</sub> |

<sup>†</sup> This configuration is nonstable; that is, Q may not persist when preset and clear return to their inactive (high) level.

SN54276 . . . J PACKAGE  
SN74276 . . . N PACKAGE  
(TOP VIEW)



## logic symbol<sup>‡</sup>



<sup>‡</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

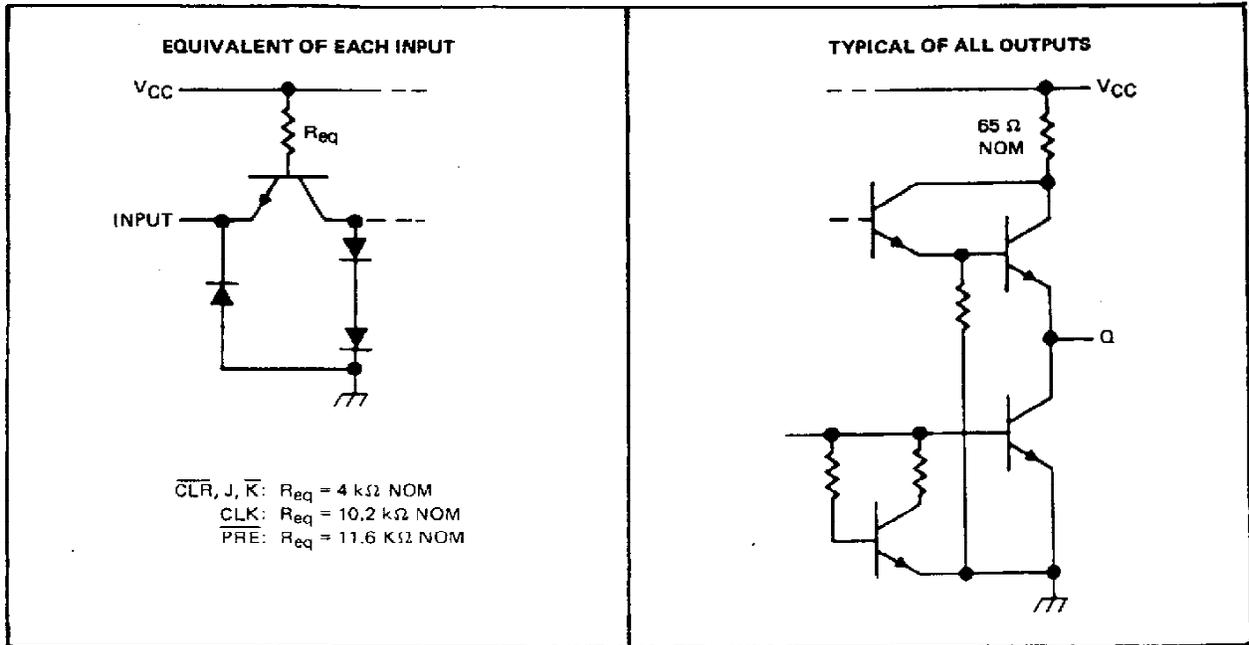
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# SN54276, SN74276 QUADRUPLE J-K FLIP-FLOPS

## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|   |                |
|---|----------------|
| Supply voltage, $V_{CC}$ (see Note 1) .....         | 7 V            |
| Input voltage .....                                 | 5.5 V          |
| Operating free-air temperature range: SN54276 ..... | -55°C to 125°C |
| SN74276 .....                                       | 0°C to 70°C    |
| Storage temperature range .....                     | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

# SN54276, SN74276 QUADRUPLE J-K FLIP-FLOPS

## recommended operating conditions

|                                       |                                 | SN54276 |     |      | SN74276 |     |      | UNIT         |
|---------------------------------------|---------------------------------|---------|-----|------|---------|-----|------|--------------|
|                                       |                                 | MIN     | NOM | MAX  | MIN     | NOM | MAX  |              |
| Supply voltage, $V_{CC}$              |                                 | 4.5     | 5   | 5.5  | 4.75    | 5   | 5.25 | V            |
| High-level output current, $I_{OH}$   |                                 |         |     | -800 |         |     | -800 | $\mu$ A      |
| Low-level output current, $I_{OL}$    |                                 |         |     | 16   |         |     | 16   | mA           |
| Clock frequency                       |                                 | 0       |     | 35   | 0       |     | 35   | MHz          |
| Pulse width, $t_W$                    | Clock high                      | 13.5    |     |      | 13.5    |     |      | ns           |
|                                       | Clock low                       | 15      |     |      | 15      |     |      |              |
|                                       | Preset or clear low             | 12      |     |      | 12      |     |      |              |
| Setup time, $t_{su}$                  | J, K inputs                     | 3↓      |     |      | 3↓      |     |      | ns           |
|                                       | Clear and preset inactive state | 10↓     |     |      | 10↓     |     |      |              |
| Input hold time, $t_h$                |                                 | 10↓     |     |      | 10↓     |     |      | ns           |
| Operating free-air temperature, $T_A$ |                                 | -55     |     | 125  | 0       |     | 70   | $^{\circ}$ C |

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER |  | TEST CONDITIONS†   | MIN | TYP‡ | MAX  | UNIT    |
|-----------|--|--|-----|------|------|---------|
| $V_{IH}$  | High-level input voltage               |  | 2   |      |      | V       |
| $V_{IL}$  | Low-level input voltage                |  |     |      | 0.8  | V       |
| $V_{IK}$  | Input clamp voltage                    | $V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$  |     |      | -1.5 | V       |
| $V_{OH}$  | High-level output voltage              | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$ | 2.4 | 3.4  |      | V       |
| $V_{OL}$  | Low-level output voltage               | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$    |     | 0.2  | 0.4  | V       |
| $I_I$     | Input current at maximum input voltage | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$   |     |      | 1    | mA      |
| $I_{IH}$  | High-level input current               | $V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$   |     |      | 40   | $\mu$ A |
| $I_{IL}$  | Low-level input current                | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$   |     |      | -1.6 | mA      |
| $I_{OS}$  | Short-circuit output current§          | $V_{CC} = \text{MAX}$  | -30 |      | -85  | mA      |
| $I_{CC}$  | Supply current                         | $V_{CC} = \text{MAX}$  |     | 60   | 81   | mA      |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ .

§ Not more than one output should be shorted at a time.

## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

| PARAMETER        |  | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|------------------|--|--|-----|-----|-----|------|
| $f_{\text{max}}$ | Maximum clock frequency                                      |  | 35  | 50  |     | MHz  |
| $t_{PLH}$        | Propagation delay time, low-to-high-level output from preset | $C_L = 15 \text{ pF}, R_L = 400 \Omega,$<br>See Note 2 |     | 15  | 25  | ns   |
| $t_{PHL}$        | Propagation delay time, high-to-low-level output from clear  |  |     | 18  | 30  | ns   |
| $t_{PLH}$        | Propagation delay time, low-to-high level output from clock  |  |     | 17  | 30  | ns   |
| $t_{PHL}$        | Propagation delay time, high-to-low level output from clock  |  |     | 20  | 30  | ns   |

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| SN74276DW        | OBSOLETE              | SOIC         | DW              | 20   |             | TBD                     | Call TI              | Call TI                      | Samples Not Available       |
| SN74276DWR       | OBSOLETE              | SOIC         | DW              | 20   |             | TBD                     | Call TI              | Call TI                      | Samples Not Available       |
| SN74276DWR       | OBSOLETE              | SOIC         | DW              | 20   |             | TBD                     | Call TI              | Call TI                      | Samples Not Available       |
| SN74276N         | OBSOLETE              | PDIP         | N               | 20   |             | TBD                     | Call TI              | Call TI                      | Samples Not Available       |
| SN74276N         | OBSOLETE              | PDIP         | N               | 20   |             | TBD                     | Call TI              | Call TI                      | Samples Not Available       |
| SN74276N3        | OBSOLETE              | PDIP         | N               | 20   |             | TBD                     | Call TI              | Call TI                      | Samples Not Available       |
| SN74276N3        | OBSOLETE              | PDIP         | N               | 20   |             | TBD                     | Call TI              | Call TI                      | Samples Not Available       |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

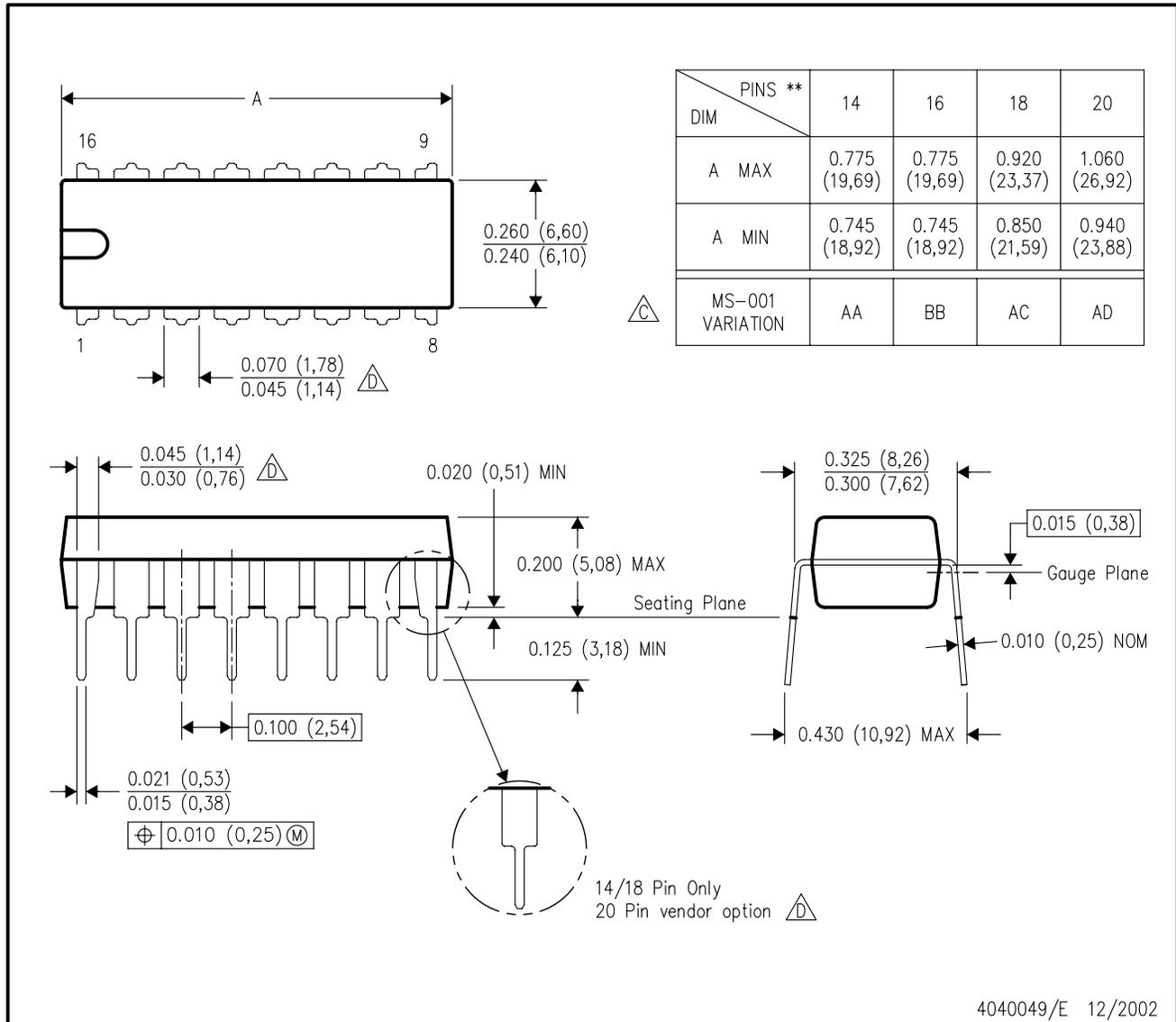
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N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

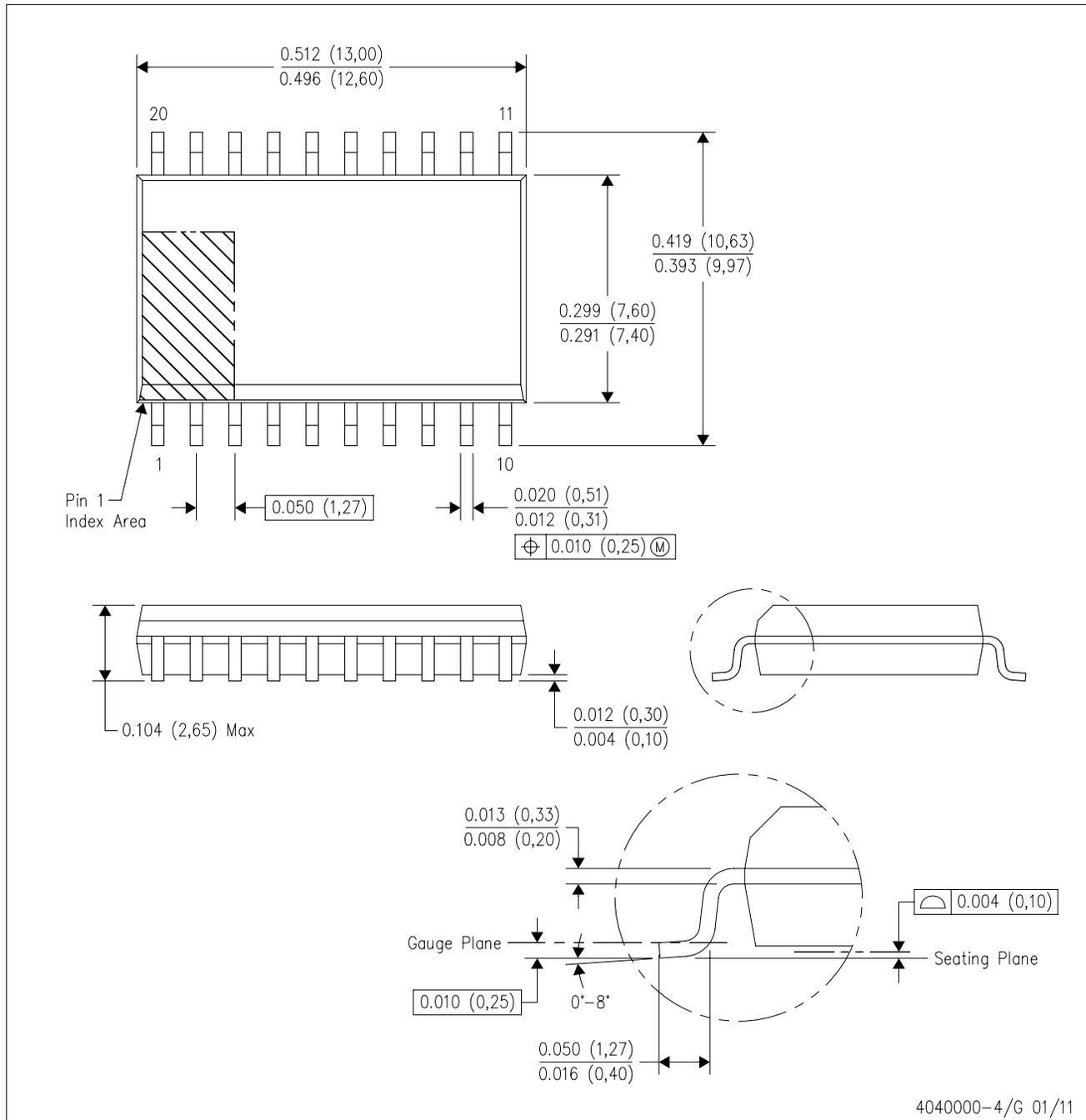
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AC.

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