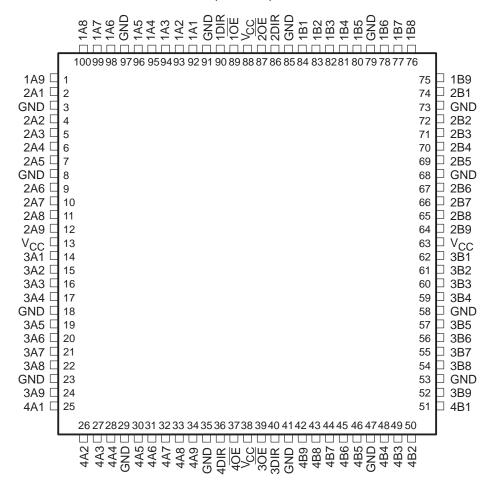
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- Members of the Texas Instruments Widebus+™ Family
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- Packaged in 100-Pin Plastic Thin Quad Flat (PZ) Package With 14 × 14-mm Body Using 0.5-mm Lead Pitch

SN74ABT32245 . . . PZ PACKAGE (TOP VIEW)



#### description

The 'ABT32245 are 36-bit (quad 9-bit) noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as four 9-bit transceivers, two18-bit transceivers, or one 36-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) inputs. The output-enable  $(\overline{OE})$  inputs can be used to disable the device so that the buses are effectively isolated.

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## SN54ABT32245, SN74ABT32245 36-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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#### description (continued)

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

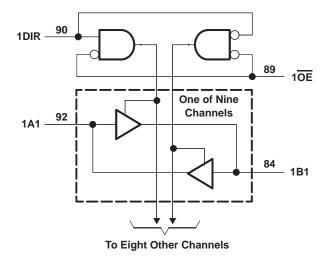
Active bus-hold circuitry holds unused or floating data inputs at a valid logic level.

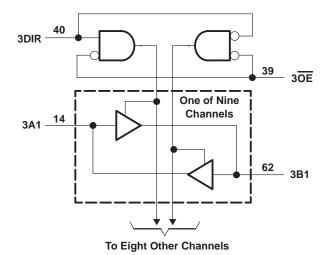
The SN54ABT32245 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to  $125^{\circ}$ C. The SN74ABT32245 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

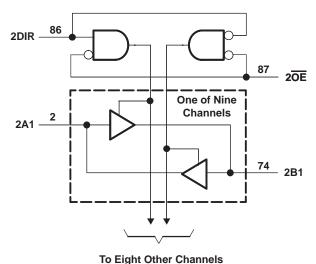
# FUNCTION TABLE (each 9-bit section)

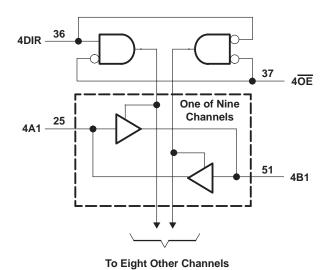
	•	,
INP	UTS	
OE	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	X	Isolation

## logic diagram (positive logic)









absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	$-0.5\;V$ to 7 $V$
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	$-0.5 \text{ V}$ to 7 V
Voltage range applied to any output in the high state or power-off state, VO	-0.5  V to $5.5  V$
Current into any output in the low state, IO: SN54ABT32245	96 mA
SN74ABT32245	128 mA
Input clamp current, $I_{ K }(V_{ I } < 0)$	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	50 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 2)	1.2 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

# SN54ABT32245, SN74ABT32245 36-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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### recommended operating conditions

				3T32245	SN74ABT32245		
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage			5.5	4.5	5.5	V
VIH	High-level input voltage			N	2		V
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage			VCC	0	VCC	V
IOH	High-level output current			-24		-32	mA
loL	Low-level output current		770	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	30	10		10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		200		200		μs/V
TA	Operating free-air temperature	_	-55	125	-40	85	°C



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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER TEST CONDITIONS		TEGT CONDITIONS		SN54ABT32245			SN74ABT32245				
			MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	UNIT		
VIK		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$		2.5			2.5			V
V		V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$		3			3			
VOH		V 45V	$I_{OH} = -24 \text{ mA}$		2						V
		V <sub>CC</sub> = 4.5 V	$I_{OH} = -32 \text{ mA}$					2			
V		\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	I <sub>OL</sub> = 48 mA		0.55		0.55		V		
VOL	$V_{CC} = 4.5 \text{ V}$		$I_{OL} = 64 \text{ mA}$						0.55		V
l <sub>i</sub>	Control inputs	$V_{CC} = 0 \text{ to } 5.5 \text{ V},$	$V_I = V_{CC}$ or $C$	SND			±1			±1	μА
·	A or B ports	$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V},$	$V_I = V_{CC}$ or $C$	GND			±20			±20	
	A or B ports	V 45V	V <sub>I</sub> = 0.8 V		100		100			4	
<sup>I</sup> I(hold)		V <sub>CC</sub> = 4.5 V	V <sub>I</sub> = 2 V		-100	Š	<b>Y</b> ,	-100			μΑ
lozpu‡		$\frac{\text{V}_{CC}}{\text{OE}} = 0 \text{ to } 2.1 \text{ V},$	$V_0 = 0.5 \text{ V to}$	2.7 V,		700	±50			±50	μΑ
I <sub>OZPD</sub> ‡		$\frac{\text{V}_{CC}}{\text{OE}} = 2.1 \text{ V to 0},$	$V_0 = 0.5 \text{ V to}$	2.7 V,	-	270	±50			±50	μΑ
IOZH§		$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V},$	V <sub>O</sub> = 2.7 V,	OE ≥ 2 V	Q.		10			10	μΑ
I <sub>OZL</sub> §		$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V},$	V <sub>O</sub> = 0.5 V,	OE ≥ 2 V			-10			-10	μΑ
loff		$V_{CC} = 0$ ,	$V_I$ or $V_O \le 4.5$	5 V			±100			±100	μΑ
ICEX		$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 5.5 V	Outputs high			50			50	μΑ
IO¶		$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.5 \text{ V}$		-50	-100	-180	-50	-100	-180	mA
lcc		V <sub>CC</sub> = 5.5 V,	Outputs high Outputs low Outputs disabled				3			3	
		$I_{O} = 0$ ,			20				20	mA	
		$V_I = V_{CC}$ or GND					2			2	
ΔICC#		$V_{CC} = 5.5 \text{ V},$ Other inputs at $V_{CC}$ or	One input at 3.4 V, or GND				1			1	mA
Ci	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V				3.5			3.5		pF
Cio	A or B ports	V <sub>O</sub> = 2.5 V or 0.5 V			9.5			9.5		pF	

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>&</sup>lt;sup>‡</sup> This parameter is specified by characterization.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup>This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

# SN54ABT32245, SN74ABT32245 36-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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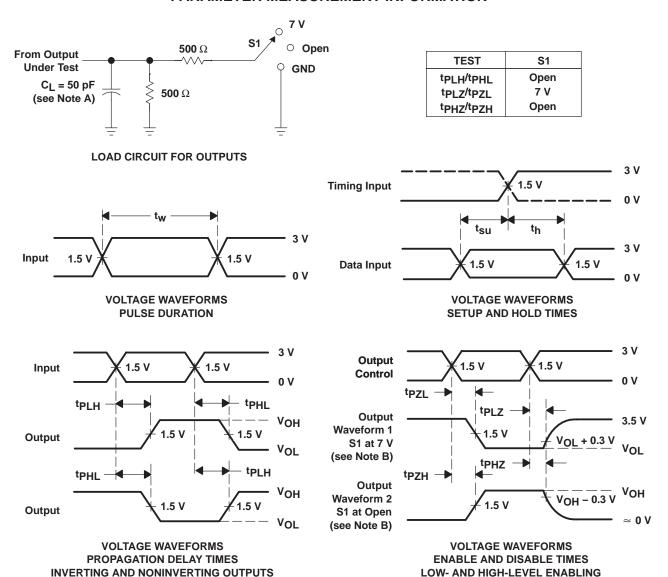
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54AI	3T32245	SN74ABT32245		UNIT
	(INPUT)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<sup>t</sup> PLH	A or B	B or A	1.7	3.2	4.4	1.7	5.3	1.7	5	
<sup>t</sup> PHL			1.7	3.3	4.6	1.7	5.3	1.7	5.2	ns
<sup>t</sup> PZH	ŌĒ	D on A	1.6	4.2	6.1	1.6	7.6	1.6	7.3	
t <sub>PZL</sub>		B or A	2.7	5.2	7	2.7	8.2	2.7	8.1	ns
<sup>t</sup> PHZ	ŌĒ	B or A	1.3	3.9	6.1	1.3	6.7	1.3	6.5	ns
t <sub>PLZ</sub>		BULA	2	4.4	6.6	2 2	7.2	2	6.9	115



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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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