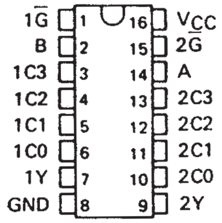
SN54LS253, SN54S253, SN74LS253, SN74S253
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

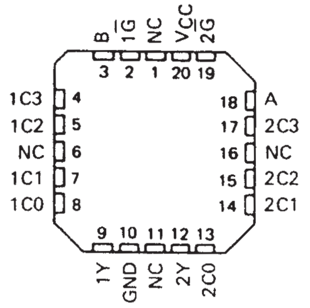
SDLS147 − SEPTEMBER 1972 − REVISED MARCH 1988

- **Three-State Version of SN54/74LS153, SN54/74S153**
- **Schottky-Diode-Clamped Transistors**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to Serial Conversion**
- **Fully Compatible with Most TTL Circuits**
- **Low Power Dissipation**
  'LS253 . . . 35 mW Typical
  'S253 . . . 225 mW Typical

SN54LS253, SN54S253 . . . J OR W PACKAGE
SN74LS253, SN74S253 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS253, SN54S253 . . . FK PACKAGE
(TOP VIEW)



NC-No internal connection

description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

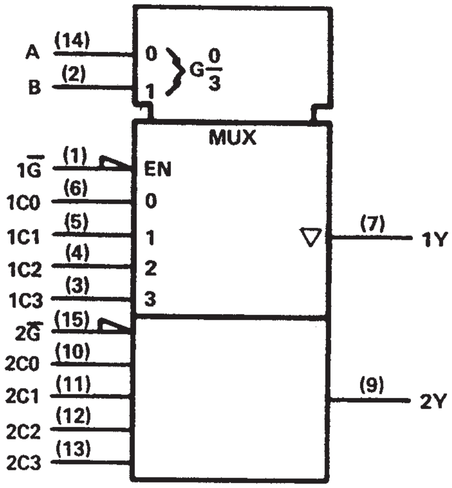
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage:	'LS253	7 V
	'S253	5.5 V
Off-state output voltage		5.5 V
Operating free-air temperature range:	SN54LS253, SN54S253	− 55°C to 125°C
	SN74LS253, SN74S253	0°C to 70°C
Storage temperature range		− 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

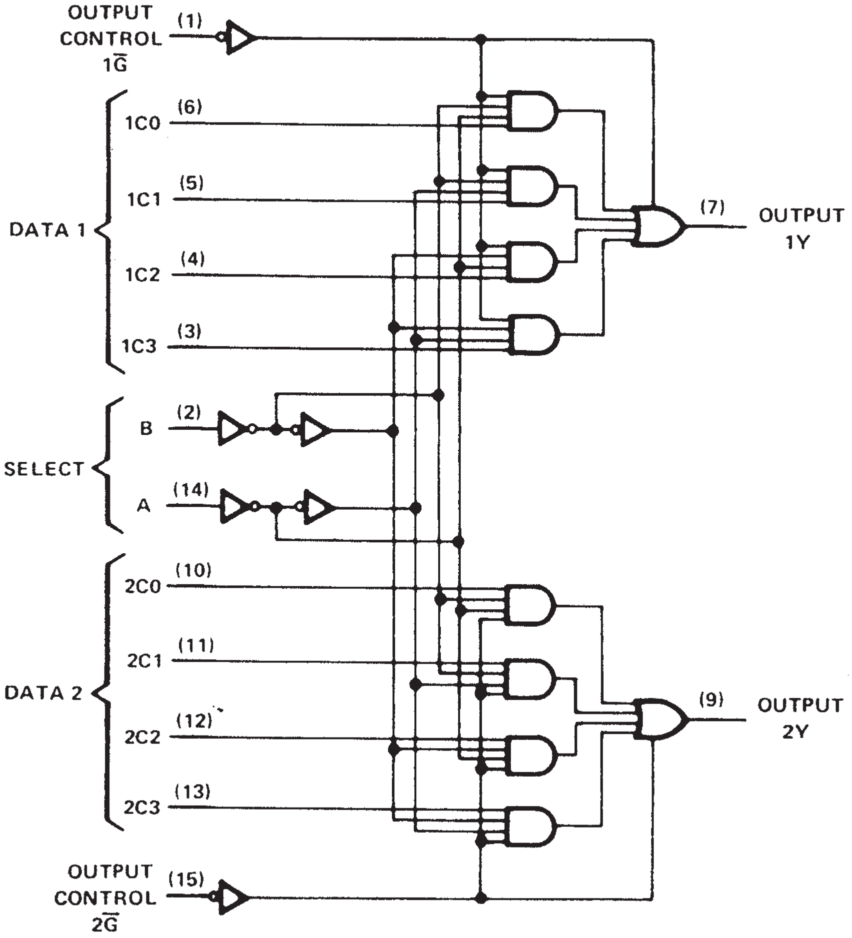
TEXAS INSTRUMENTS

logic symbol†



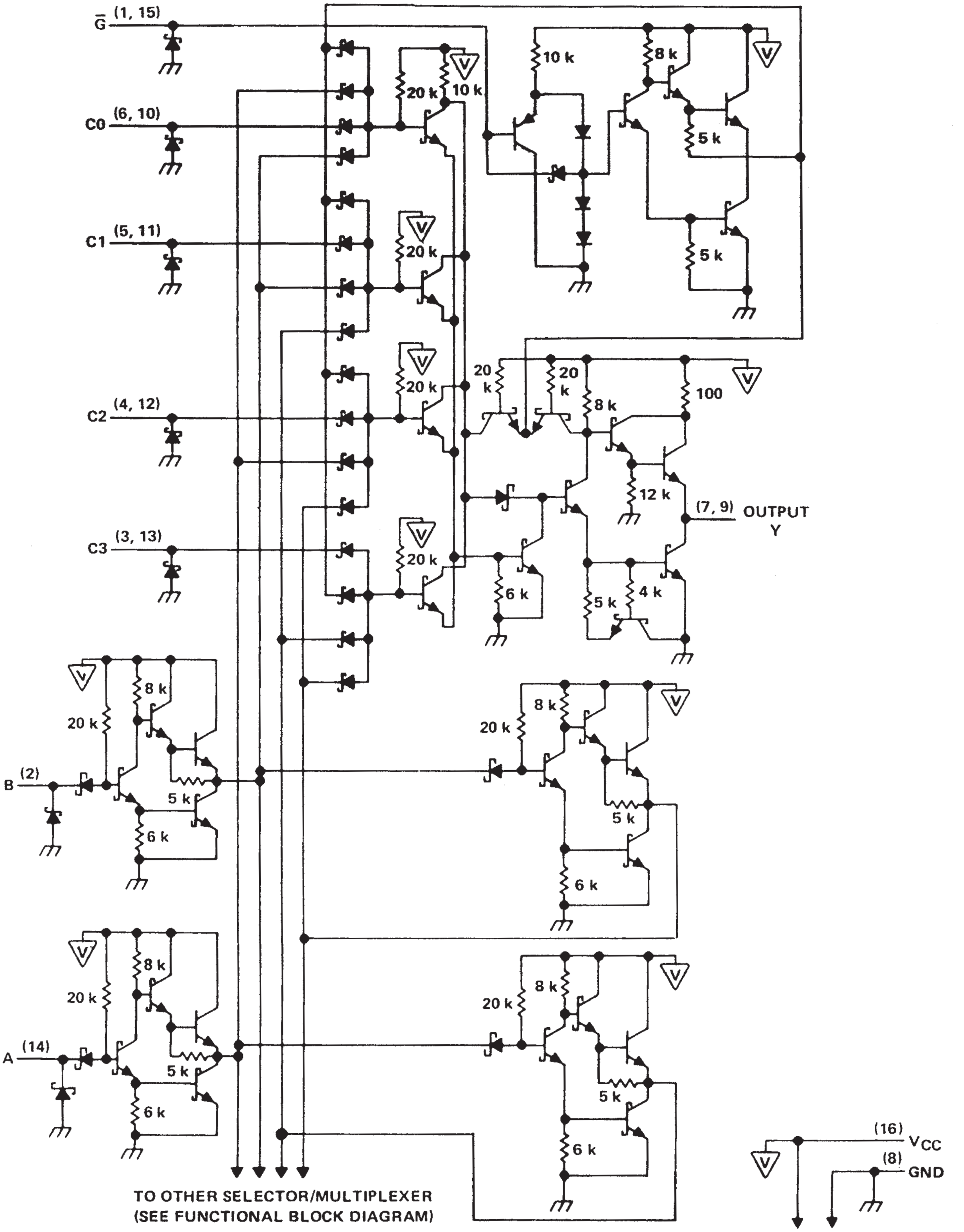
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

schematic (each selector/multiplexer, and the common select section)



Pin numbers shown are for D, J, N, and W packages.

recommended operating conditions

		SN54LS253			SN74LS253			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS253			SN74LS253			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX,	I_{OH} = MAX	2.4	3.4		2.4	3.1		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.25	0.5	
I_{OZ}	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.7 V			20			20	μA
		V_O = 0.4 V			−20			−20	
I_I	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V	$\overline{G}$			−0.2			−0.2	mA
		All other			−0.4			−0.4	
I_{OS}§	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	V_{CC} = MAX, See Note 2	Condition A		7	12		7	12	mA
		Condition B		8.5	14		8.5	14	

† For conditions shown as MIN or MAX, use the appropriate value spcified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration for the short-circuit should exceed one second.

NOTE 2: I_{CC} is measured with the outputs open under the following conditions:

A. All inputs grounded.

B. Output control at 4.5 V, all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L = 15 pF, R_L = 2 kΩ, See Note 3		17	25	ns
t_{PHL}					13	20	
t_{PLH}	Select	Y			30	45	ns
t_{PHL}					21	32	
t_{PZH}	Output Control	Y			15	28	ns
t_{PZL}					15	23	
t_{PHZ}	Output Control	Y	C_L = 5 pF, R_L = 2 kΩ, See Note 3		27	41	ns
t_{PLZ}					18	27	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54S253			SN74S253			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			− 2			− 6.5	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	− 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = MIN, I_I = − 18 mA				− 1.2	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	Series 54S	2.5	3.4		V
		Series 74S	2.7	3.4		
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_{OZ}	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.4 V			50	μA
		V_O = 0.5 V			− 50	
I_I	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V				50	μA
I_{IL}	V_{CC} = MAX, V_I = 0.5 V	$\overline{G}$ = 0.8 V			− 2	mA
		$\overline{G}$ = 2 V			− 0.25	
I_{OS}§	V_{CC} = MAX		− 40		− 100	mA
I_{CC}	V_{CC} = MAX, See Note 2	Condition A		45	70	mA
		Condition B		65	85	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the outputs open under the following conditions:
A. All inputs grounded.
B. Output control at 4.5 V, all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	R_L = 280 Ω, C_L = 15 pF, See Note 3		6	9	ns
t_{PHL}					6	9	
t_{PLH}	Select	Y			11.5	18	ns
t_{PHL}					12	18	
t_{PZH}	Output Control	Y			11	16.5	ns
t_{PZL}					12	18	
t_{PHZ}	Output Control	Y	R_L = 280 Ω, C_L = 5 pF, See Note 3		6.5	9.5	ns
t_{PLZ}					10	15	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
76017012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
7601701EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
7601701EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
7601701FA	NRND	CFP	W	16	1	TBD	Call TI	Call TI	
7601701FA	NRND	CFP	W	16	1	TBD	Call TI	Call TI	
JM38510/30908B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/30908B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/30908BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
JM38510/30908BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
JM38510/30908BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
JM38510/30908BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
M38510/30908B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/30908B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/30908BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
M38510/30908BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
M38510/30908BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
M38510/30908BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
SN54LS253J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN54LS253J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN74LS253D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/ Ball Finish	MSL Peak Temp [(3)]	Samples (Requires Login)
SN74LS253DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	
SN74LS253J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	
SN74LS253N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS253N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS253N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	
SN74LS253N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	
SN74LS253NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS253NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS253NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS253NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S253N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	
SN74S253N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	

PACKAGE OPTION ADDENDUM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
SNJ54LS253FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS253FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS253J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LS253J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LS253W	NRND	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LS253W	NRND	CFP	W	16	1	TBD	A42	N / A for Pkg Type	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54LS253, SN74LS253 :

- Catalog: SN74LS253

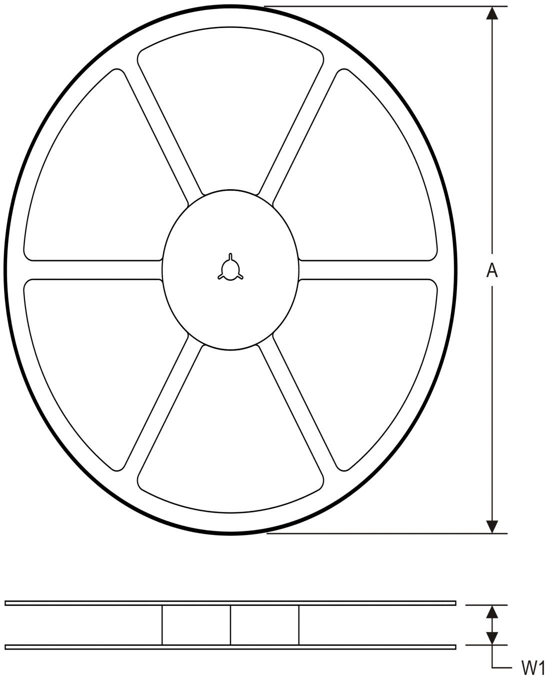
- Military: SN54LS253

NOTE: Qualified Version Definitions:

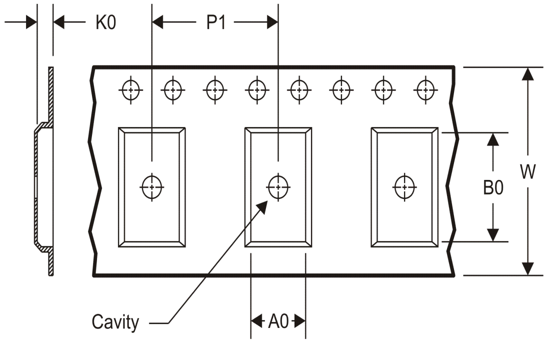
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



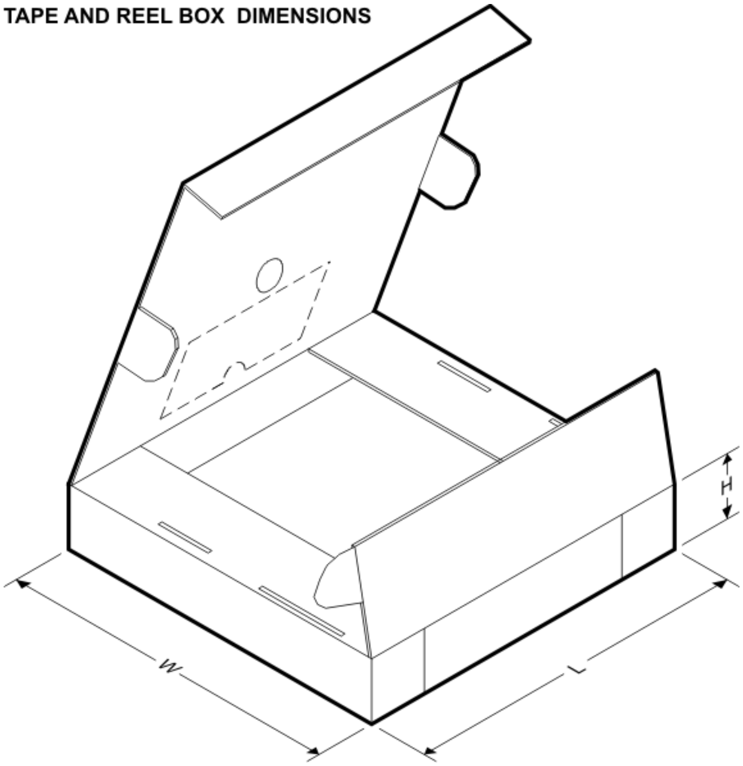
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS253DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS253NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

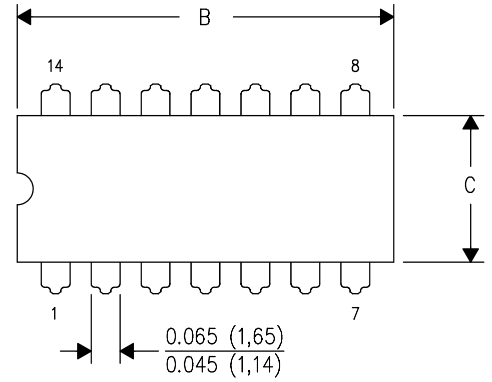


*All dimensions are nominal

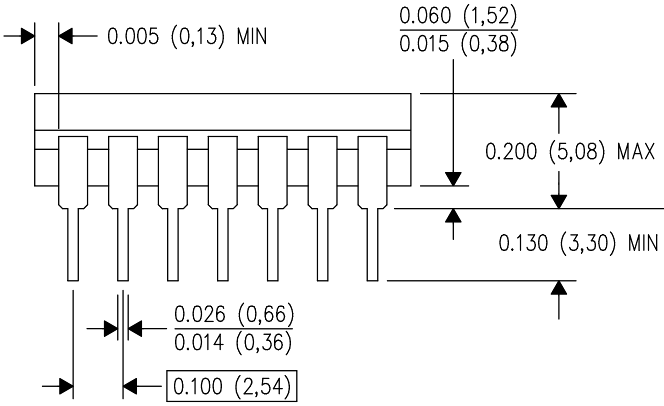
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS253DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS253NSR	SO	NS	16	2000	367.0	367.0	38.0

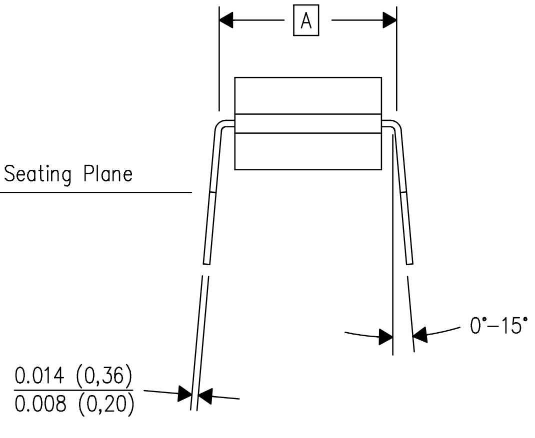
J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



PINS ** / DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)





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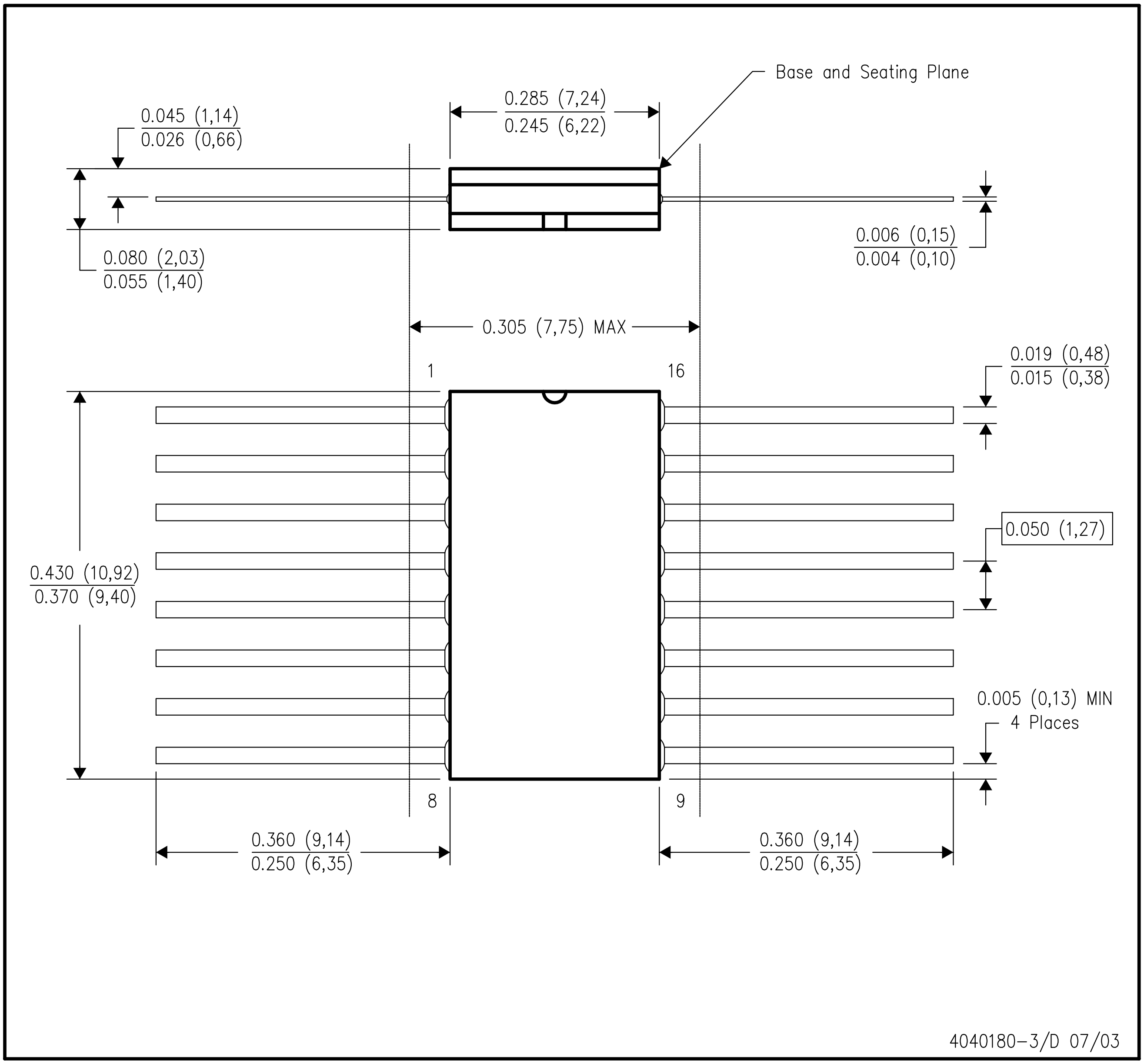
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

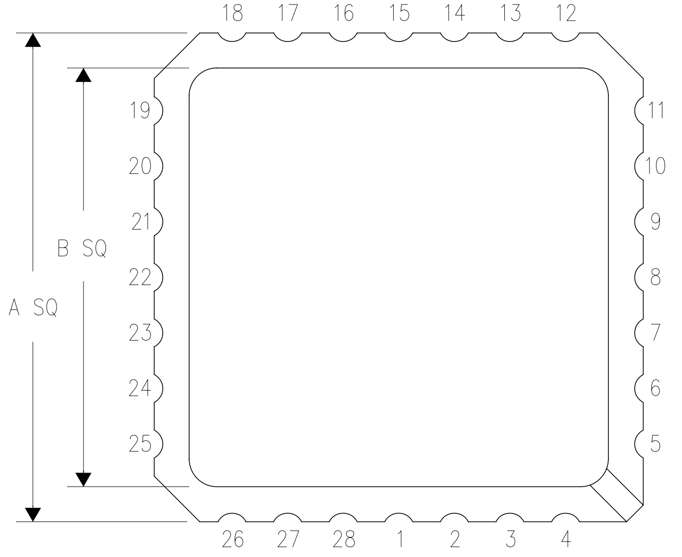
W (R–GDFP–F16) CERAMIC DUAL FLATPACK



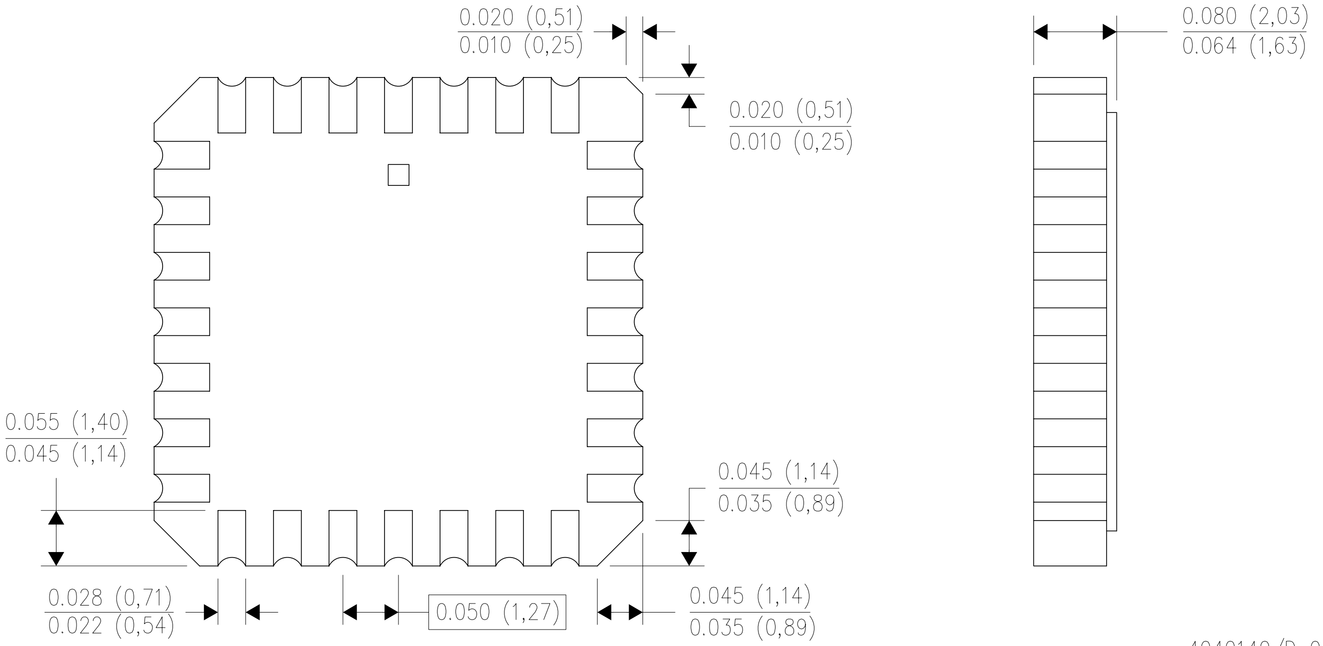
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1–F16 and JEDEC MO–092AC

FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

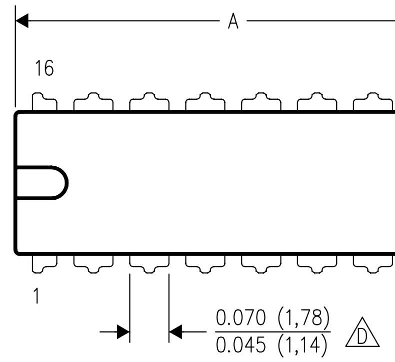


4040140/D 01/11

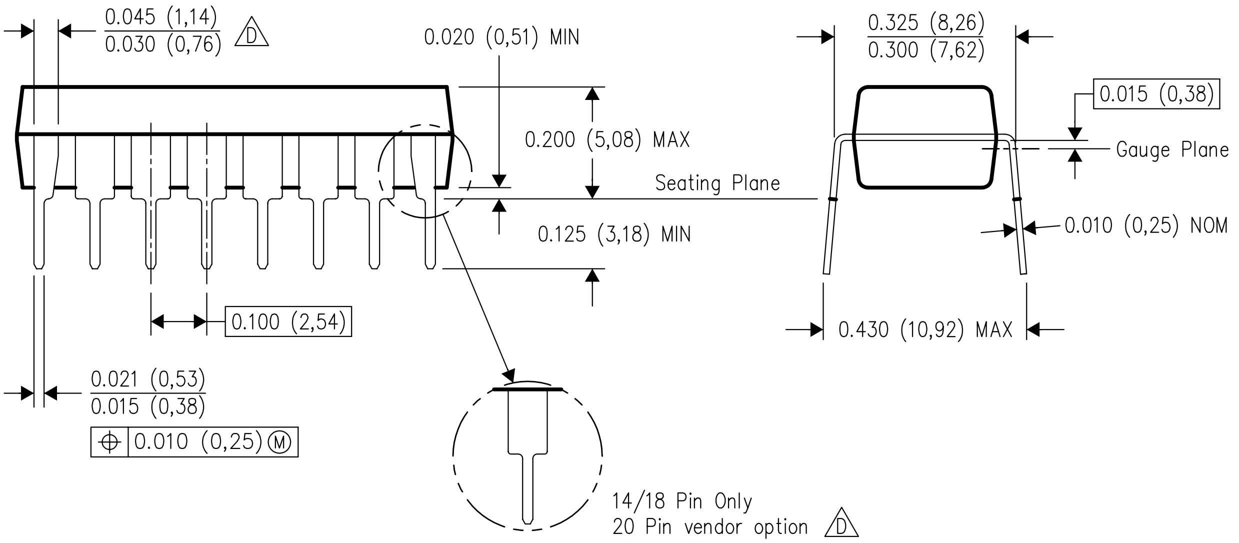
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



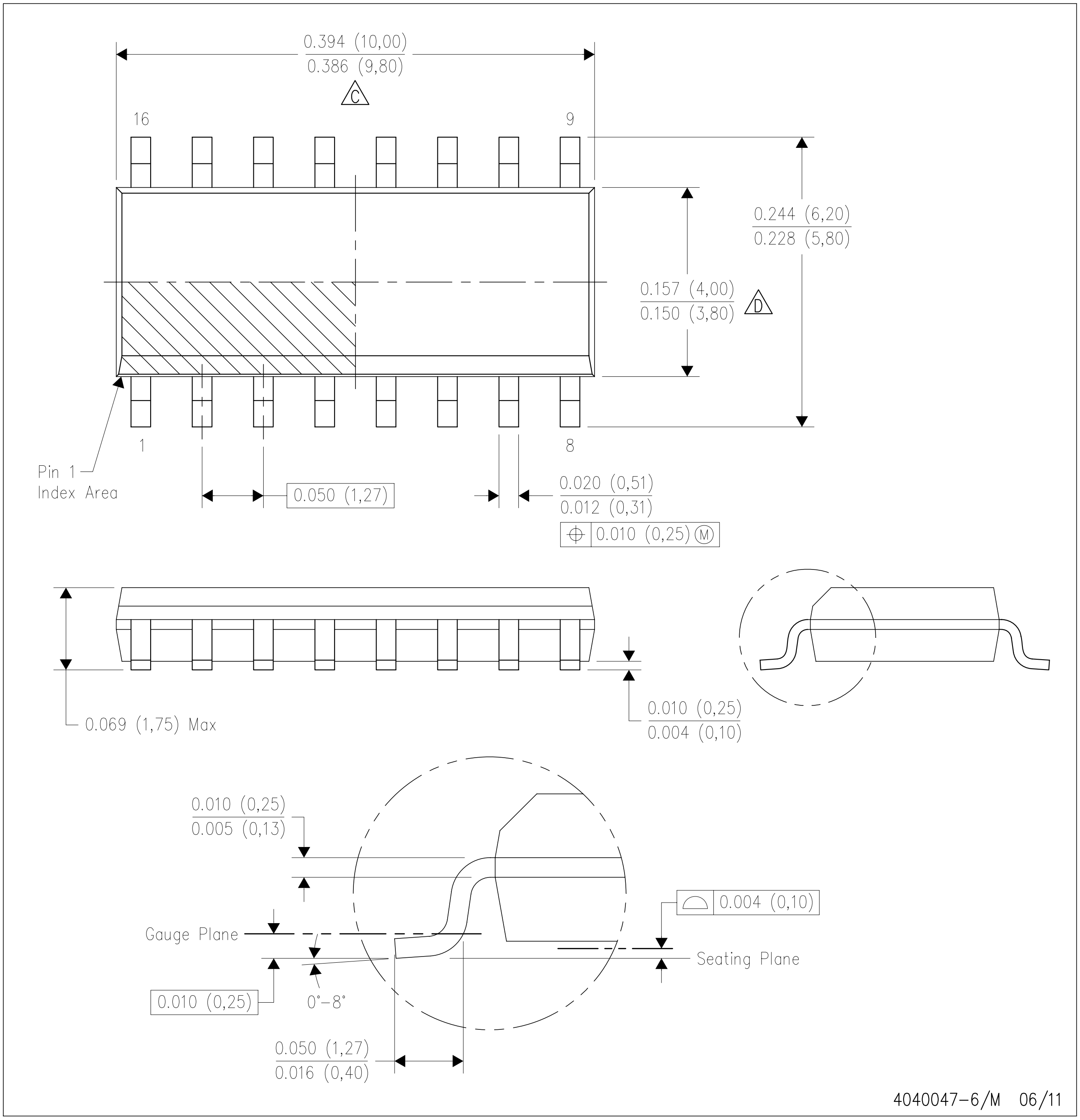
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



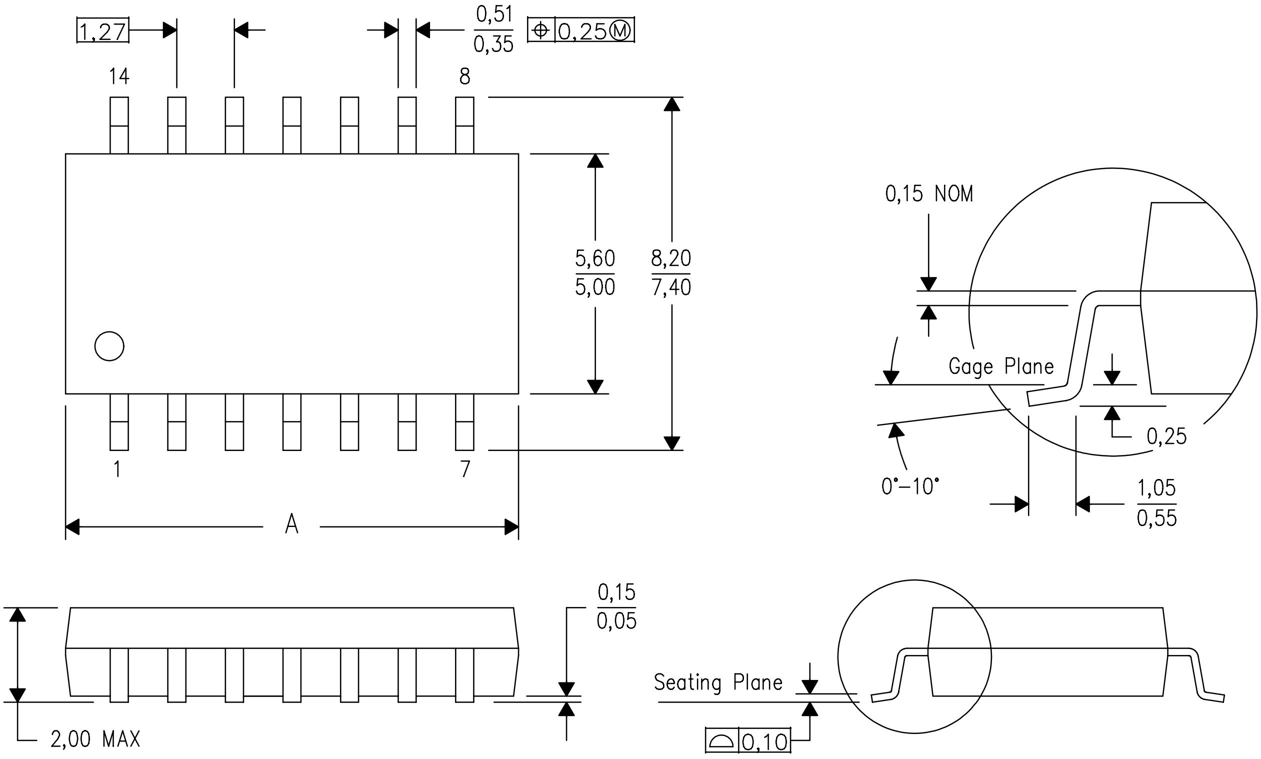
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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