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SN54LVC374A, SN74LVC374A
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS
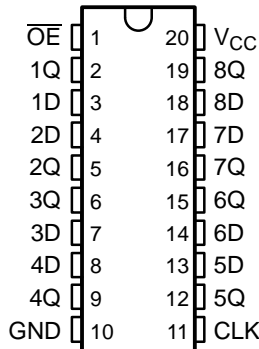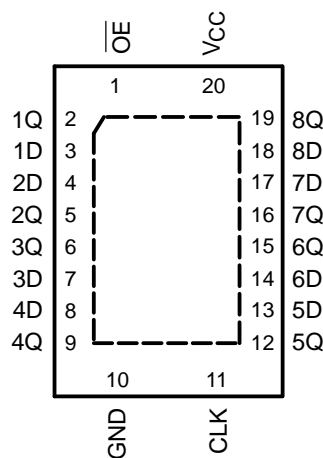SCAS296N−JANUARY 1993−REVISED MAY 2005

FEATURES

- **Operate From 1.65 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 6.5 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**

- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
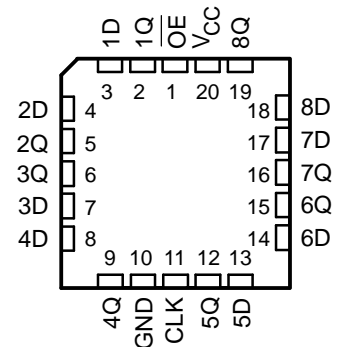 - **1000-V Charged-Device Model (C101)**

SN54LVC374A . . . J OR W PACKAGE
SN74LVC374A . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)

$\overline{OE}$	1	20	V_{CC}
1Q	2	19	8Q
1D	3	18	8D
2D	4	17	7D
2Q	5	16	7Q
3Q	6	15	6Q
3D	7	14	6D
4D	8	13	5D
4Q	9	12	5Q
GND	10	11	CLK

SN74LVC374A . . . RGY PACKAGE
(TOP VIEW)

1Q	2	19	8Q
1D	3	18	8D
2D	4	17	7D
2Q	5	16	7Q
3Q	6	15	6Q
3D	7	14	6D
4D	8	13	5D
4Q	9	12	5Q

$\overline{OE}$ (1) V_{CC} (20) GND (10) CLK (11)

SN54LVC374A . . . FK PACKAGE
(TOP VIEW)

1D(3) 1Q(2) $\overline{OE}$(1) V_{CC}(20) 8Q(19)

2D	4	18	8D
2Q	5	17	7D
3Q	6	16	7Q
3D	7	15	6Q
4D	8	14	6D

4Q(9) GND(10) CLK(11) 5Q(12) 5D(13)

DESCRIPTION/ORDERING INFORMATION

The SN54LVC374A octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC374A octal edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP – N	Tube of 20	SN74LVC374AN	SN74LVC374AN
	QFN – RGY	Reel of 1000	SN74LVC374ARGYR	LC374A
	SOIC – DW	Tube of 25	SN74LVC374ADW	LVC374A
		Reel of 2000	SN74LVC374ADWR	
	SOP – NS	Reel of 2000	SN74LVC374ANSR	LVC374A
	SSOP – DB	Reel of 2000	SN74LVC374ADBR	LC374A
	TSSOP – PW	Tube of 70	SN74LVC374APW	LC374A
		Reel of 2000	SN74LVC374APWR	
		Reel of 250	SN74LVC374APWT	
	TVSOP – DGV	Reel of 2000	SN74LVC374ADGVR	LC374A
−55°C to 125°C	CDIP – J	Tube of 20	SNJ54LVC374AJ	SNJ54LVC374AJ
	CFP – W	Tube of 85	SNJ54LVC374AW	SNJ54LVC374AW
	LCCC – FK	Tube of 55	SNJ54LVC374AFK	SNJ54LVC374AFK

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)

To Seven Other Channels
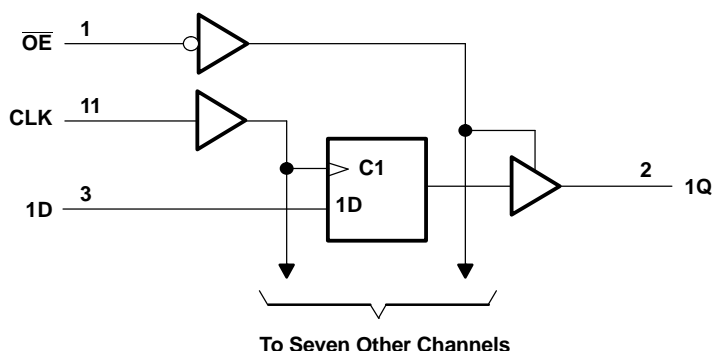
Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6.5	V
V_I	Input voltage range[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2][3]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		−50	mA
I_{OK}	Output clamp current	V_O < 0		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance	DB package[4]		70	°C/W
		DGV package[4]		92	
		DW package[4]		58	
		N package[4]		69	
		NS package[4]		60	
		PW package[4]		83	
		RGY package[5]		37	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) The package thermal impedance is calculated in accordance with JESD 51-5.

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Recommended Operating Conditions[1]

			SN54LVC374A MIN	SN54LVC374A MAX	SN74LVC374A MIN	SN74LVC374A MAX	UNIT
V_{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V			$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V			1.7		
		V_{CC} = 2.7 V to 3.6 V	2		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V				$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V				0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8		0.8	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3-state	0	5.5	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V				−4	mA
		V_{CC} = 2.3 V				−8	
		V_{CC} = 2.7 V		−12		−12	
		V_{CC} = 3 V		−24		−24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V				4	mA
		V_{CC} = 2.3 V				8	
		V_{CC} = 2.7 V		12		12	
		V_{CC} = 3 V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	SN54LVC374A			SN74LVC374A			UNIT
				MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
V_{OH}	$I_{OH} = -100$ μA		1.65 V to 3.6 V				$V_{CC} - 0.2$			V
			2.7 V to 3.6 V	$V_{CC} - 0.2$						
	$I_{OH} = -4$ mA		1.65 V				1.2			
	$I_{OH} = -8$ mA		2.3 V				1.7			
	$I_{OH} = -12$ mA		2.7 V	2.2			2.2			
			3 V	2.4			2.4			
	$I_{OH} = -24$ mA		3 V	2.2			2.2			
V_{OL}	$I_{OL} = 100$ μA		1.65 V to 3.6 V						0.2	V
			2.7 V to 3.6 V			0.2				
	$I_{OL} = 4$ mA		1.65 V						0.45	
	$I_{OL} = 8$ mA		2.3 V						0.7	
	$I_{OL} = 12$ mA		2.7 V			0.4			0.4	
	$I_{OL} = 24$ mA		3 V			0.55			0.55	
I_I	$V_I = 0$ to 5.5 V		3.6 V			±5			±5	μA
I_{off}	V_I or $V_O = 5.5$ V		0						±10	μA
I_{OZ}	$V_O = 0$ to 5.5 V		3.6 V			±15			±10	μA
I_{CC}	$V_I = V_{CC}$ or GND	$I_O = 0$	3.6 V			10			10	μA
	3.6 V $\leq V_I \leq 5.5$ V[2]					10			10	
ΔI_{CC}	One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500			500	μA
C_i	$V_I = V_{CC}$ or GND		3.3 V		4	12		4		pF
C_o	$V_O = V_{CC}$ or GND		3.3 V		5.5	12		5.5		pF

(1) All typical values are at $V_{CC} = 3.3$ V, $T_A = 25°C$.
(2) This applies in the disabled state only.

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Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVC374A				UNIT
		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		80		100	MHz
t_w	Pulse duration, CLK high or low	3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	2		2		ns
t_h	Hold time, data after CLK↑	1.5		1.5		ns

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN74LVC374A								UNIT
		V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		(1)		(1)		80		100	MHz
t_w	Pulse duration, CLK high or low	(1)		(1)		3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	(1)		(1)		2		2		ns
t_h	Hold time, data after CLK↑	(1)		(1)		1.5		1.5		ns

(1)   This information was not available at the time of publication.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC374A				UNIT
			V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
f_{max}			80		100		MHz
t_{pd}	CLK	Q		9.5	1	8.5	ns
t_{en}	$\overline{OE}$	Q		9.5	1	8.5	ns
t_{dis}	$\overline{OE}$	Q		8	1	7	ns

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC374A								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			(1)		(1)		80		100		MHz
t_{pd}	CLK	Q	(1)	(1)	(1)	(1)		8.1	1.5	7	ns
t_{en}	$\overline{OE}$	Q	(1)	(1)	(1)	(1)		8.5	1.5	7.5	ns
t_{dis}	$\overline{OE}$	Q	(1)	(1)	(1)	(1)		7.1	1.5	6.5	ns
$t_{sk(o)}$										1	ns

(1)   This information was not available at the time of publication.

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V TYP	V_{CC} = 2.5 V TYP	V_{CC} = 3.3 V TYP	UNIT
C_{pd} Power dissipation capacitance per flip-flop	Outputs enabled	f = 10 MHz	(1)	(1)	54.5	pF
	Outputs disabled		(1)	(1)	13.5	

(1)   This information was not available at the time of publication.

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PARAMETER MEASUREMENT INFORMATION
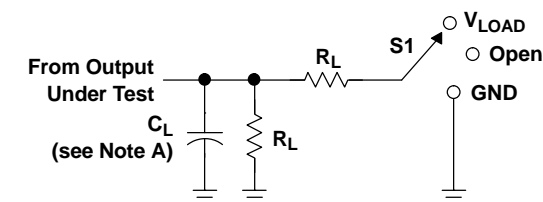
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
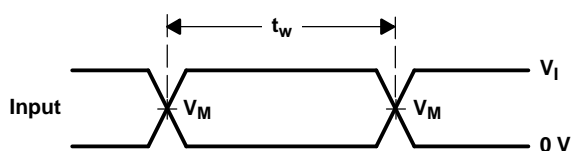
VOLTAGE WAVEFORMS
PULSE DURATION
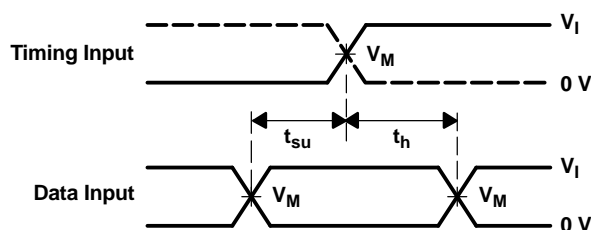
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
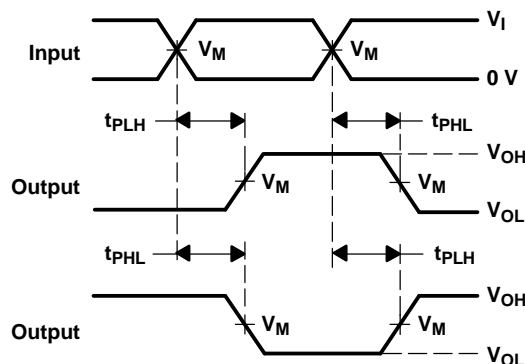
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS
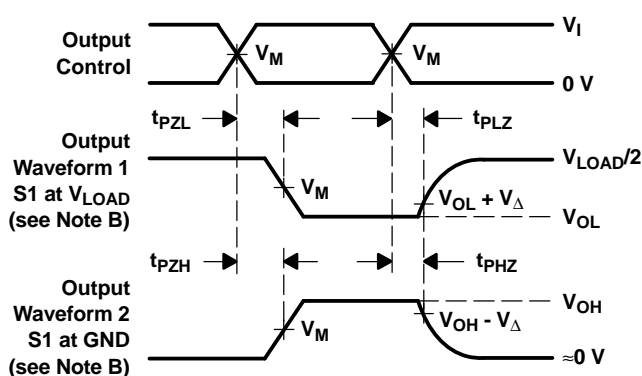
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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24-Jan-2013

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
5962-9757401Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	-55 to 125	5962-9757401Q2A SNJ54LVC 374AFK	Samples
5962-9757401QRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	-55 to 125	5962-9757401QR A SNJ54LVC374AJ	Samples
5962-9757401QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	-55 to 125	5962-9757401QS A SNJ54LVC374AW	Samples
5962-9757401V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9757401V2A SNV54LVC 374AFK	Samples
5962-9757401VRA	ACTIVE	CDIP	J	20	20	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9757401VR A SNV54LVC374AJ	Samples
5962-9757401VSA	ACTIVE	CFP	W	20	25	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9757401VS A SNV54LVC374AW	Samples
SN74LVC374ADBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	-40 to 85		
SN74LVC374ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC374A	Samples
SN74LVC374ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC374A	Samples
SN74LVC374ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC374A	Samples
SN74LVC374ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC374A	Samples
SN74LVC374ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC374A	Samples
SN74LVC374ADGVRG4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC374A	Samples
SN74LVC374ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC374A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74LVC374ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC374A	Samples
SN74LVC374ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC374A	Samples
SN74LVC374ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC374A	Samples
SN74LVC374ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC374A	Samples
SN74LVC374ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC374A	Samples
SN74LVC374AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74LVC374AN	Samples
SN74LVC374ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74LVC374AN	Samples
SN74LVC374ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC374A	Samples
SN74LVC374ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC374A	Samples
SN74LVC374ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC374A	Samples
SN74LVC374APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC374A	Samples
SN74LVC374APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC374A	Samples
SN74LVC374APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC374A	Samples
SN74LVC374APWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		
SN74LVC374APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC374A	Samples
SN74LVC374APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC374A	Samples
SN74LVC374APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC374A	Samples
SN74LVC374APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC374A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74LVC374APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC374A	Samples
SN74LVC374APWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC374A	Samples
SN74LVC374ARGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC374A	Samples
SN74LVC374ARGYRG4	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC374A	Samples
SNJ54LVC374AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9757401Q2A SNJ54LVC 374AFK	Samples
SNJ54LVC374AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9757401QRA SNJ54LVC374AJ	Samples
SNJ54LVC374AW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9757401QSA SNJ54LVC374AW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVC374A, SN54LVC374A-SP, SN74LVC374A :

- Catalog: SN74LVC374A, SN54LVC374A

- Automotive: SN74LVC374A-Q1, SN74LVC374A-Q1

- Enhanced Product: SN74LVC374A-EP, SN74LVC374A-EP

- Military: SN54LVC374A

- Space: SN54LVC374A-SP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC374ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVC374ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC374ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LVC374ANSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LVC374APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC374APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC374APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC374APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC374ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC374ADBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LVC374ADGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74LVC374ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LVC374ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LVC374APWR	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74LVC374APWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74LVC374APWRG4	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74LVC374APWT	TSSOP	PW	20	250	367.0	367.0	38.0
SN74LVC374ARGYR	VQFN	RGY	20	3000	367.0	367.0	35.0

J (R—GDIP—T**)   CERAMIC DUAL IN—LINE PACKAGE
14 LEADS SHOWN
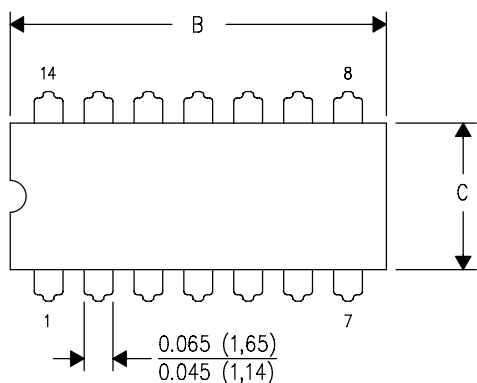
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)
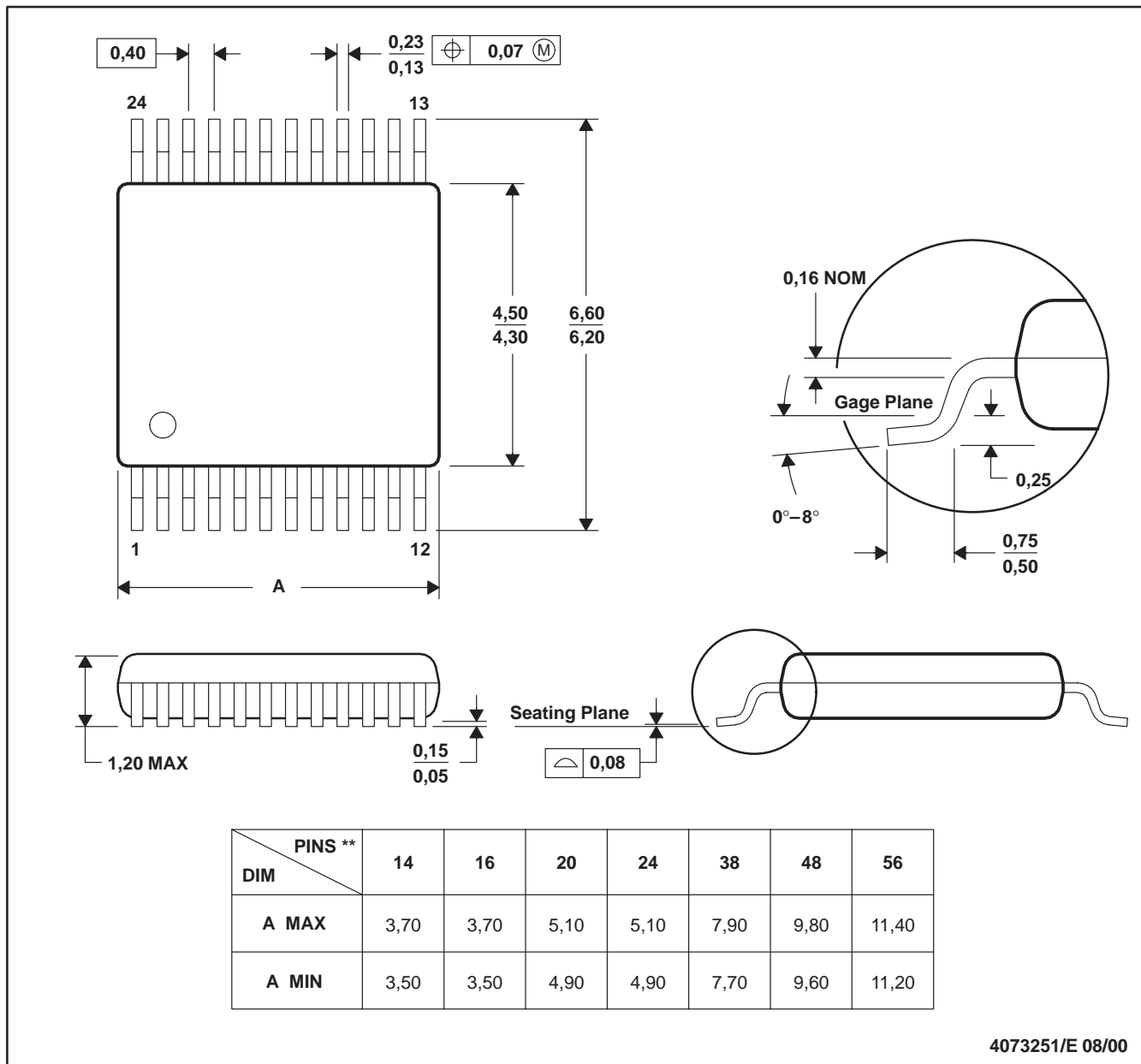
A

0°—15°

0.014 (0,36)
0.008 (0,20)
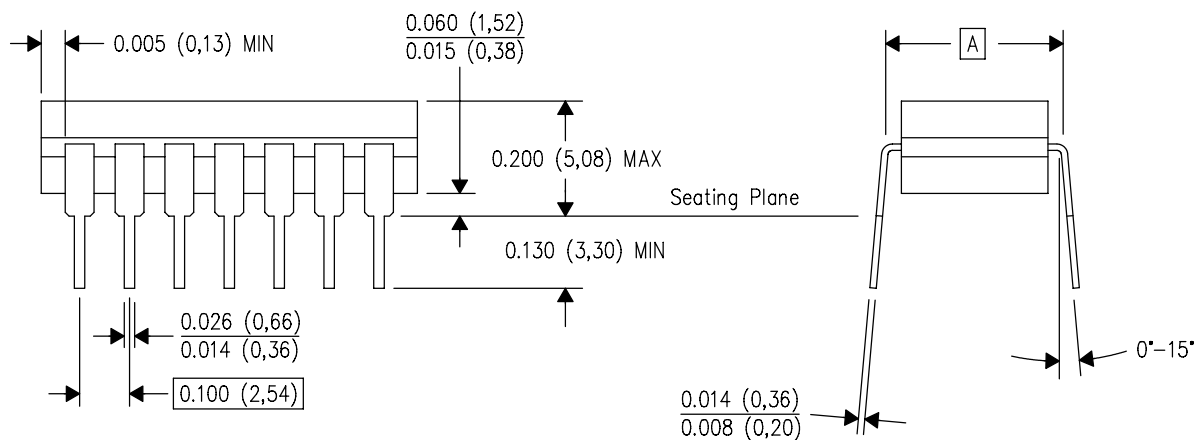
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. This package is hermetically sealed with a ceramic lid using glass frit.
          D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E. Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

W (R−GDFP−F20)   CERAMIC DUAL FLATPACK
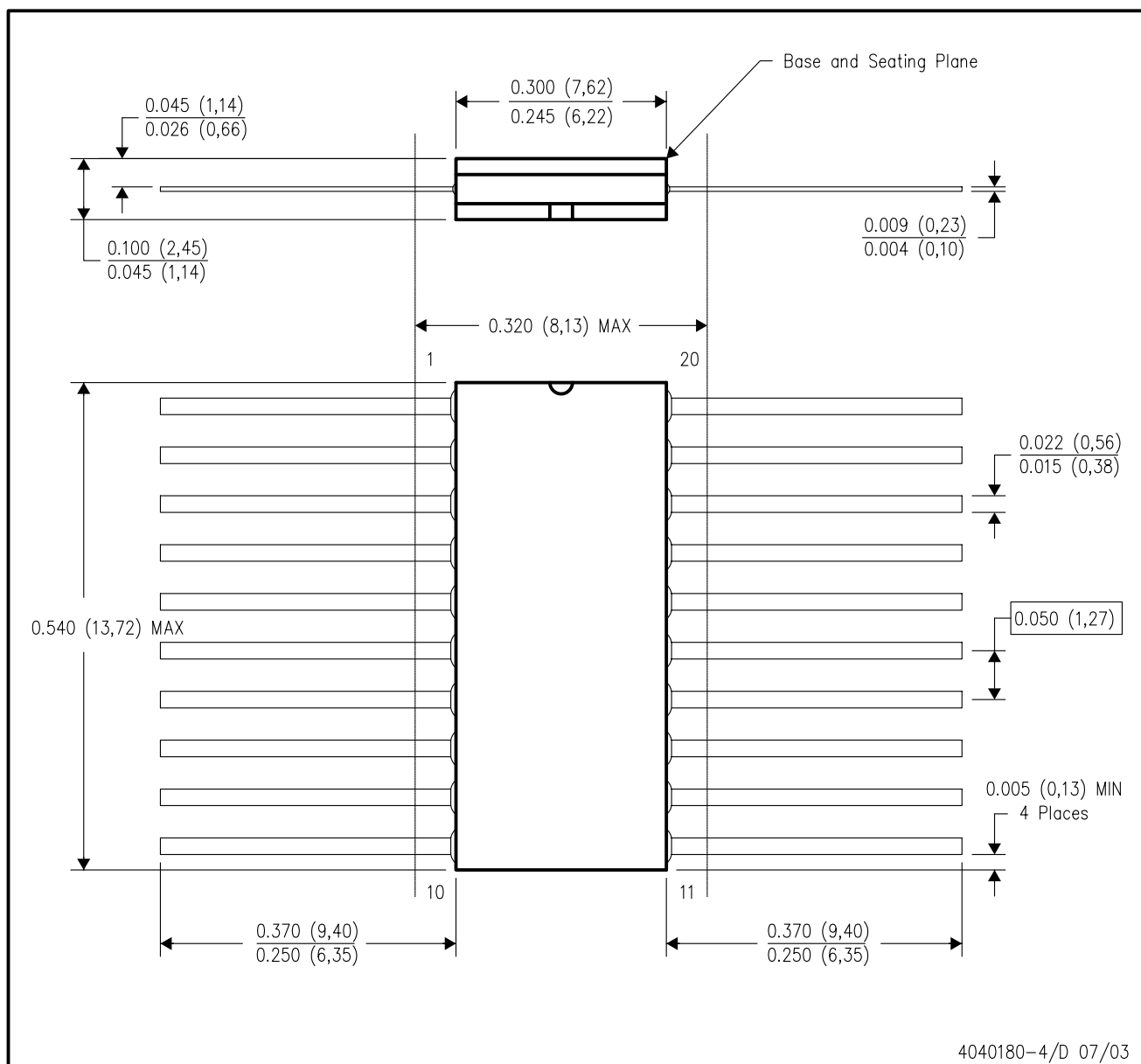
Base and Seating Plane

$\frac{0.045\ (1,14)}{0.026\ (0,66)}$

$\frac{0.300\ (7,62)}{0.245\ (6,22)}$

$\frac{0.100\ (2,45)}{0.045\ (1,14)}$

$\frac{0.009\ (0,23)}{0.004\ (0,10)}$

0.320 (8,13) MAX

1   20

$\frac{0.022\ (0,56)}{0.015\ (0,38)}$

0.540 (13,72) MAX

0.050 (1,27)

0.005 (0,13) MIN
4 Places

10   11

$\frac{0.370\ (9,40)}{0.250\ (6,35)}$ $\frac{0.370\ (9,40)}{0.250\ (6,35)}$

4040180−4/D 07/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package can be hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only.
         E. Falls within Mil−Std 1835 GDFP2−F20

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FK (S−CQCC−N**) LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN
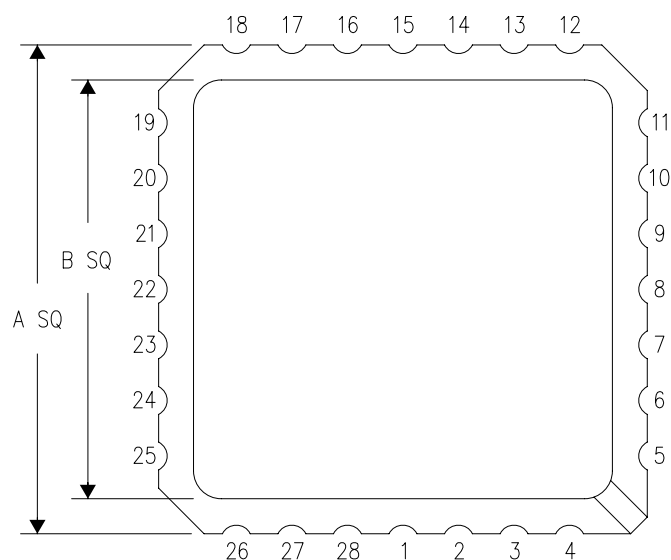
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)
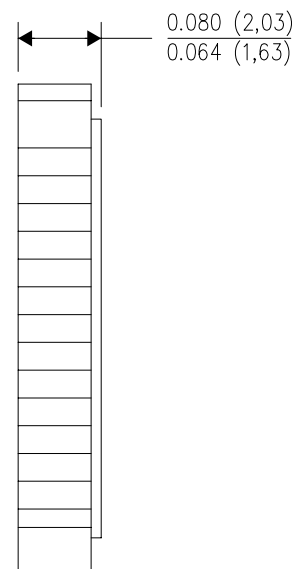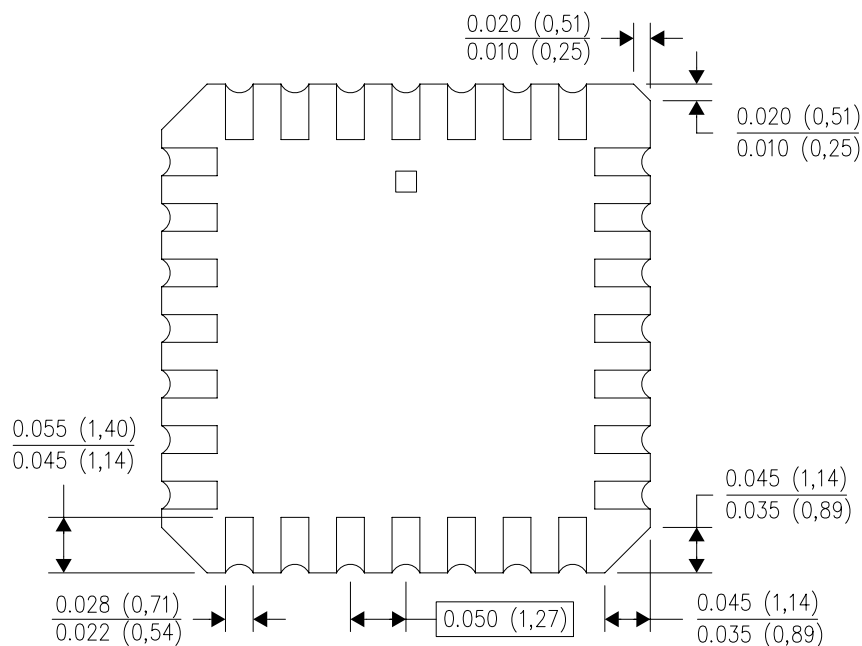
4040140/D 01/11

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a metal lid.
        D. Falls within JEDEC MS−004

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N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE
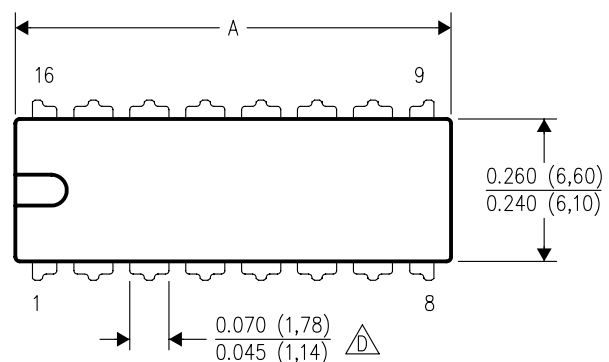
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
⚠C MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14) ⚠D

0.045 (1,14)
0.030 (0,76) ⚠D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option ⚠D

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX
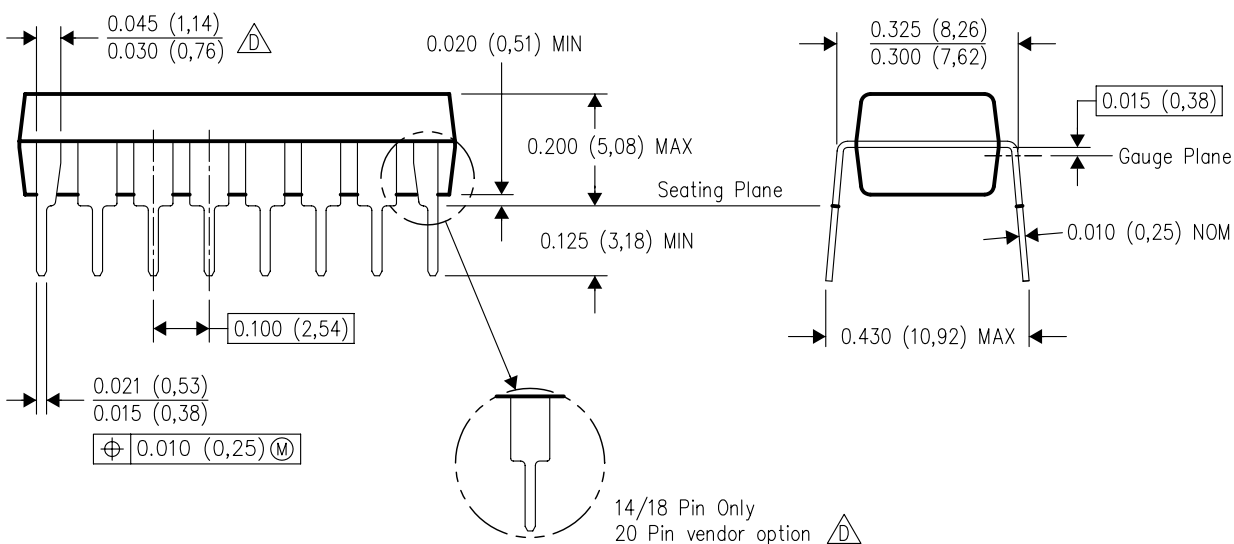
4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
    ⚠C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
    ⚠D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

DW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

$$\frac{0.512\ (13,00)}{0.496\ (12,60)}$$

20   11

$$\frac{0.419\ (10,63)}{0.393\ (9,97)}$$

$$\frac{0.299\ (7,60)}{0.291\ (7,40)}$$

1   10

Pin 1
Index Area

$$\frac{0.020\ (0,51)}{0.012\ (0,31)}$$

⊕ | 0.010 (0,25) Ⓜ

0.050 (1,27)

0.104 (2,65) Max

$$\frac{0.012\ (0,30)}{0.004\ (0,10)}$$

$$\frac{0.013\ (0,33)}{0.008\ (0,20)}$$

⌒ | 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

$$\frac{0.050\ (1,27)}{0.016\ (0,40)}$$

4040000−4/G 01/11
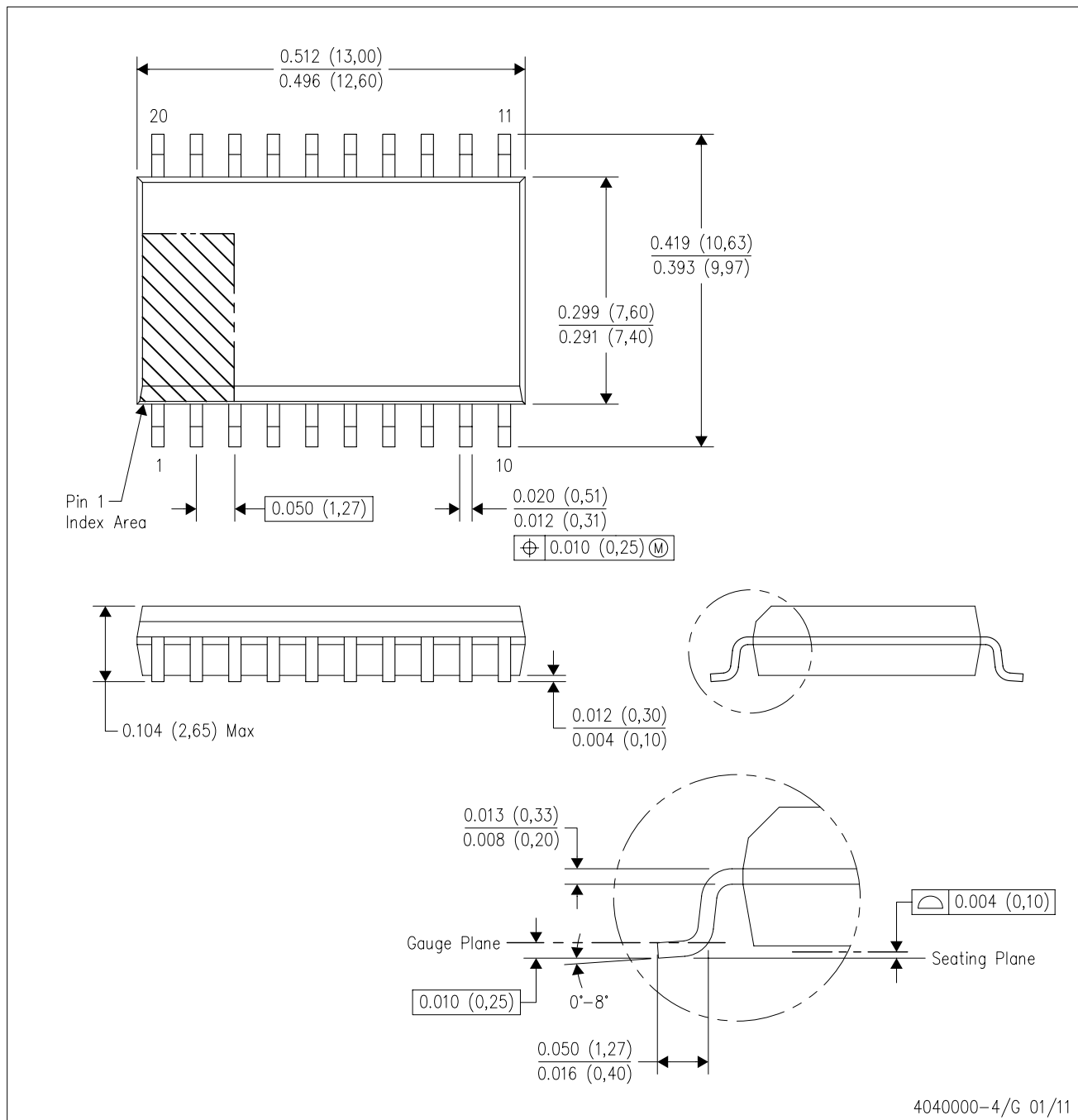
NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AC.

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE
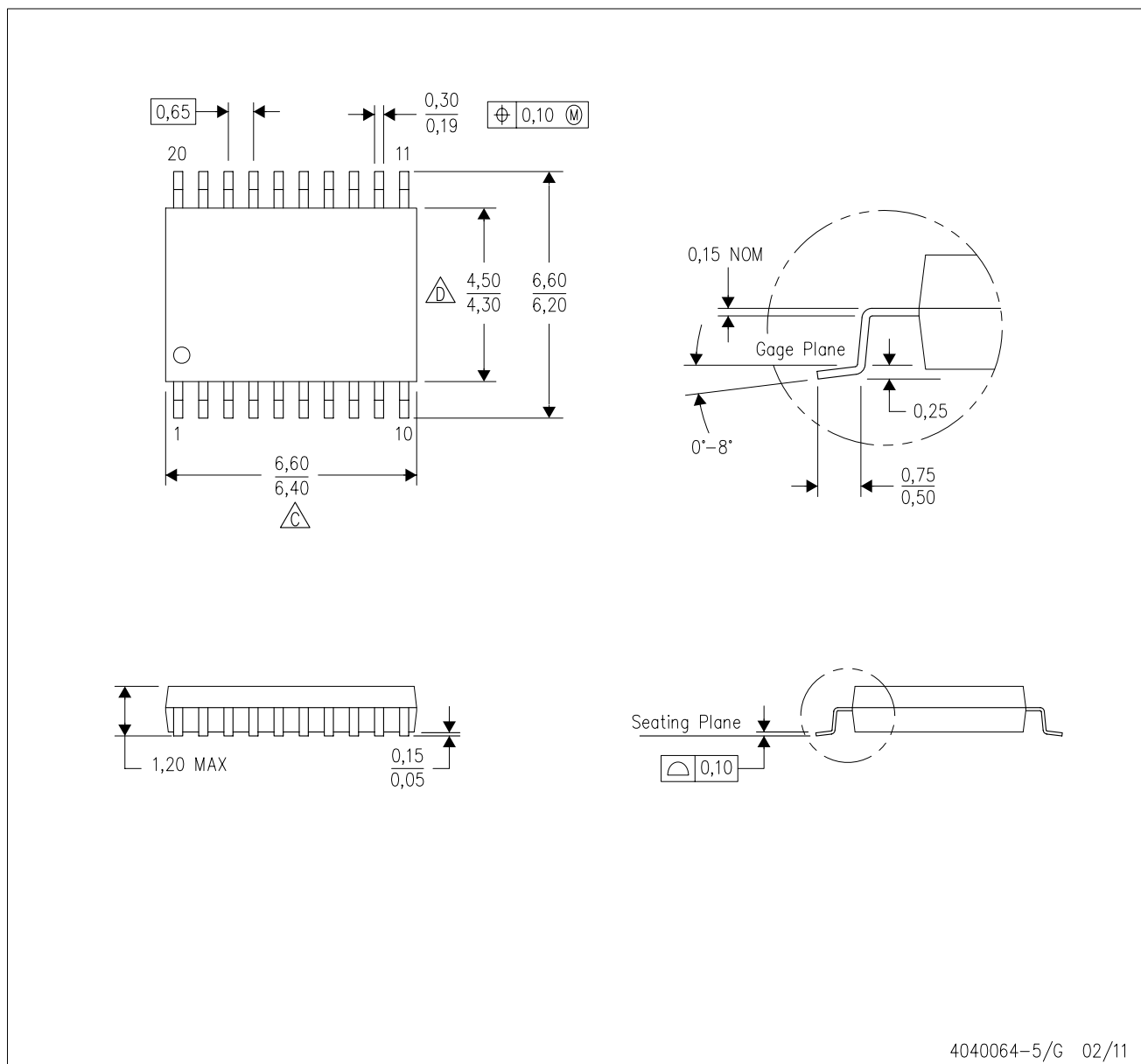
0,65   ◄►   ◄►   0,30
                          0,19   ⊕ 0,10 Ⓜ

20   11

4,50   6,60
4,30   6,20

1   10

6,60
6,40
Ⓒ

0,15 NOM

Gage Plane

0°−8°   0,25

0,75
0,50

1,20 MAX   0,15
                      0,05

Seating Plane

⌓ 0,10

4040064−5/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B. This drawing is subject to change without notice.
          Ⓒ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
          Ⓓ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
          E. Falls within JEDEC MO−153

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

5,6

20x0,25

1,55

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note F)
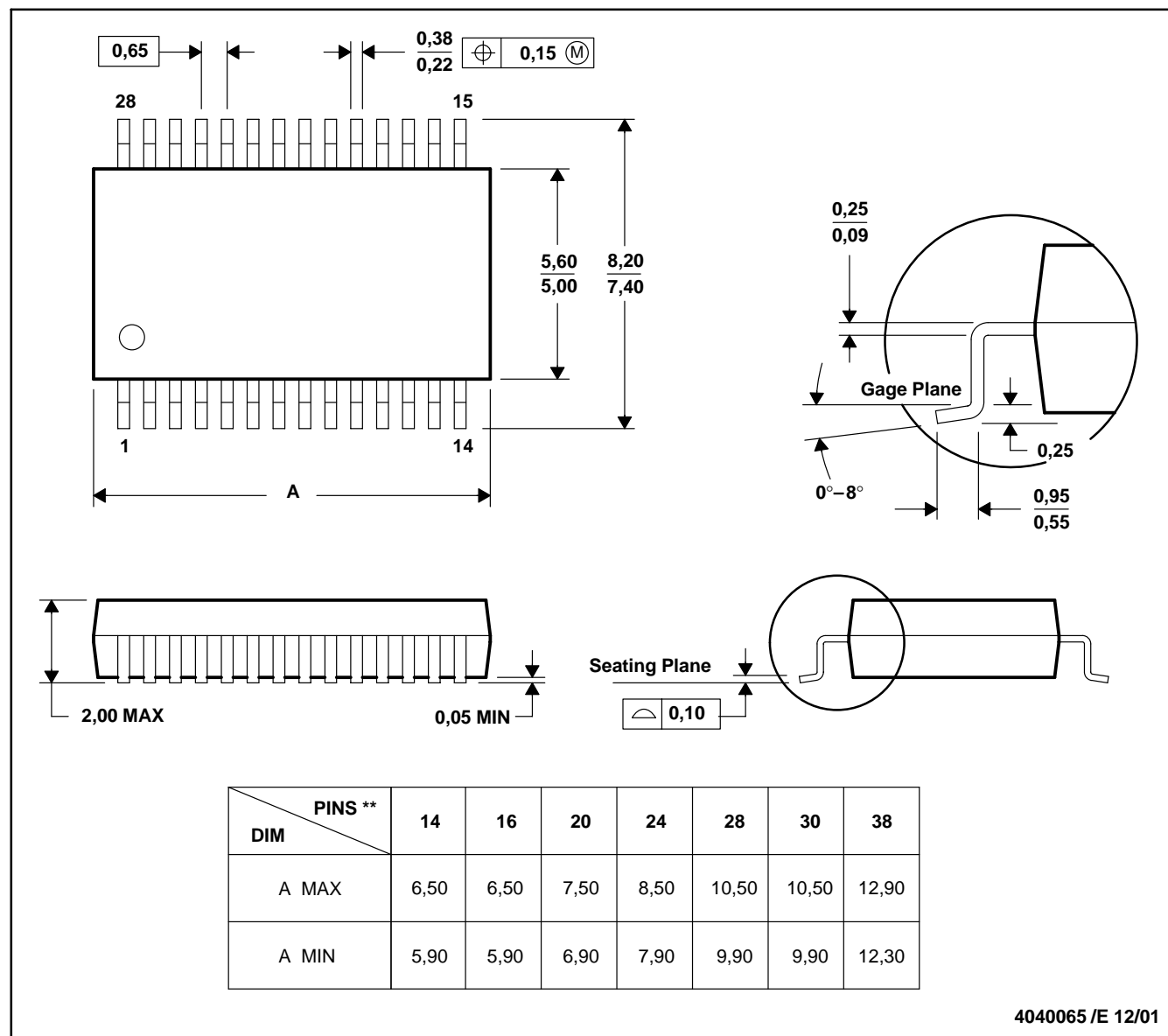
0,3

1,6

0,07
All Around

Pad Geometry
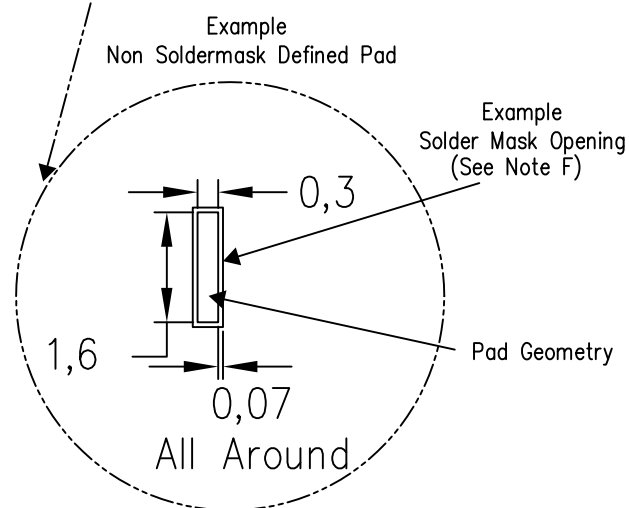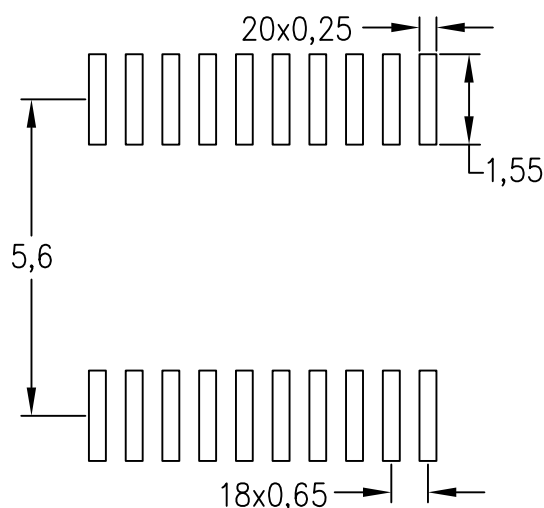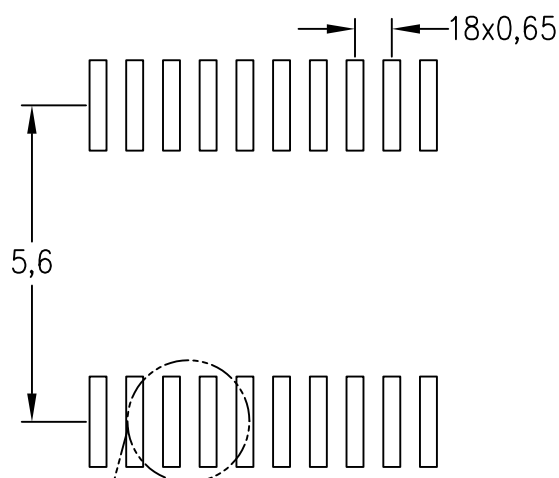
4211284−5/F   12/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate design.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
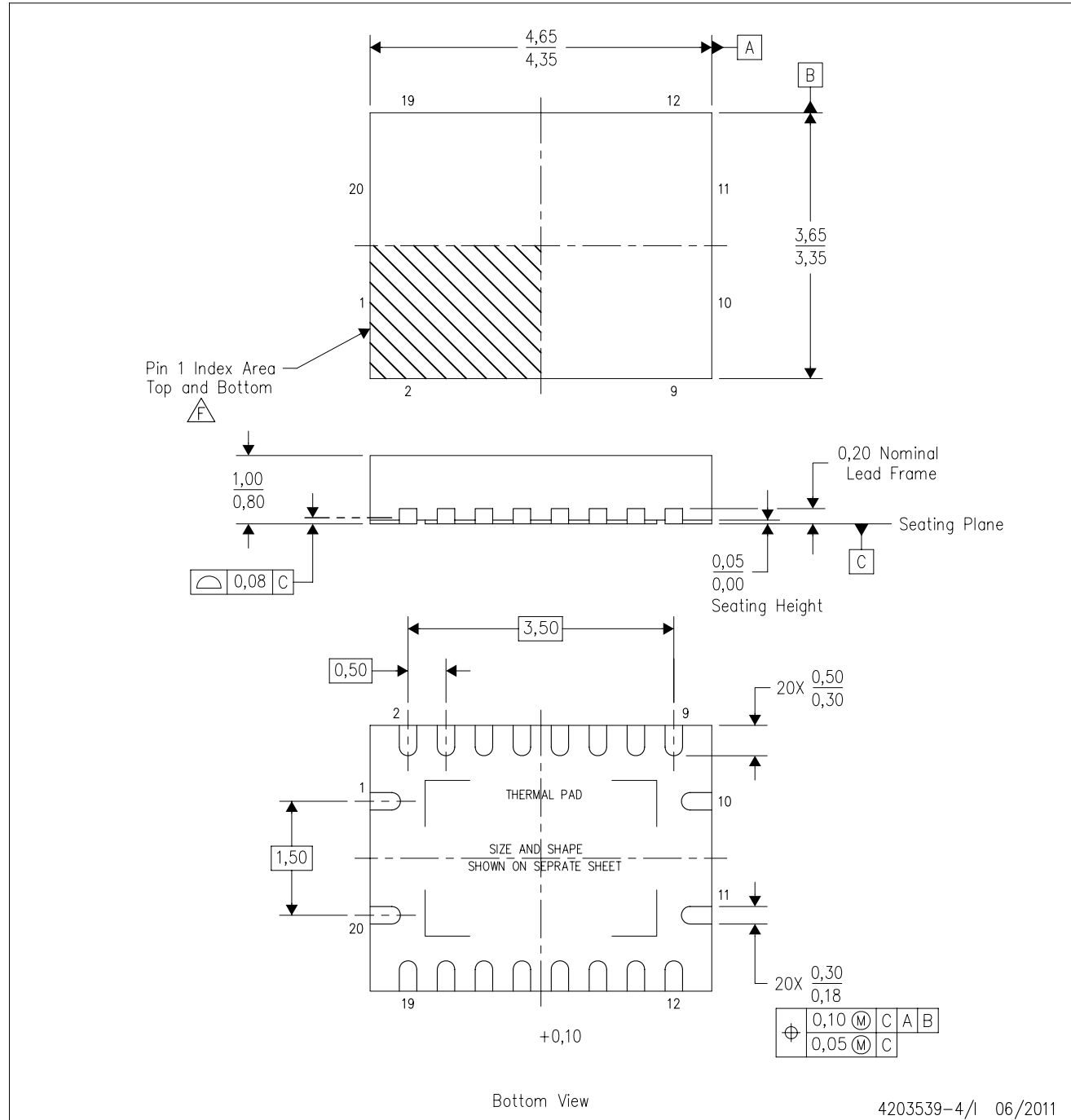
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RGY (R−PVQFN−N20)   PLASTIC QUAD FLATPACK NO−LEAD

4203539−4/I   06/2011

Bottom View

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
          C.   QFN (Quad Flatpack No−Lead) package configuration.
          D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
          E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
          F.   Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
               The Pin 1 identifiers are either a molded, marked, or metal feature.
          G.   Package complies to JEDEC MO−241 variation BA.

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RGY (R–PVQFN–N20)   PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
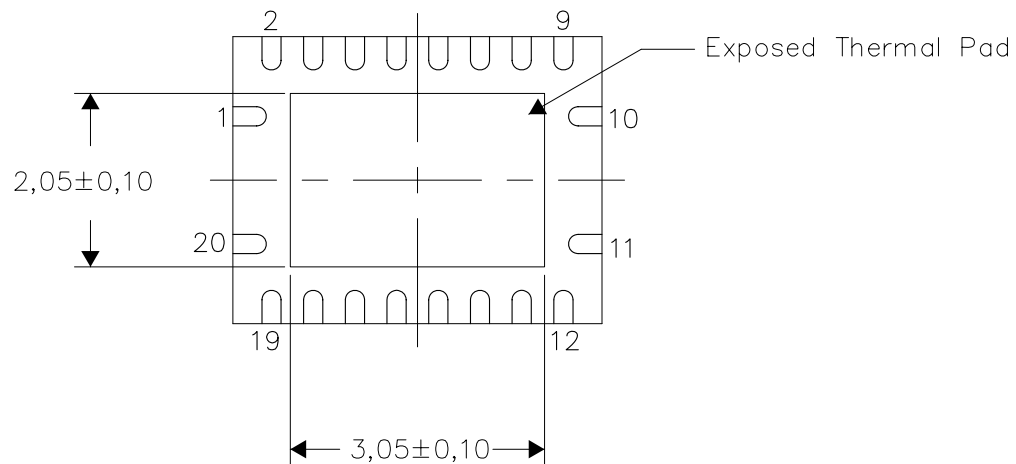
Bottom View

Exposed Thermal Pad Dimensions

4206353–4/0 11/11

NOTE: All linear dimensions are in millimeters

RGY (R−PVQFN−N20)   PLASTIC QUAD FLATPACK NO−LEAD
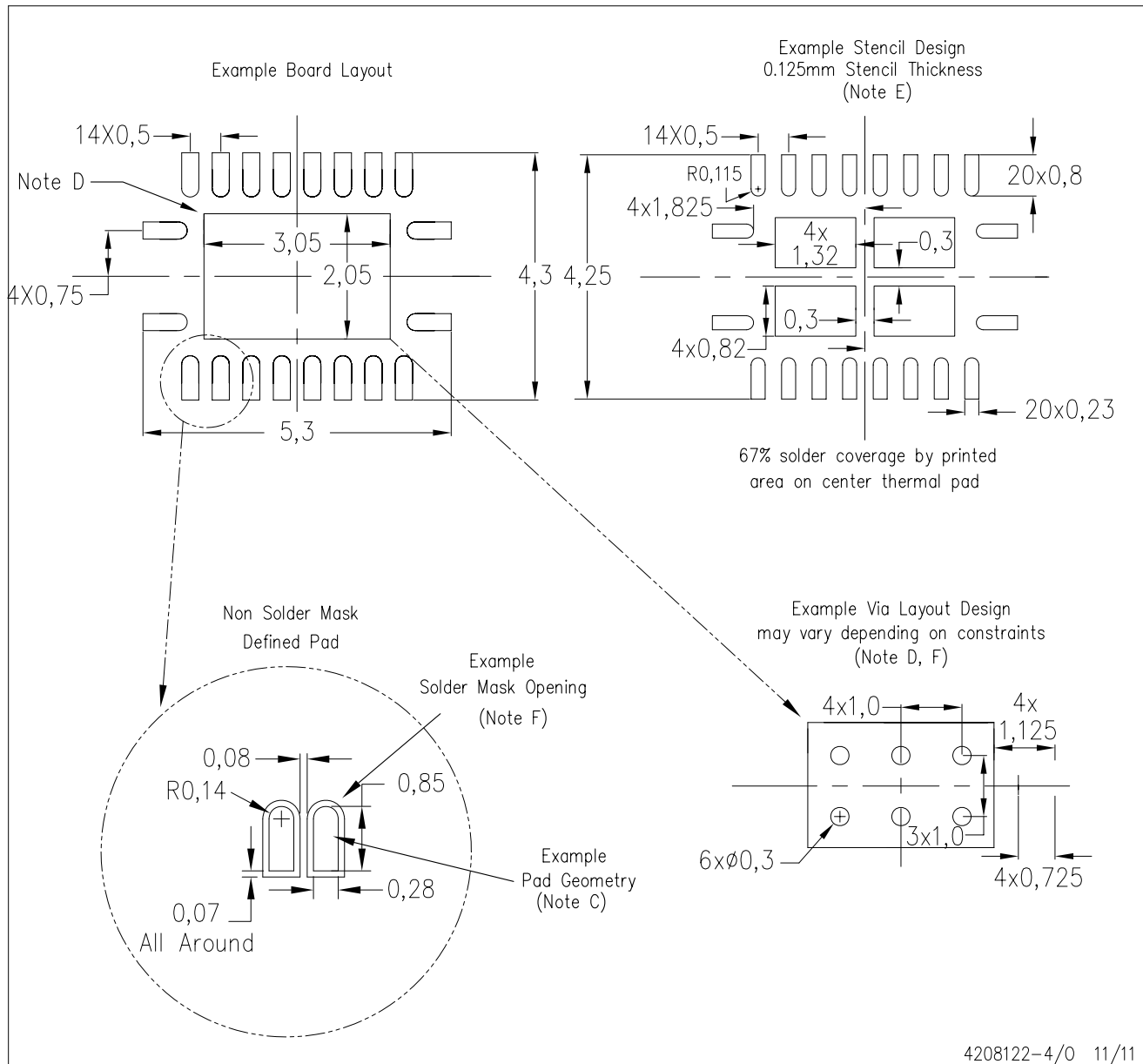
Example Board Layout

14X0,5

Note D

3,05

2,05

4,3 4,25

4X0,75

5,3

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

14X0,5

R0,115

4x1,825

4x
1,32

0,3

20x0,8

0,3

4x0,82

20x0,23

67% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

0,08

R0,14

0,85

0,07

0,28

All Around

Example
Pad Geometry
(Note C)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

4x1,0

4x
1,125

6x∅0,3

3x1,0

4x0,725

4208122−4/0   11/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate designs.
         D.   This package is designed to be soldered to a thermal pad on the board.   Refer to Application Note, Quad Flat−Pack
              QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
              for specific thermal information, via requirements, and recommended board layout.
              These documents are available at www.ti.com <http://www.ti.com>.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.   Customers should
              contact their board assembly site for stencil design recommendations.   Refer to IPC 7525 for stencil design considerations.
         F.   Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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MECHANICAL DATA

NS (R-PDSO-G)** PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN
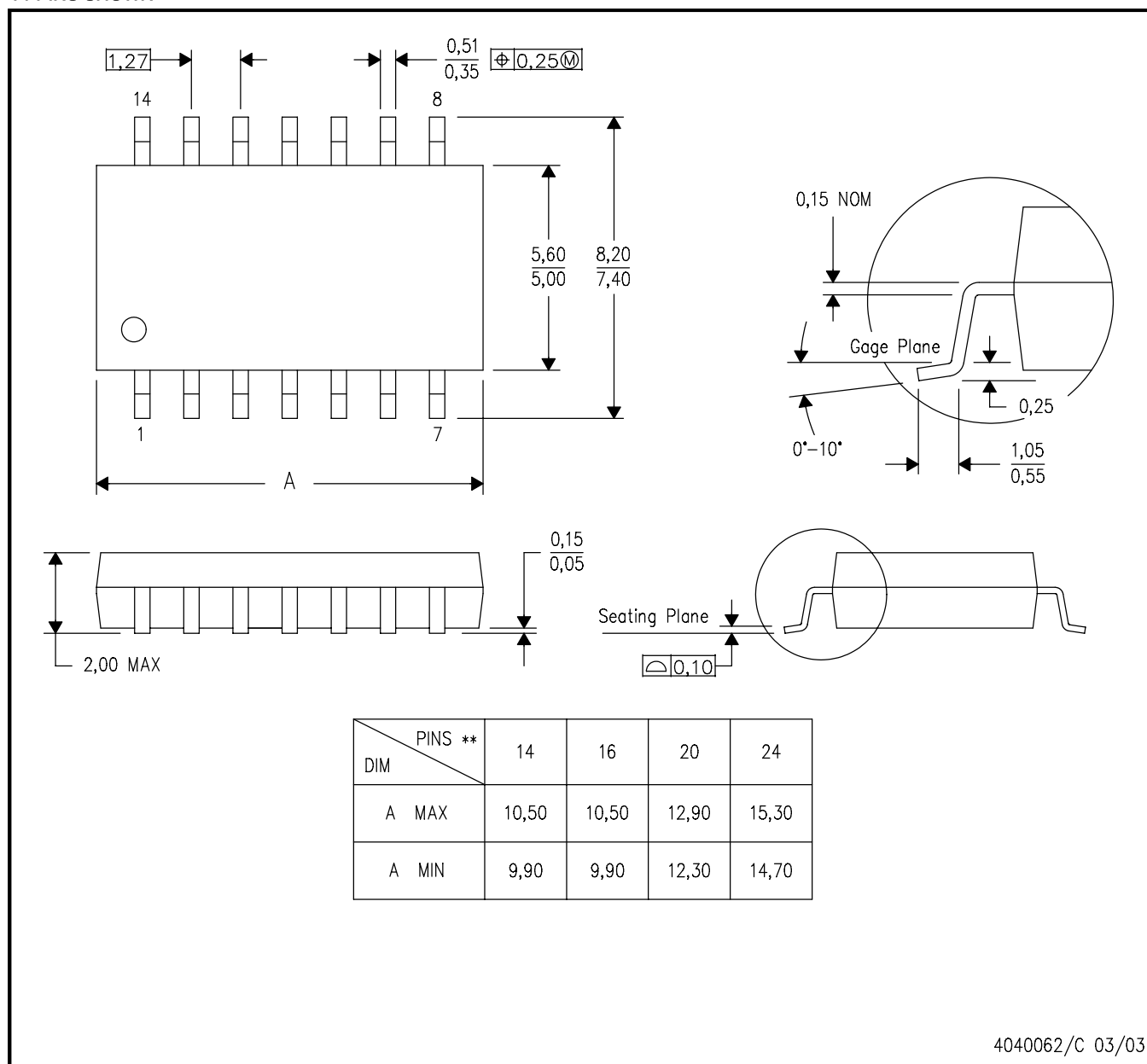
PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
　　　　 B. This drawing is subject to change without notice.
　　　　 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
　　　　 D. Falls within JEDEC MO-150

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