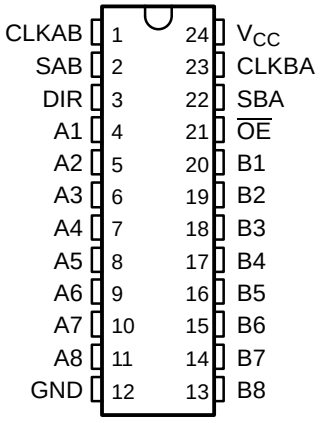
# SN54LVC646A, SN74LVC646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCAS302J–JANUARY 1993–REVISED AUGUST 2005

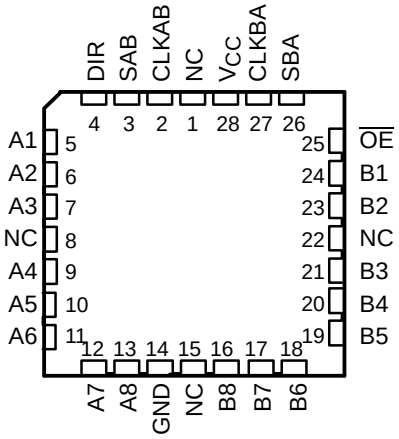
## FEATURES

- **Operate From 1.65 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max $t_{pd}$ of 7.4 ns at 3.3 V**
- **Typical $V_{OLP}$ (Output Ground Bounce) <0.8 at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) >2 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V $V_{CC}$)**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

**SN54LVC646A . . . JT OR W PACKAGE**
**SN74LVC646A . . . DB, DW, NS, OR PW PACKAGE**
**(TOP VIEW)**




**SN54LVC646A . . . FK PACKAGE**
**(TOP VIEW)**




NC - No internal connection

## DESCRIPTION/ORDERING INFORMATION

The SN54LVC646A octal bus transceiver and register is designed for 2.7-V to 3.6-V $V_{CC}$ operation, and the SN74LVC646A octal bus transceiver and register is designed for 1.65-V to 3.6-V $V_{CC}$ operation.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE(1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | SOIC – DW | Tube of 25 | SN74LVC646ADW | LVC646A |
| | | Reel of 2000 | SN74LVC646ADWR | |
| | SOP – NS | Reel of 2000 | SN74LVC646ANSR | LVC646A |
| | SSOP – DB | Reel of 2000 | SN74LVC646ADBR | LC646A |
| | TSSOP – PW | Tube of 60 | SN74LVC646APW | LC646A |
| | | Reel of 2000 | SN74LVC646APWR | |
| | | Reel of 250 | SN74LVC646APWT | |
| –55°C to 125°C | CDIP – JT | Tube of 15 | SNJ54LVC646AJT | SNJ54LVC646AJT |
| | CFP – W | Tube of 85 | SNJ54LVC646AW | SNJ54LVC646AW |
| | LCCC – FK | Tube of 42 | SNJ54LVC646AFK | SNJ54LVC646AFK |

(1) Package drawings, standard packing quantities, thermal data, symboliztion, and PCB design guidelines are available at www.ti.com/sc/package.

## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

These devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that are performed with the 'LVC646A devices.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port is stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data is stored in one register and B data can be stored in the other register.

When an output function is disabled, the input function still is enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

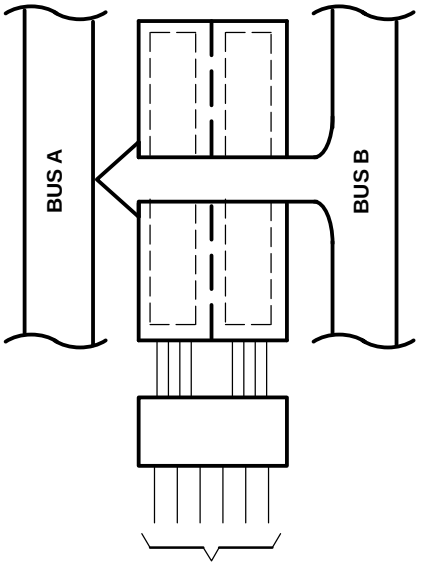
These devices are fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**FUNCTION TABLE**

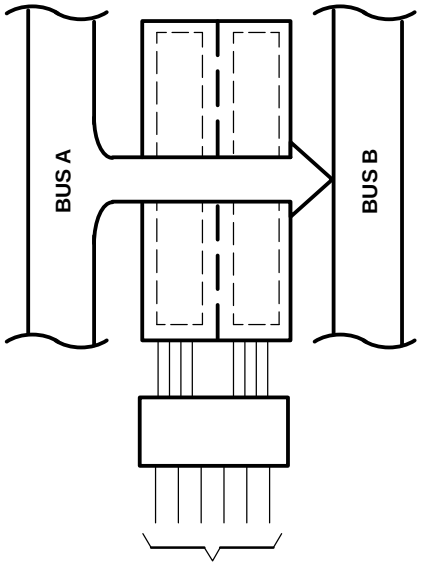
| INPUTS | | | | | | DATA I/O | | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA | A1–A8 | B1–B8 | |
| X | X | ↑ | X | X | X | Input | Unspecified(1) | Store A, B unspecified(1) |
| X | X | X | ↑ | X | X | Unspecified(1) | Input | Store B, A unspecified(1) |
| H | X | ↑ | ↑ | X | X | Input | Input | Store and B data |
| H | X | H or L | H or L | X | X | Input disabled | Input disabled | Isolation, hold storage |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | H or L | X | H | Output | Input | Stored B data to A bus |
| L | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| L | H | H or L | X | H | X | Input | Output | Stored A data to B bus |

(1) The data-output functions can be enabled or disabled by various signals at $\overline{OE}$ and DIR. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.



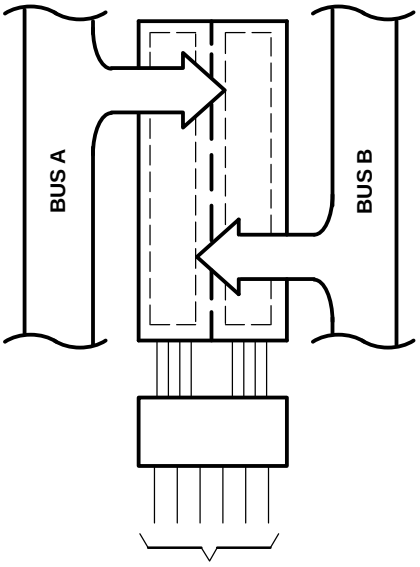

| 21 | 3 | 1 | 23 | 2 | 22 |
|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
| L | L | X | X | X | L |

**REAL-TIME TRANSFER**
**BUS B TO BUS A**



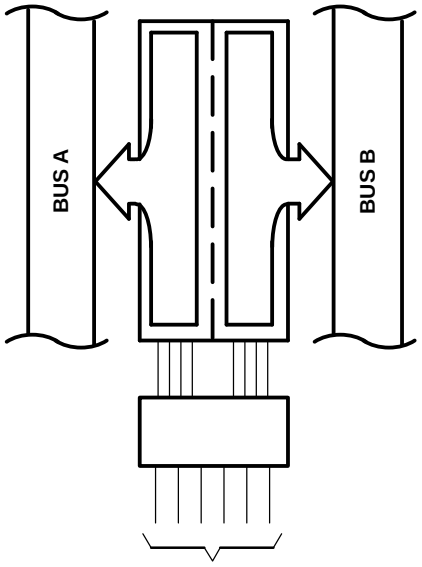

| 21 | 3 | 1 | 23 | 2 | 22 |
|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
| L | H | X | X | L | X |

**REAL-TIME TRANSFER**
**BUS A TO BUS B**




| 21 | 3 | 1 | 23 | 2 | 22 |
|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
| X | X | ↑ | X | X | X |
| X | X | X | ↑ | X | X |
| H | X | ↑ | ↑ | X | X |

**STORAGE FROM**
**A, B, OR A AND B**

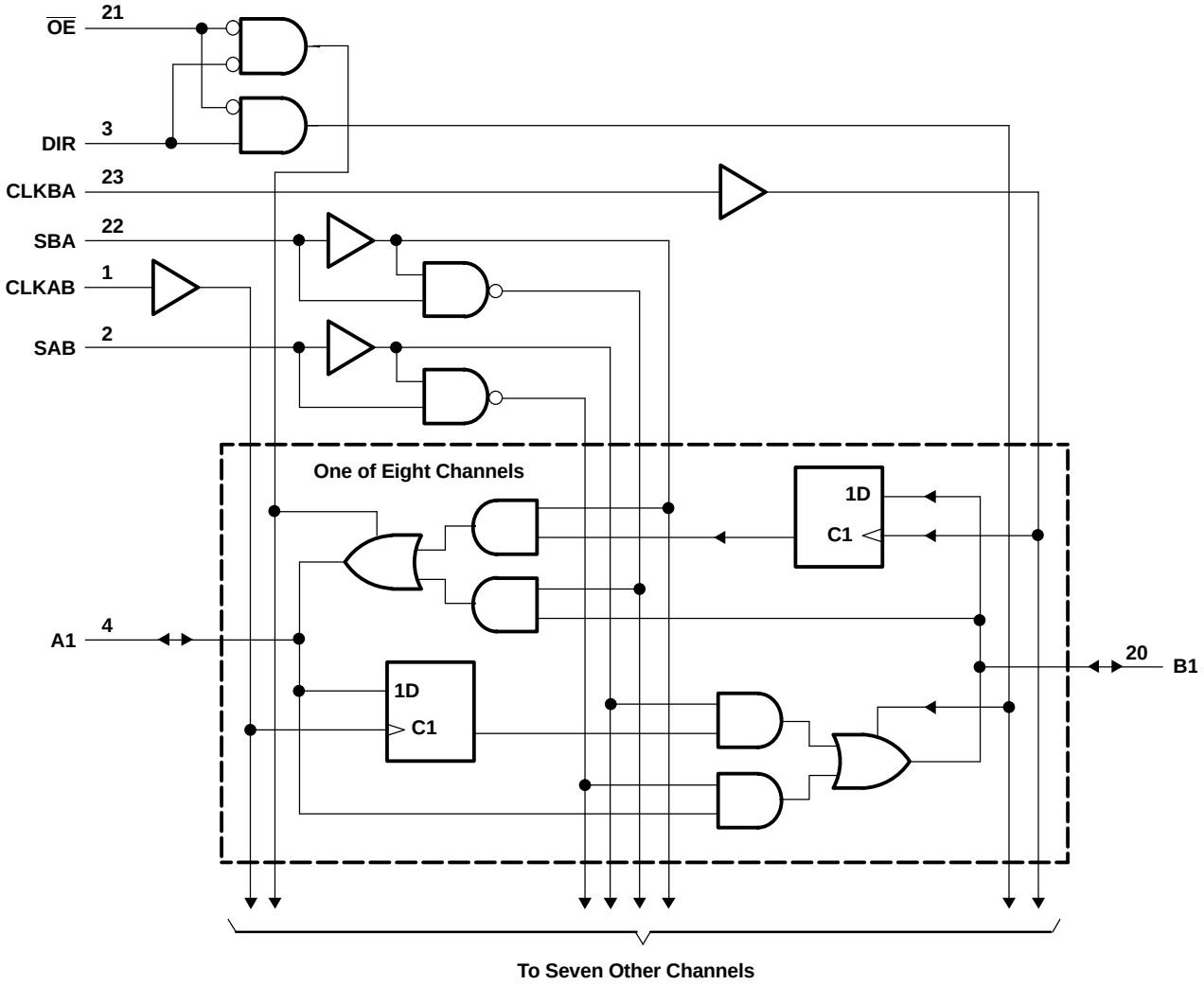



| 21 | 3 | 1 | 23 | 2 | 22 |
|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
| L | L | X | H or L | X | H |
| L | H | H or L | X | H | X |

**TRANSFER STORED DATA**
**TO A AND/OR B**

**Figure 1. Bus-Management Functions**

## LOGIC DIAGRAM (POSITIVE LOGIC)




Pin numbers shown are for the DB, DW, JT, NS, PW, and W packages.

## Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage range applied to any output in the high or low state(2)(3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance(4) | DB package | | 63 | °C/W |
| | | DW package | | 46 | |
| | | NS package | | 65 | |
| | | PW package | | 88 | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of $V_{CC}$ is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions(1)

| | | | SN54LVC646A | | SN74LVC646A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | Operating | 2 | 3.6 | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | | 0.65 × $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | | 1.7 | | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | | | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | | | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | | 0.8 | |
| $V_I$ | Input voltage | | 0 | 5.5 | | 5.5 | V |
| $V_O$ | Output voltage | High or low state | 0 | $V_{CC}$ | | $V_{CC}$ | V |
| | | 3-state | 0 | 5.5 | | 5.5 | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | | | –4 | mA |
| | | $V_{CC}$ = 2.3 V | | | | –8 | |
| | | $V_{CC}$ = 2.7 V | | –12 | | –12 | |
| | | $V_{CC}$ = 3 V | | –24 | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | | | 8 | |
| | | $V_{CC}$ = 2.7 V | | 12 | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | SN54LVC646A | | | SN74LVC646A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP(1) | MAX | MIN | TYP(1) | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –100 µA | | 1.65 V to 3.6 V | | | | $V_{CC}$ – 0.2 | | | V |
| | | | | 2.7 V to 3.6 V | $V_{CC}$ – 0.2 | | | | | | |
| | | $I_{OH}$ = –4 mA | | 1.65 V | | | | 1.2 | | | |
| | | $I_{OH}$ = –8 mA | | 2.3 V | | | | 1.7 | | | |
| | | $I_{OH}$ = –12 mA | | 2.7 V | 2.2 | | | 2.2 | | | |
| | | | | 3 V | 2.4 | | | 2.4 | | | |
| | | $I_{OH}$ = –24 mA | | 3 V | 2.2 | | | 2.2 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 µA | | 1.65 V to 3.6 V | | | | | | 0.2 | V |
| | | | | 2.7 V to 3.6 V | | | 0.2 | | | | |
| | | $I_{OL}$ = 4 mA | | 1.65 V | | | | | | 0.45 | |
| | | $I_{OL}$ = 8 mA | | 2.3 V | | | | | | 0.7 | |
| | | $I_{OL}$ = 12 mA | | 2.7 V | | | 0.4 | | | 0.4 | |
| | | $I_{OL}$ = 24 mA | | 3 V | | | 0.55 | | | 0.55 | |
| $I_I$ | Control inputs | $V_I$ = 0 to 5.5 V | | 3.6 V | | | ±5 | | | ±5 | µA |
| $I_{off}$ | | $V_I$ or $V_O$ = 5.5 V | | 0 | | | | | | ±10 | µA |
| $I_{OZ}$(2) | | $V_O$ = 0 to 5.5 V | | 3.6 V | | | ±15 | | | ±10 | µA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND | $I_O$ = 0 | 3.6 V | | | 10 | | | 10 | µA |
| | | 3.6 V ≤ $V_I$ ≤ 5.5 V(3) | | | | | 10 | | | 10 | |
| $\Delta I_{CC}$ | | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | 2.7 V to 3.6 V | | | 500 | | | 500 | µA |
| $C_i$ | Control inputs | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 4.5 | | | 4.5 | | pF |
| $C_{io}$ | A or B port | $V_O$ = $V_{CC}$ or GND | | 3.3 V | | 7.5 | | | 7.5 | | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
(2) For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
(3) This applies in the disabled state only.

## Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| | | SN54LVC646A | | | | UNIT |
|---|---|---|---|---|---|---|
| | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | |
| | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 150 | | 150 | MHz |
| $t_w$ | Pulse duration | 3.3 | | 3.3 | | ns |
| $t_{su}$ | Setup time, data before CLK↑ | 1.6 | | 1.5 | | ns |
| $t_h$ | Hold time, data after CLK↑ | 1.7 | | 1.7 | | ns |

## Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| | | SN74LVC646A | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ = 1.8 V ± 0.18 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | (1) | | (1) | | 150 | | 150 | MHz |
| $t_w$ | Pulse duration | (1) | | (1) | | 3.3 | | 3.3 | | ns |
| $t_{su}$ | Setup time, data before CLK↑ | (1) | | (1) | | 1.6 | | 1.5 | | ns |
| $t_h$ | Hold time, data after CLK↑ | (1) | | (1) | | 1.7 | | 1.7 | | ns |

(1) This information was not available at the time of publication.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVC646A | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | |
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 150 | | 150 | | MHz |
| $t_{pd}$ | A or B | B or A | | 7.9 | 1 | 7.4 | ns |
| | CLK | A or B | | 8.8 | 1 | 8.4 | |
| | SBA or SAB | | | 9.9 | 1 | 8.6 | |
| $t_{en}$ | $\overline{OE}$ | A | | 10.2 | 1 | 8.2 | ns |
| $t_{dis}$ | $\overline{OE}$ | A | | 8.9 | 1 | 7.5 | ns |
| $t_{en}$ | DIR | B | | 10.4 | 1 | 8.3 | ns |
| $t_{dis}$ | DIR | B | | 8.7 | 1 | 7.9 | ns |

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74LVC646A | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | (1) | | (1) | | 150 | | 150 | | MHz |
| $t_{pd}$ | A or B | B or A | (1) | (1) | (1) | (1) | | 7.9 | 1 | 7.4 | ns |
| | CLK | A or B | (1) | (1) | (1) | (1) | | 8.8 | 1 | 8.4 | |
| | SBA or SAB | | (1) | (1) | (1) | (1) | | 9.9 | 1 | 8.6 | |
| $t_{en}$ | $\overline{OE}$ | A | (1) | (1) | (1) | (1) | | 10.2 | 1 | 8.2 | ns |
| $t_{dis}$ | $\overline{OE}$ | A | (1) | (1) | (1) | (1) | | 8.9 | 1 | 7.5 | ns |
| $t_{en}$ | DIR | B | (1) | (1) | (1) | (1) | | 10.4 | 1 | 8.3 | ns |
| $t_{dis}$ | DIR | B | (1) | (1) | (1) | (1) | | 8.7 | 1 | 7.9 | ns |

(1) This information was not available at the time of publication.

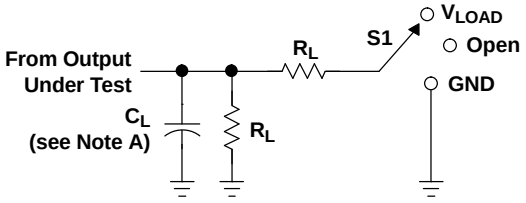
## Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | TYP | TYP | TYP | |
| Cpd | Power dissipation capacitance per transceiver | Outputs enabled | f = 10 MHz | (1) | (1) | 75 | pF |
| | | Outputs disabled | | (1) | (1) | 9 | |

(1) This information was not available at the time of publication.

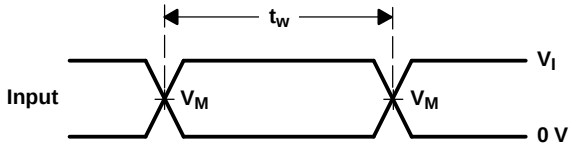
## PARAMETER MEASUREMENT INFORMATION



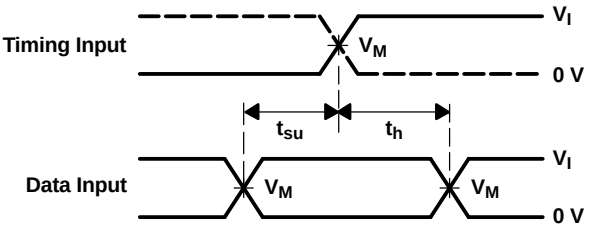

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

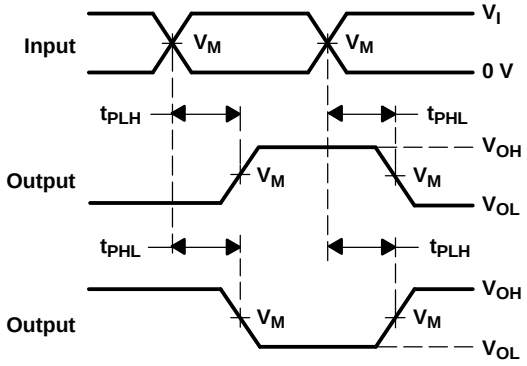
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3.3 V ± 0.3 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



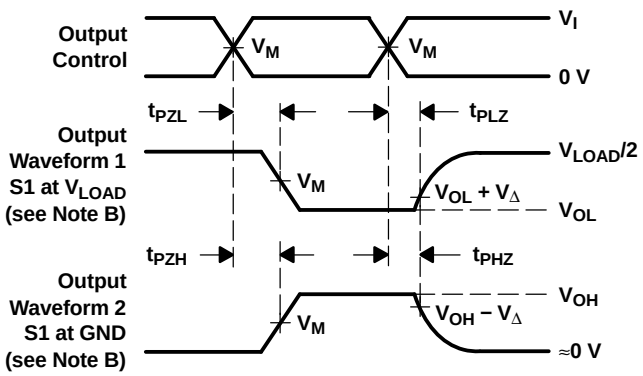

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-9762601Q3A | ACTIVE | LCCC | FK | 28 | 1 | TBD | Call TI | Call TI | |
| 5962-9762601QKA | ACTIVE | CFP | W | 24 | 1 | TBD | Call TI | Call TI | |
| 5962-9762601QLA | ACTIVE | CDIP | JT | 24 | 1 | TBD | Call TI | Call TI | |
| SN74LVC646ADBLE | OBSOLETE | SSOP | DB | 24 | | TBD | Call TI | Call TI | |
| SN74LVC646ADBR | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC646ADBRE4 | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC646ADBRG4 | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC646ADW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC646ADWE4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC646ADWG4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC646APW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC646APWE4 | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC646APWG4 | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC646APWLE | OBSOLETE | TSSOP | PW | 24 | | TBD | Call TI | Call TI | |
| SN74LVC646APWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC646APWRE4 | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC646APWRG4 | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC646APWT | ACTIVE | TSSOP | PW | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC646APWTE4 | ACTIVE | TSSOP | PW | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LVC646APWTG4 | ACTIVE | TSSOP | PW | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SNJ54LVC646AFK | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| SNJ54LVC646AJT | ACTIVE | CDIP | JT | 24 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54LVC646AW | ACTIVE | CFP | W | 24 | 1 | TBD | A42 | N / A for Pkg Type | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



**OTHER QUALIFIED VERSIONS OF SN54LVC646A, SN74LVC646A :**

- Catalog: SN74LVC646A
- Military: SN54LVC646A

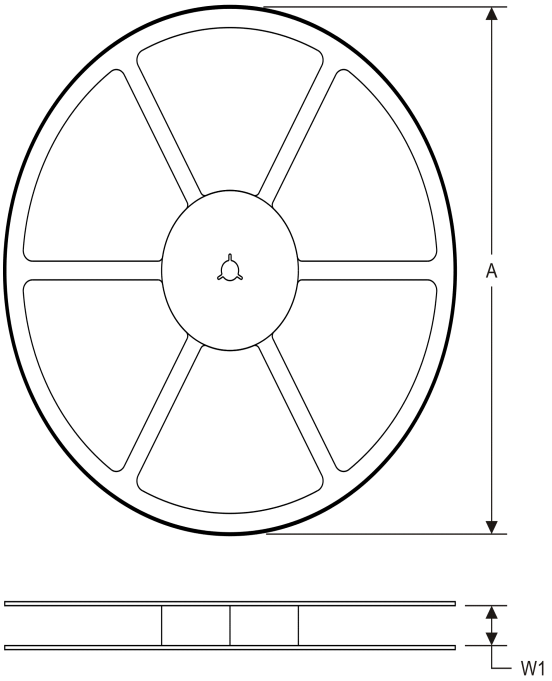
- Space: SN54LVC646A-SP

NOTE: Qualified Version Definitions:

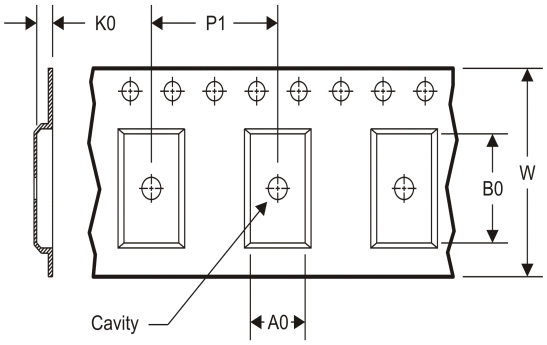
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



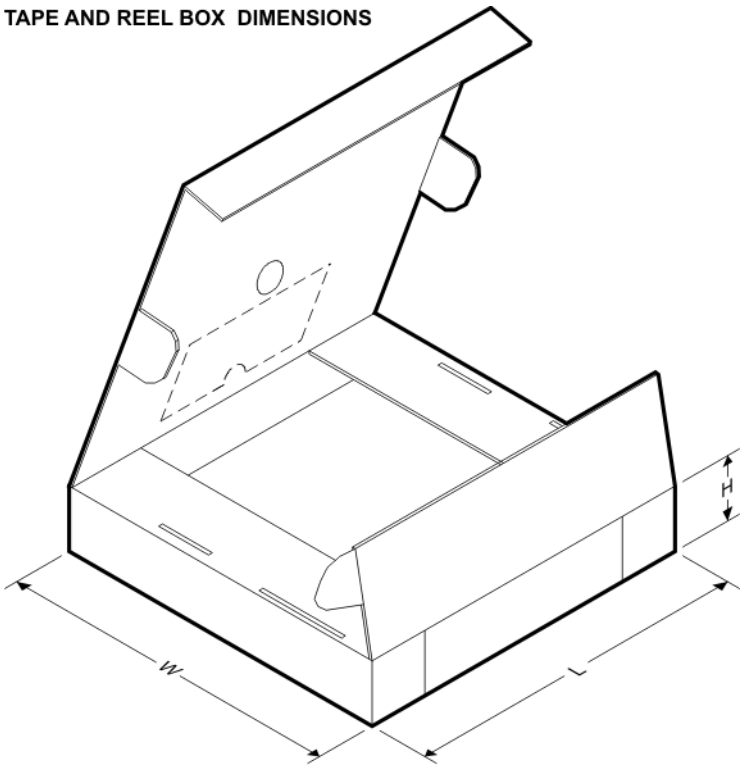

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC646ADBR | SSOP | DB | 24 | 2000 | 330.0 | 16.4 | 8.2 | 8.8 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVC646APWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LVC646APWT | TSSOP | PW | 24 | 250 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



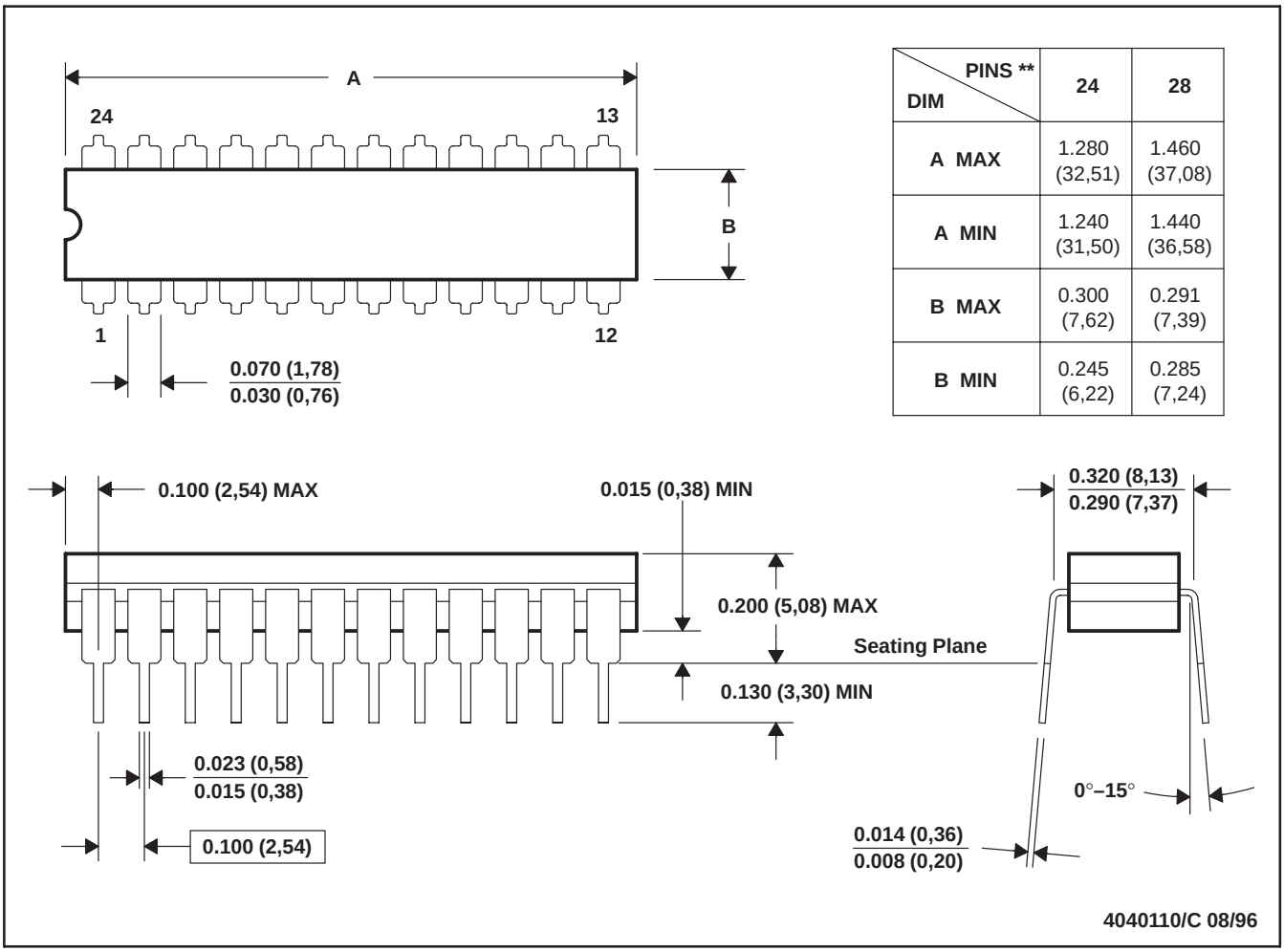

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC646ADBR | SSOP | DB | 24 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVC646APWR | TSSOP | PW | 24 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVC646APWT | TSSOP | PW | 24 | 250 | 367.0 | 367.0 | 38.0 |

MCER004A – JANUARY 1995 – REVISED JANUARY 1997

**JT (R-GDIP-T**)** **CERAMIC DUAL-IN-LINE**

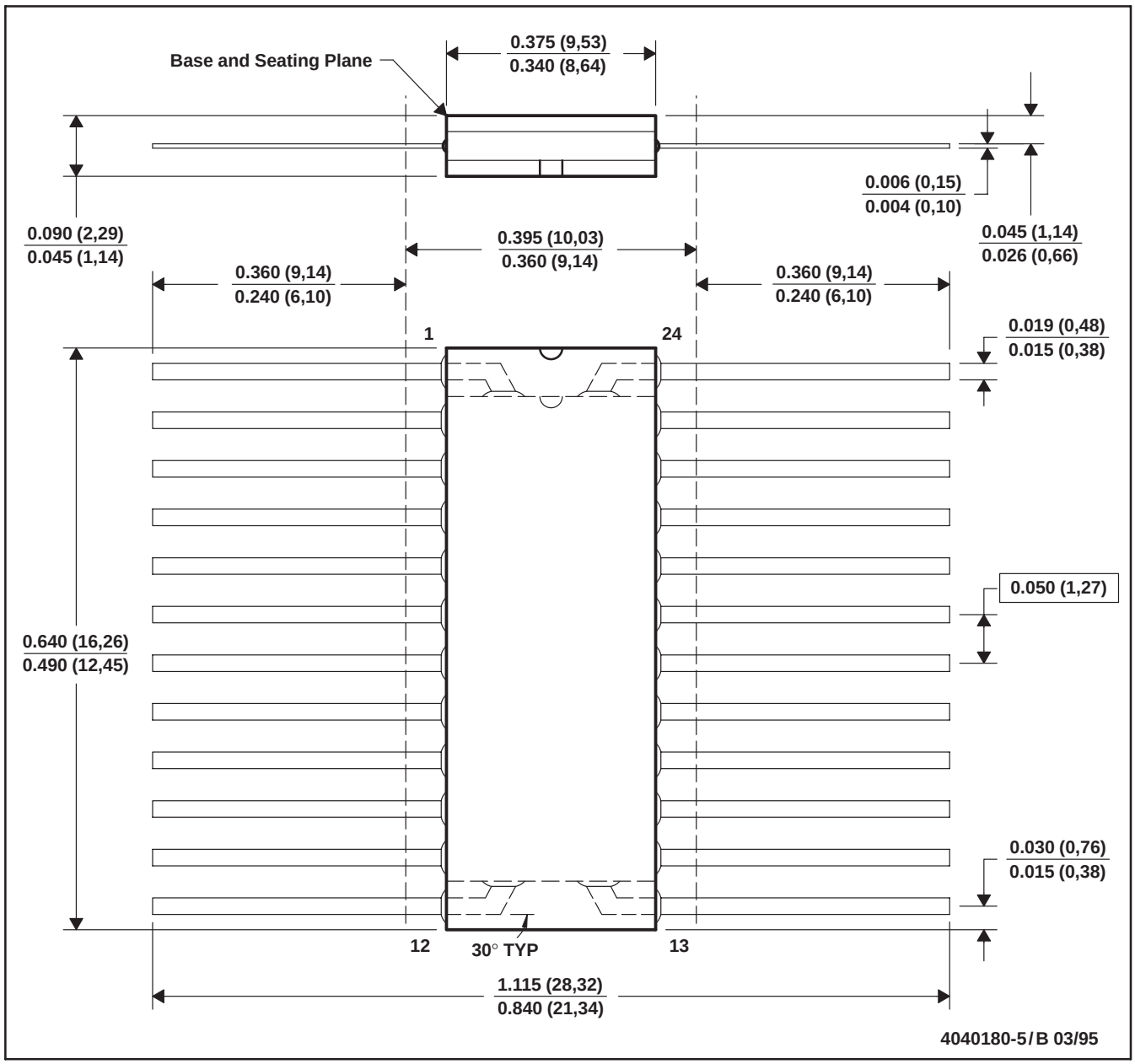
**24 LEADS SHOWN**




| DIM \ PINS ** | 24 | 28 |
|---|---|---|
| A MAX | 1.280 (32,51) | 1.460 (37,08) |
| A MIN | 1.240 (31,50) | 1.440 (36,58) |
| B MAX | 0.300 (7,62) | 0.291 (7,39) |
| B MIN | 0.245 (6,22) | 0.285 (7,24) |

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

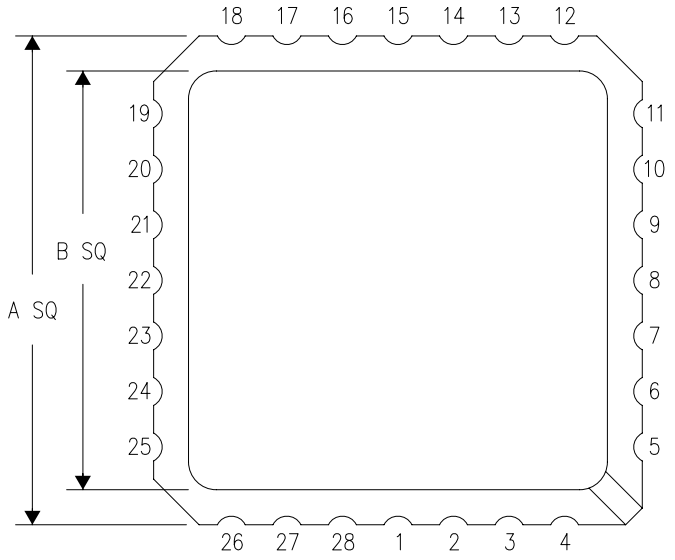
**W (R-GDFP-F24)** **CERAMIC DUAL FLATPACK**



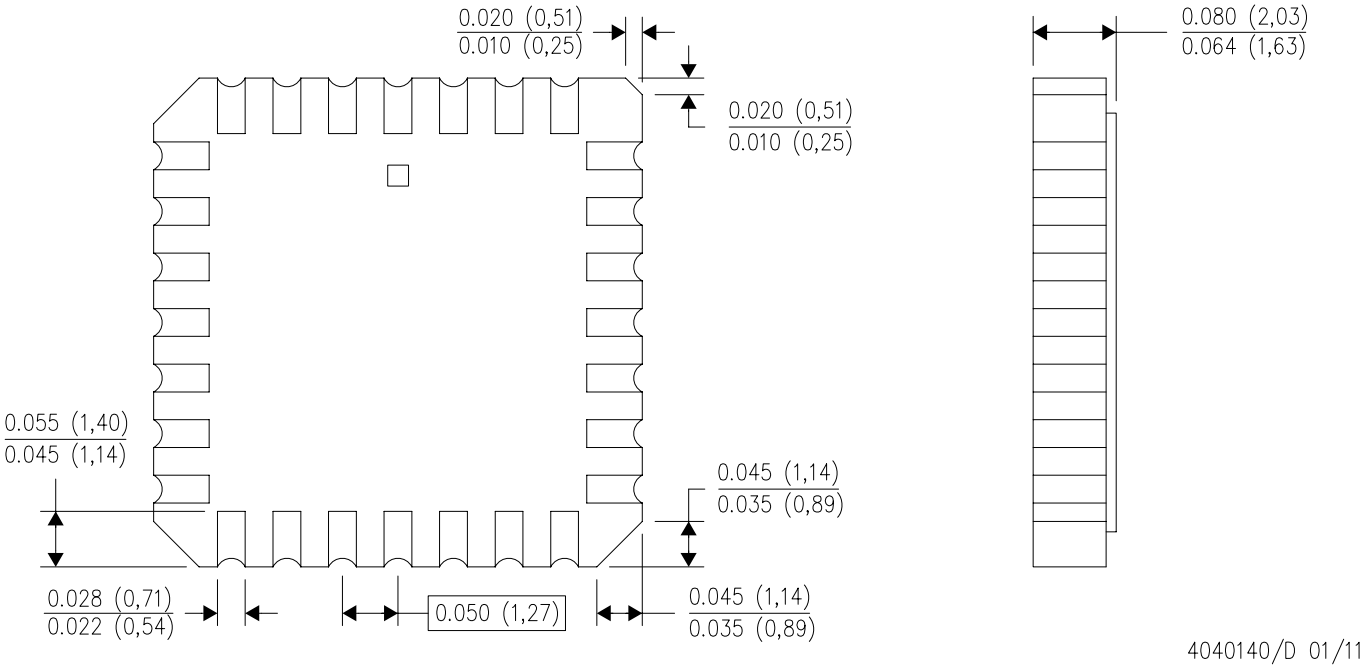

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
E. Index point is provided on cap for terminal identification only.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



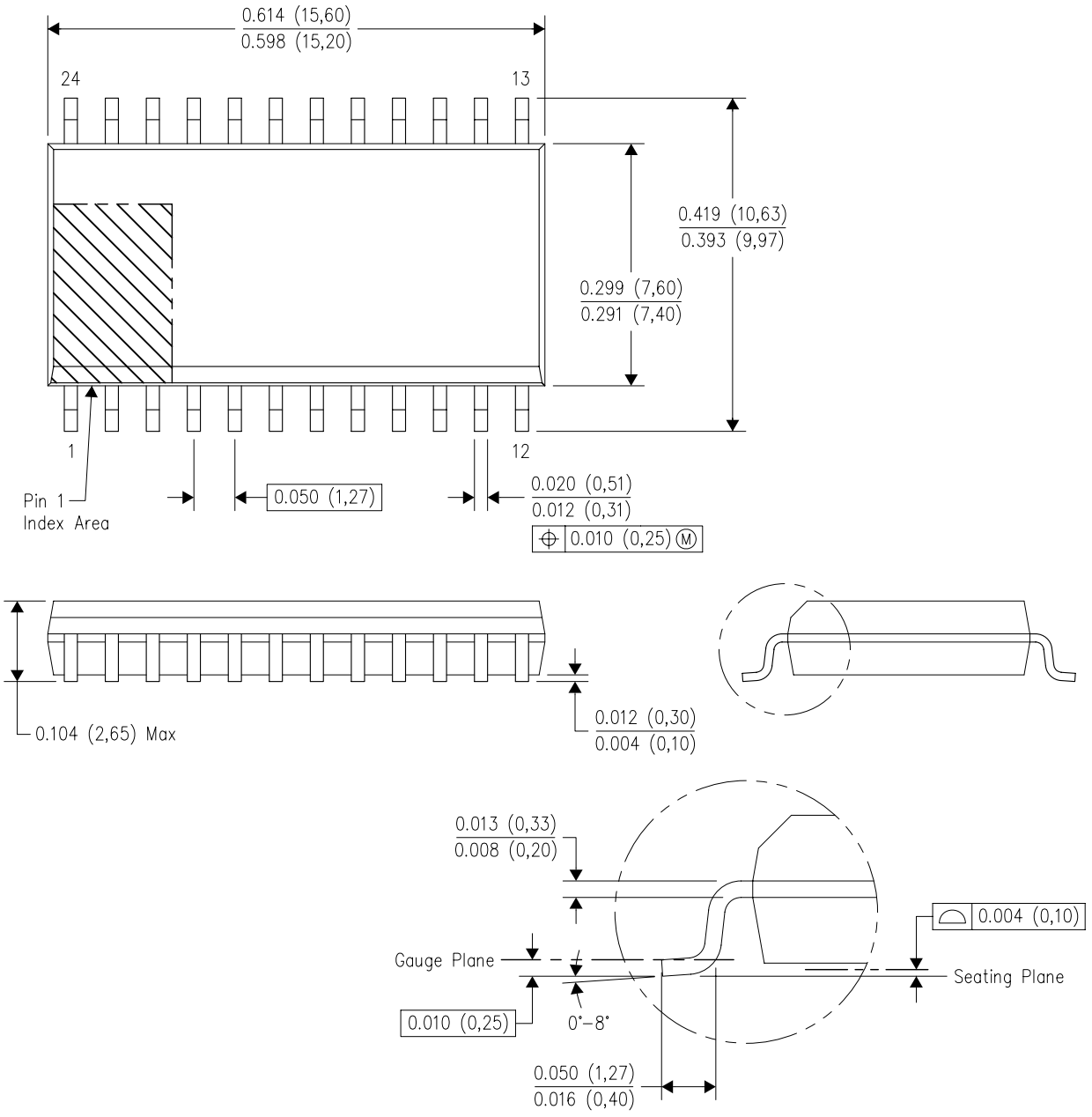

| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |




4040140/D 01/11

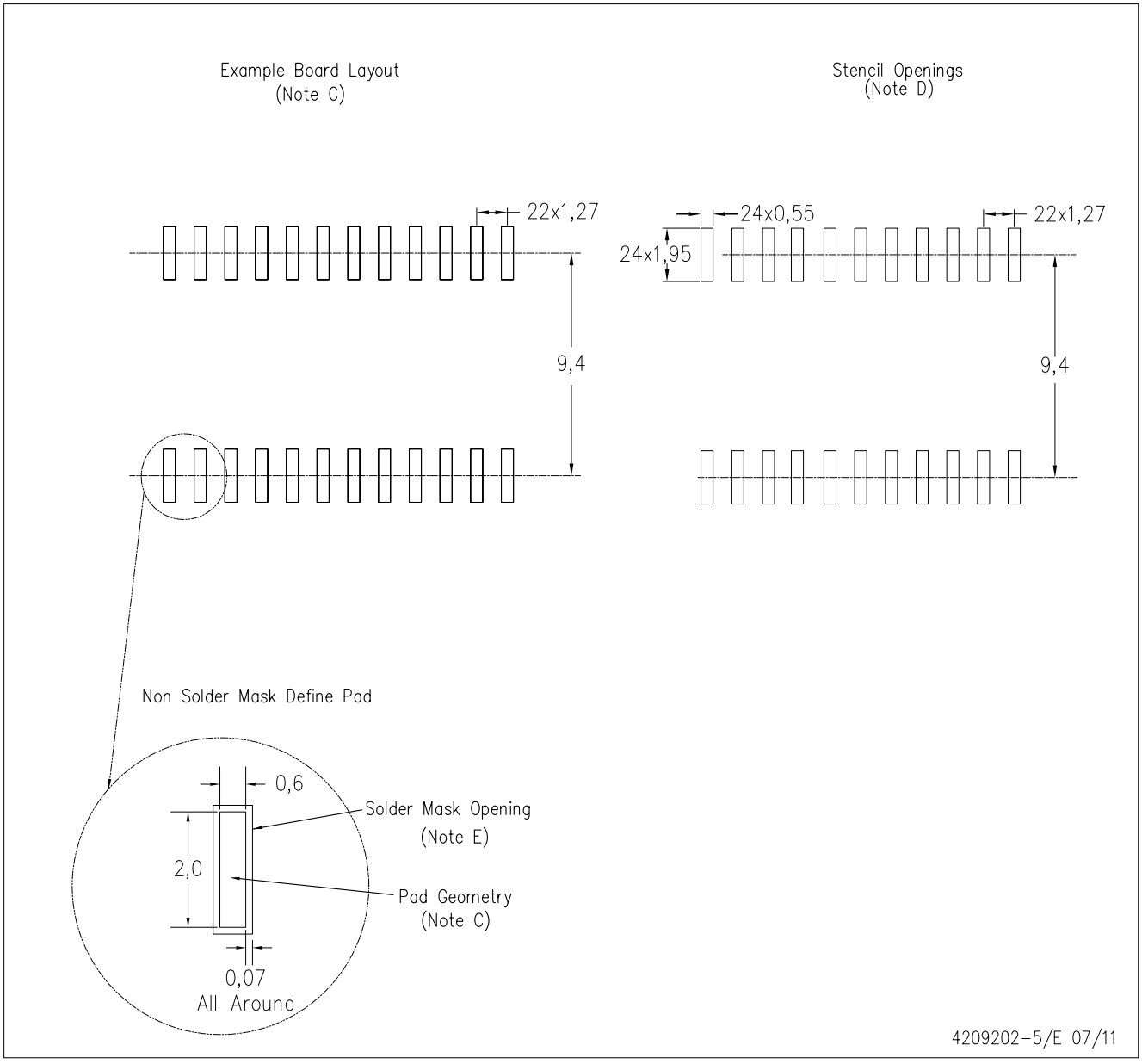
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



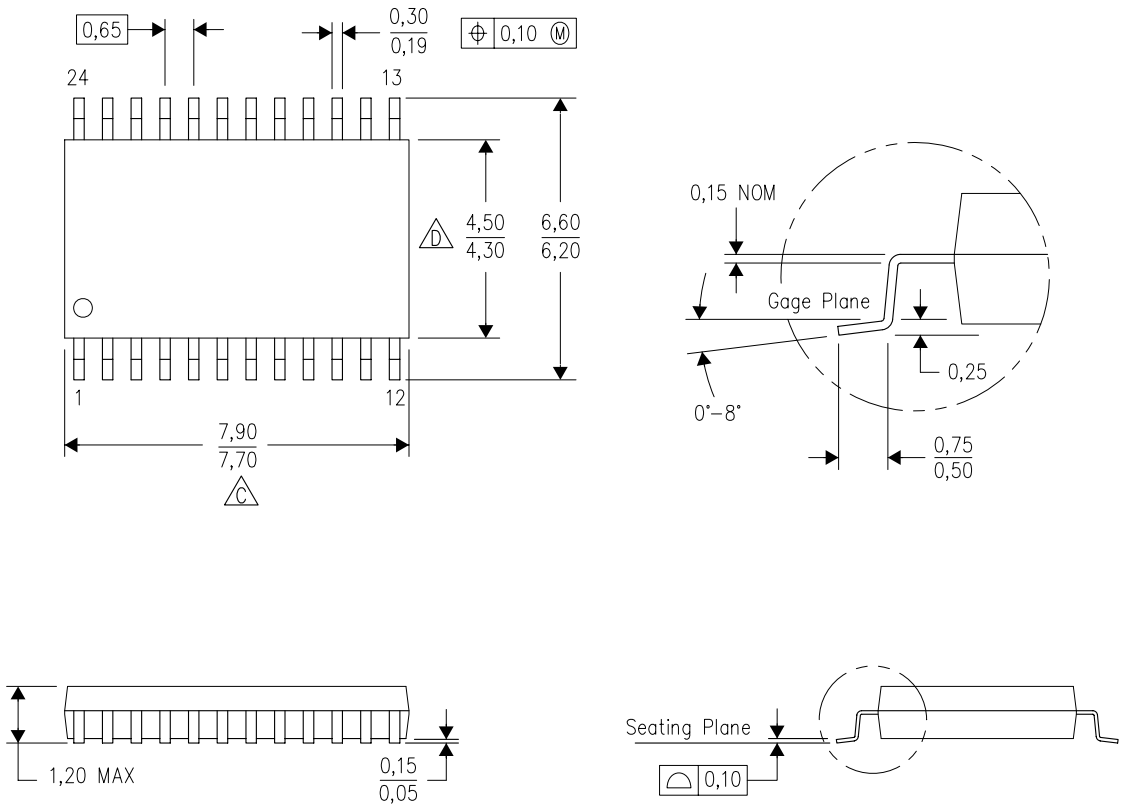

NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

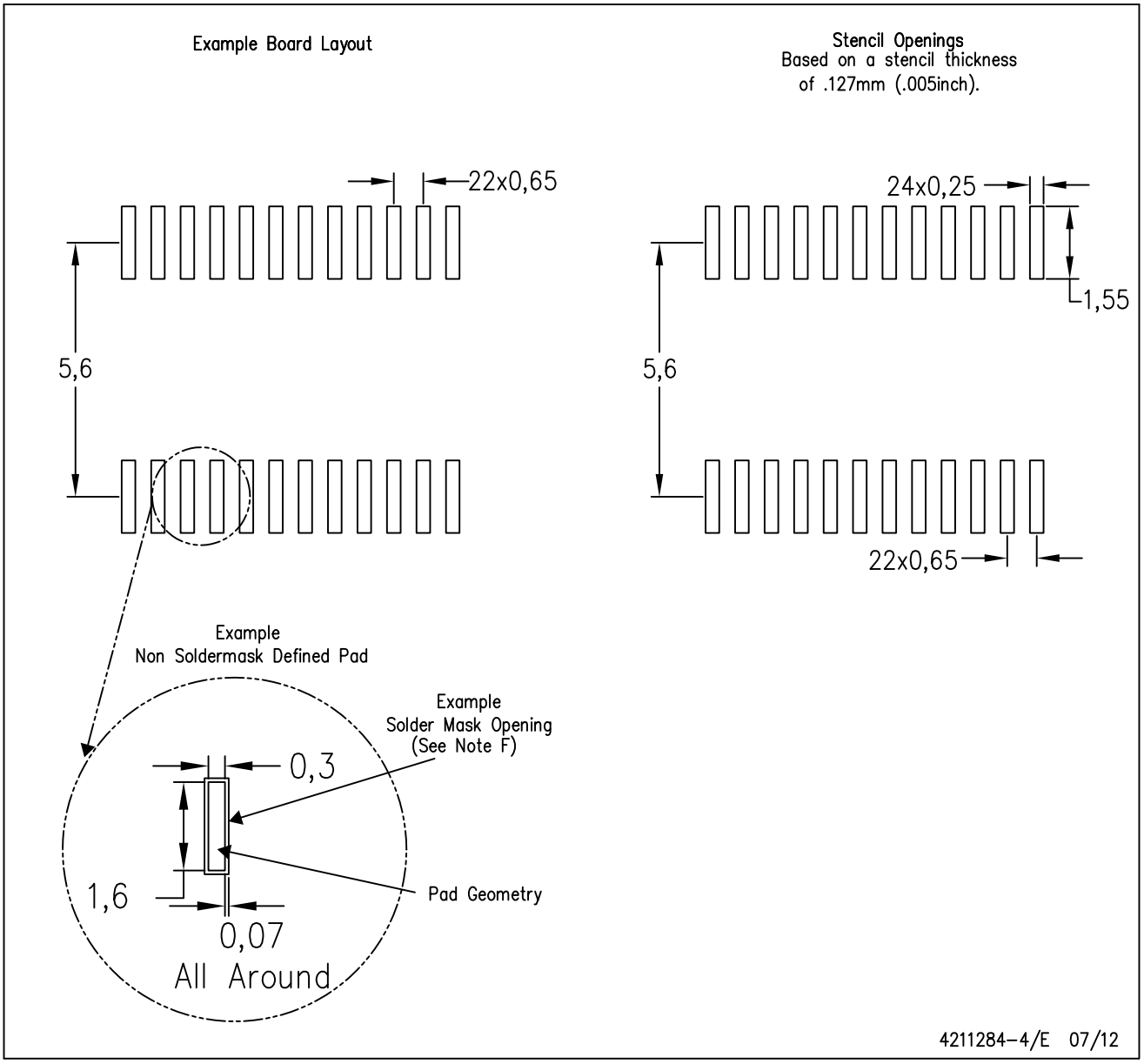
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE




4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE

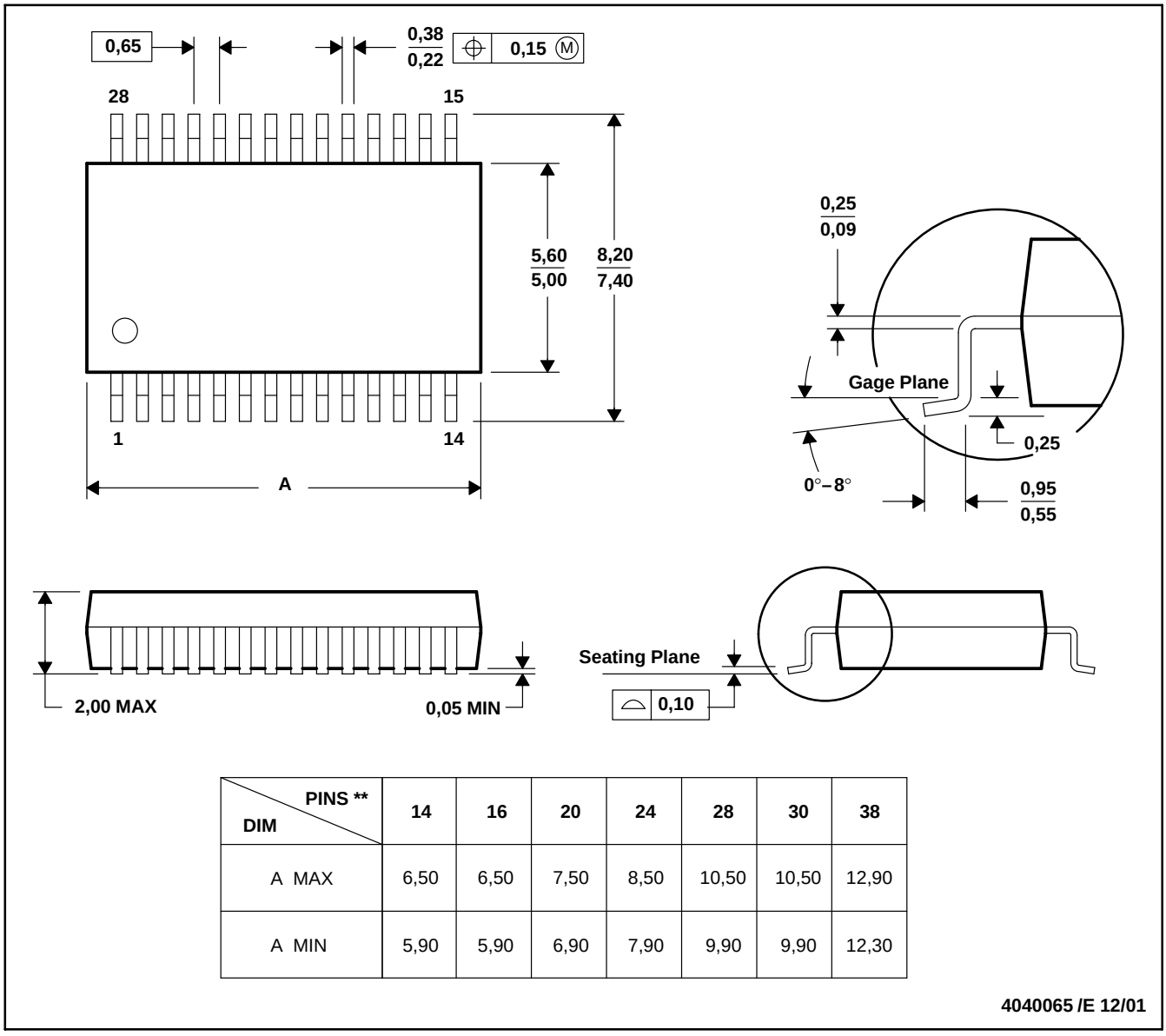



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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