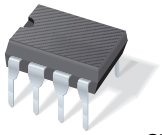




INDUSTRIAL CAN TRANSCEIVER

Check for Samples: SN55HVD251, SN65HVD251

FEATURES

- **Drop-In Improved Replacement for the PCA82C250 and PCA82C251**
- **Bus-Fault Protection of ±36 V**
- **Meets or Exceeds ISO 11898**
- **Signaling Rates(1) Up to 1 Mbps**
- **High Input Impedance Allows up to 120 Nodes on a Bus**
- **Bus Pin ESD Protection Exceeds 14 kV HBM**
- **Unpowered Node Does Not Disturb the Bus**
- **Low-Current Standby Mode — 200 µA Typical**
- **Thermal Shutdown Protection**
- **Glitch-Free Power-Up and Power-Down Bus Protection For Hot-Plugging**
- **DeviceNet Vendor ID # 806**

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in bps (bits per second).

APPLICATIONS

- **CAN Data Buses**
- **Industrial Automation**
- **SAE J1939 Standard Data Bus Interface**
- **NMEA 2000 Standard Data Bus Interface**

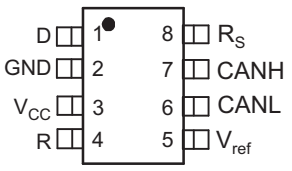
DESCRIPTION

The HVD251 is intended for use in applications employing the Controller Area Network (CAN) serial communication physical layer in accordance with the ISO 11898 Standard. The HVD251 provides differential transmit capability to the bus and differential receive capability to a CAN controller at speeds up to 1 megabits per second (Mbps).

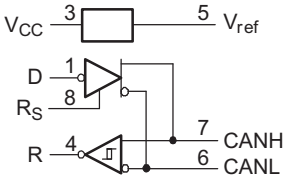
Designed for operation in harsh environments, the device features cross-wire, overvoltage and loss of ground protection to ±36 V. Also featured are overtemperature protection as well as -7 V to 12 V common-mode range, and tolerance to transients of ±200 V. The transceiver interfaces the single-ended CAN controller with the differential CAN bus found in industrial, building automation, and automotive applications.

Rs, pin 8, selects one of three different modes of operation: high-speed, slope control, or low-power mode. The high-speed mode of operation is selected by connecting pin 8 to ground, allowing the transmitter output transistors to switch as fast as possible with no limitation on the rise and fall slope. The rise and fall slope can be adjusted by connecting a resistor to ground at pin 8; the slope is proportional to the pin's output current. Slope control with an external resistor value of 10 kΩ gives ~ 15 V/µs slew rate; 100 kΩ gives ~ 2 V/µs slew rate.

If a high logic level is applied to the Rs pin 8, the device enters a low-current standby mode where the driver is switched off and the receiver remains active. The local protocol controller returns the device to the normal mode when it transmits to the bus.



function diagram
(positive logic)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE	MARKED AS
SN65HVD251D	8-pin Small Outline Integrated Circuit (SOIC)	-40°C to 125°C	VP251
SN65HVD251P	8-pin Dual Inline Package (DIP)	-40°C to 125°C	65HVD251
SN55HVD251DRJ	8-pin Small Outline No-Lead (SON)	-55°C to 125°C	SN55HVD251

ABSOLUTE MAXIMUM RATINGS(1) (2)

			Values
Supply voltage range, V_{CC}			-0.3 V to 7 V
Voltage range at any bus terminal (CANH or CANL)			-36 V to 36 V
Transient voltage per ISO 7637, pulse 1, 2, 3a, 3b		CANH, CANL	±200 V
Input voltage range, V_I (D, Rs, or R)			-0.3 V to V_{CC} + 0.5
Receiver output current, I_O			–10 mA to 10 mA
Electrostatic discharge	Human Body Model (3)	CANH, CANL and GND	14 kV
		All pins	6 kV
	Charged-Device Model (4)	All pins	1 kV
Electrical fast transient/burst	IEC 61000-4-4, Classification B	CANH, CANL	±3 kV
Continuous total power dissipation			(see the Package Dissipation Ratings Table)

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

PACKAGE DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	T_A = 25°C POWER RATING	DERATING FACTOR (1) ABOVE T_A = 25°C	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
SOIC (D)	Low-K(2)	576 mW	4.8 mW/°C	288 mW	96 mW
	High-K(3)	924 mW	7.7 mW/°C	462 mW	154 mW
PDIP (P)	Low-K(2)	888 mW	7.4 mW/°C	444 mW	148 mW
	High-K(3)	1212 mW	10.1 mW/°C	606 mW	202 mW
SON (DRJ)	Low-K(2)	403 mW	4.03 mW/°C	262 mW	100 mW
	High-K (no Vias)(3)	1081 mW	10.8 mW/°C	703 mW	270 mW
	High-K (with Vias)	2793 mW	27.9 mW/°C	1815 mW	698 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.
(3) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

THERMAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
θ_{JB}	Junction-to-board thermal resistance		D		78.7		°C/W
			P		48.9		
			DRJ		73		
θ_{JC}	Junction-to-case thermal resistance		D		44.6		°C/W
			P		66.6		
			DRJ		52		
P_D	Device power dissipation	V_{CC} = 5 V, Tj = 27°C, RL = 60Ω, R_S at 0 V, Input to D a 500-kHz 50% duty cycle square wave			97.7		mW
		V_{CC} = 5.5 V, Tj = 130°C, RL = 60Ω, R_S at 0 V, Input to D a 500-kHz 50% duty cycle square wave			142		mW
T_{SD}	Thermal shutdown junction temperature				165		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		5.5	V
Voltage at any bus terminal (separately or common mode) V_I or V_{IC}		-7 (1)		12	V
High-level input voltage, V_{IH}	D input	0.7 V_{CC}			V
Low-level input voltage, V_{IL}	D input			0.3 V_{CC}	V
Differential input voltage, V_{ID}		-6		6	V
Input voltage to Rs, $V_{I(Rs)}$		0		V_{CC}	V
Input voltage at Rs for standby, $V_{I(Rs)}$		0.75 V_{CC}		V_{CC}	V
Rs wave-shaping resistance		0		100	kΩ
High-level output current, I_{OH}	Driver	-50			mA
	Receiver	-4			
Low-level output current, I_{OL}	Driver			50	mA
	Receiver			4	
Operating free-air temperature, T_A	SN65HVD251	-40		125	°C
	SN55HVD251	–55		125	
Junction temperature, T_J				145	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

SUPPLY CURRENT

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
I_{CC}	Supply current	Standby	Rs at V_{CC}, D at V_{CC}			275	µA
		Dominant	D at 0 V, 60 Ω load, Rs at 0 V			65	mA
		Recessive	D at V_{CC}, no load, Rs at 0 V			14	

(1) All typical values are at 25°C and with a 5-V supply.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	Figure 1 and Figure 2 , D at 0 V Rs at 0 V, T ≥ -40°C	2.75	3.5	4.5	V
		CANL		0.5		2	
$V_{O(R)}$	Bus output voltage (Recessive)	CANH	Figure 1 and Figure 2 , D at 0.7V_{CC}, Rs at 0 V,	2	2.5	3	
		CANL		2	2.5	3	
$V_{OD(D)}$	Differential output voltage (Dominant)		Figure 1 , D at 0 V, Rs at 0 V	1.5	2	3	V
			Figure 3 , D at 0 V, Rs at 0 V, R_{NODE} = 330 Ω	1.2	2	3.1	V
			Figure 3 , D at 0 V, Rs at 0 V, R_{NODE} = 165 Ω, V_{CC} ≥ 4.75 V	1.2	2	3.1	V
$V_{OD(R)}$	Differential output voltage (Recessive)		Figure 1 and Figure 2 , D at 0.7 V_{CC}	-120		12	mV
			D at 0.7 V_{CC}, no load, T ≤ 85°C	-0.5		0.05	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage		Figure 9, Rs at 0 V		600		mV
I_{IH}	High-level input current, D Input		D at 0.7 V_{CC}	-40		0	µA
I_{IL}	Low-level input current, D Input		D at 0.3 V_{CC}	-60		0	µA
$I_{OS(SS)}$	Short-circuit steady-state output current		Figure 11, V_{CANH} at -7 V, CANL Open	-200			mA
			Figure 11, V_{CANH} at 12 V, CANL Open			2.5	
			Figure 11, V_{CANL} at -7 V, CANH Open	-2			
			Figure 11, V_{CANL} at 12 V, CANH Open			200	
C_O	Output capacitance		See receiver input capacitance				
I_{OZ}	High-impedance output current		See receiver input current				
$I_{IRs(s)}$	Rs input current for standby		Rs at 0.75 V_{CC}	-10			µA
$I_{IRs(f)}$	Rs input current for full speed operation		Rs at 0 V	-550		0	µA

(1) All typical values are at 25°C and with a 5-V supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}	Propagation delay time, low-to-high-level output	Figure 4, Rs at 0 V		40	70	ns
		Figure 4, Rs with 10 kΩ to ground		90	125	
		Figure 4, Rs with 100 kΩ to ground		500	800	
t_{pHL}	Propagation delay time, high-to-low-level output	Figure 4, Rs at 0 V		85	125	
		Figure 4, Rs with 10 kΩ to ground		200	260	
		Figure 4, Rs with 100 kΩ to ground		1150	1450	
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)	Figure 4, Rs at 0 V		45	85	
		Figure 4, Rs with 10 kΩ to ground		110	180	
		Figure 4, Rs with 100 kΩ to ground		650	900	
t_r	Differential output signal rise time	Figure 4, Rs at 0 V	35	80	100	
t_f	Differential output signal fall time		35	80	100	
t_r	Differential output signal rise time	Figure 4, Rs with 10 kΩ to ground	100	150	250	
t_f	Differential output signal fall time		100	150	250	
t_r	Differential output signal rise time	Figure 4, Rs with 100 kΩ to ground	600	950	1550	
t_f	Differential output signal fall time		600	950	1550	
t_{en}	Enable time from standby to dominant	Figure 8			0.5	µs

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	Rs at 0 V, (See Table 1)			750	900	mV
V_{IT-}	Negative-going input threshold voltage			500	650		
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})				100		
V_{OH}	High-level output voltage	Figure 6, I_O = -4mA		0.8 V_{CC}			V
V_{OL}	Low-level output voltage	Figure 6, I_O = 4mA				0.2 V_{CC}	V
I_I	Bus input current	CANH or CANL at 12 V	Other bus pin at 0 V, Rs at 0 V, D at 0.7 V_{CC}			600	µA
		CANH or CANL at 12 V, V_{CC} at 0 V				715	
		CANH or CANL at -7 V		-460			
		CANH or CANL at -7 V, V_{CC} at 0 V		-340			
C_I	Input capacitance, (CANH or CANL)	Pin-to-ground, V_I = 0.4 sin (4E6πt) + 0.5 V, D at 0.7 V_{CC}			20		pF
C_{ID}	Differential input capacitance	Pin-to-pin, V_I = 0.4 sin (4E6πt) + 0.5 V, D at 0.7 V_{CC}			10		pF
R_{ID}	Differential input resistance	D at 0.7 V_{CC}, Rs at 0 V		40		100	kΩ
R_{IN}	Input resistance, (CANH or CANL)	D at 0.7 V_{CC}, Rs at 0 V		20		50	kΩ
	Receiver noise rejection	See Figure 13					

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}	Propagation delay time, low-to-high-level output	Figure 6		35	50	ns
t_{pHL}	Propagation delay time, high-to-low-level output			35	50	
$t_{sk(p)}$	Pulse skew ($\|t_{pHL} - t_{pLH}\|$)				20	
t_r	Output signal rise time			2	4	
t_f	Output signal fall time			2	4	
$t_{p(sb)}$	Propagation delay time in standby	Figure 12, Rs at V_{CC}			500	

VREF-PIN CHARACTERISTICS

over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Reference output voltage	-5 µA < I_O < 5 µA	0.45 V_{CC}		0.55 V_{CC}	V
		-50 µA < I_O < 50 µA	0.4 V_{CC}		0.6 V_{CC}	

DEVICE SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{loop1}	Total loop delay, driver input to receiver output, recessive to dominant	Figure 10, Rs at 0 V		60	100	ns
		Figure 10, Rs with 10 kΩ to ground		100	150	
		Figure 10, Rs with 100 kΩ to ground		440	800	
t_{loop2}	Total loop delay, driver input to receiver output, dominant to recessive	Figure 10, Rs at 0 V		115	150	ns
		Figure 10, Rs with 10 kΩ to ground		235	290	
		Figure 10, Rs with 100 kΩ to ground		1070	1450	
t_{loop2}	Total loop delay, driver input to receiver output, dominant to recessive	Figure 10, Rs at 0 V, V_{CC} from 4.5 V to 5.1 V,		105	145	ns

PARAMETER MEASUREMENT INFORMATION

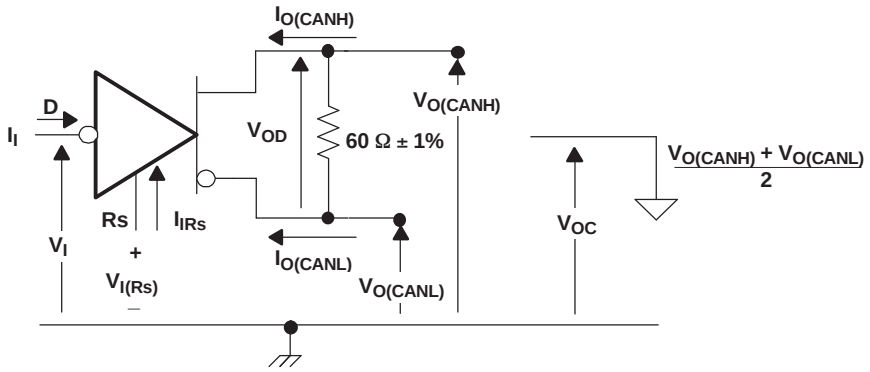


Figure 1. Driver Voltage, Current, and Test Definition

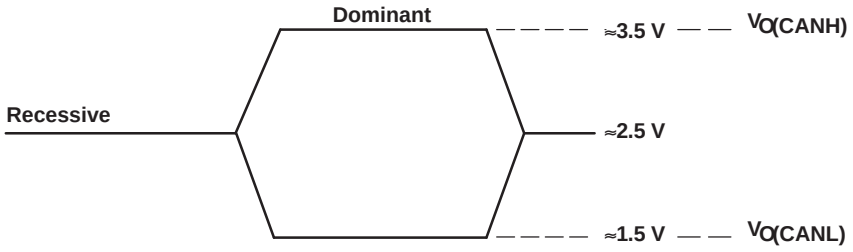


Figure 2. Bus Logic State Voltage Definitions

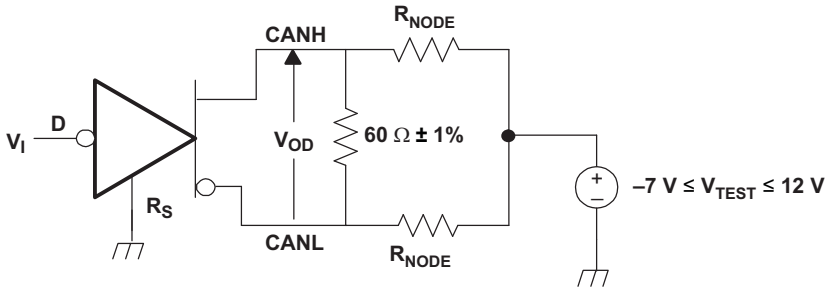


Figure 3. Driver V_{OD}

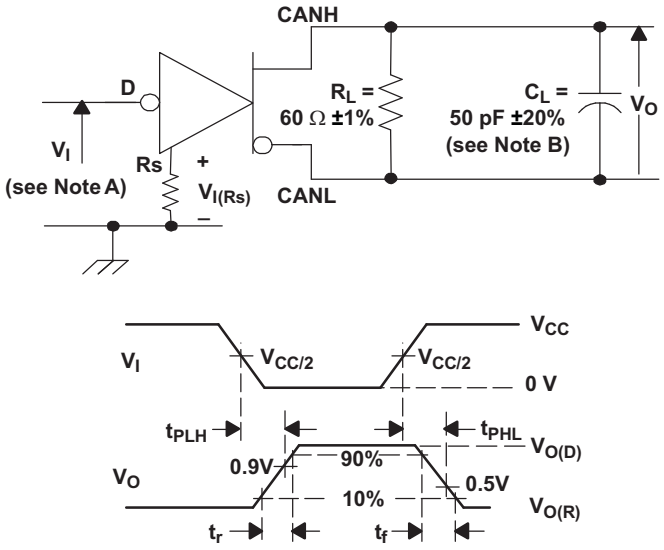


Figure 4. Driver Test Circuit and Voltage Waveforms

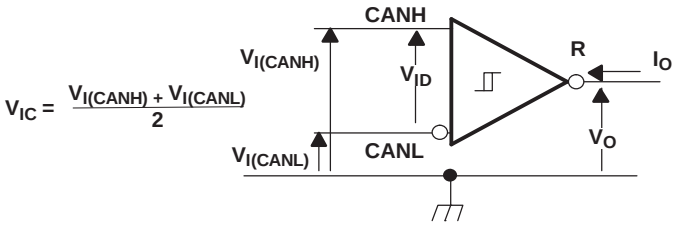
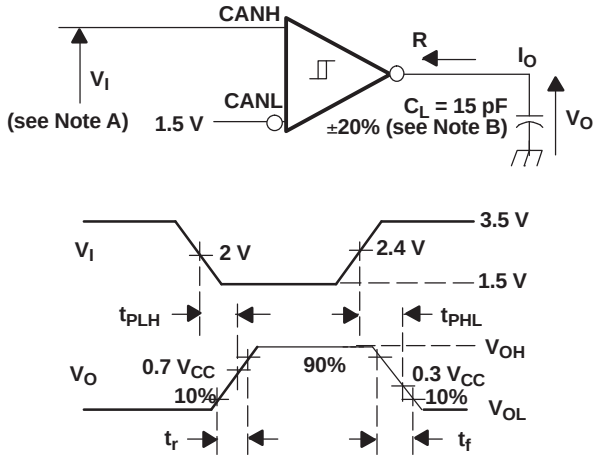


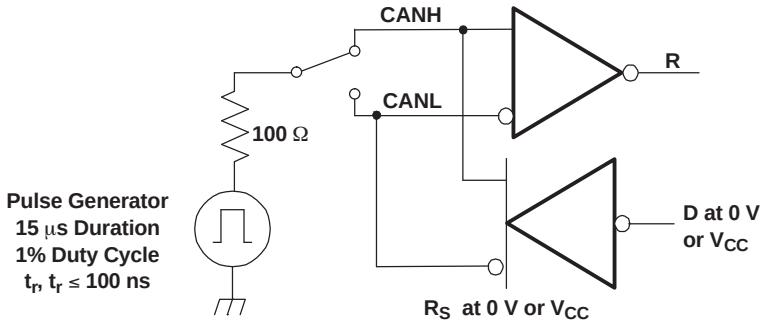
Figure 5. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 6. Receiver Test Circuit and Voltage Waveforms



A. This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 7. Test Circuit, Transient Overvoltage Test

Table 1. Receiver Characteristics Over Common Mode Voltage

INPUT		DIFFERENTIAL INPUT	OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
12 V	11.1 V	900 mV	L	V_{OL}
-6.1 V	-7 V	900 mV	L	
-1 V	-7 V	6 V	L	
12 V	6 V	6 V	L	
-6.5 V	-7 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
-7 V	-1 V	6 V	H	
6 V	12 V	6 V	H	
open	open	X	H	

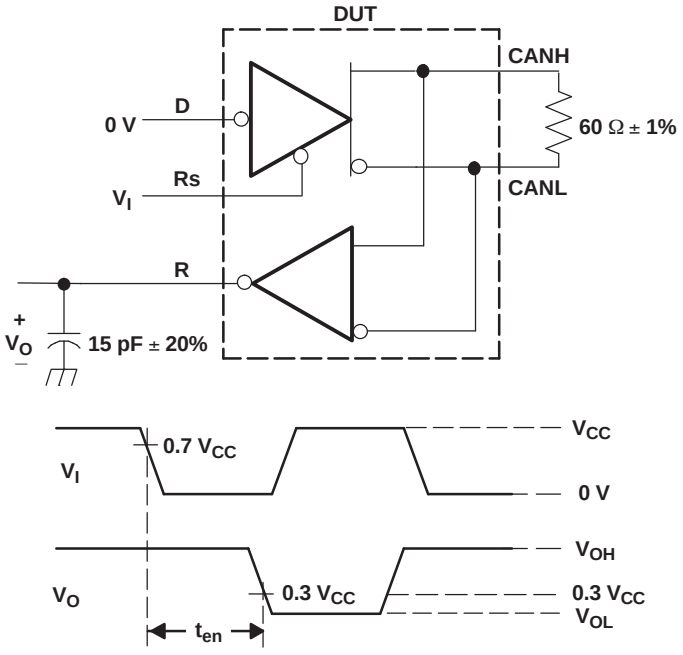
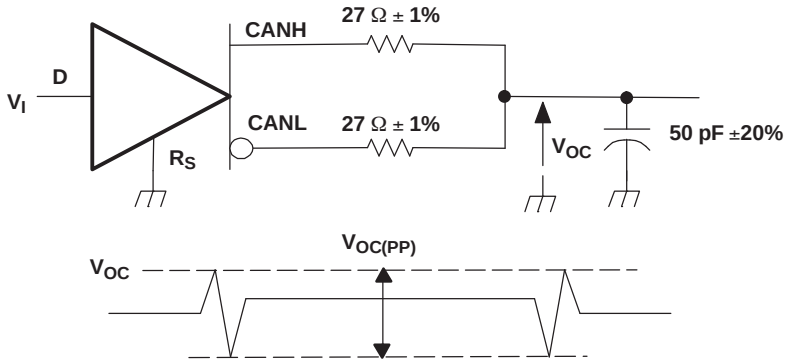


Figure 8. t_{en} Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50Ω.

Figure 9. Peak-to-Peak Common Mode Output Voltage

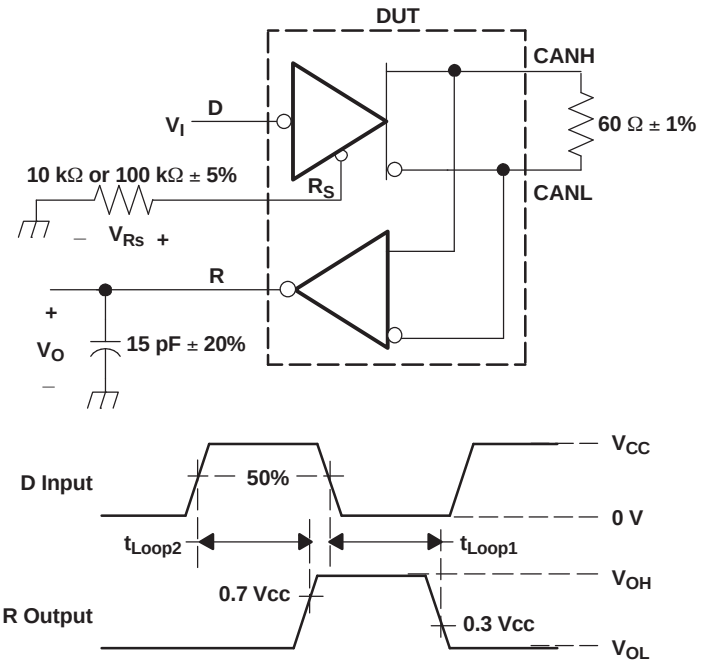


Figure 10. t_{LOOP} Test Circuit and Voltage Waveforms

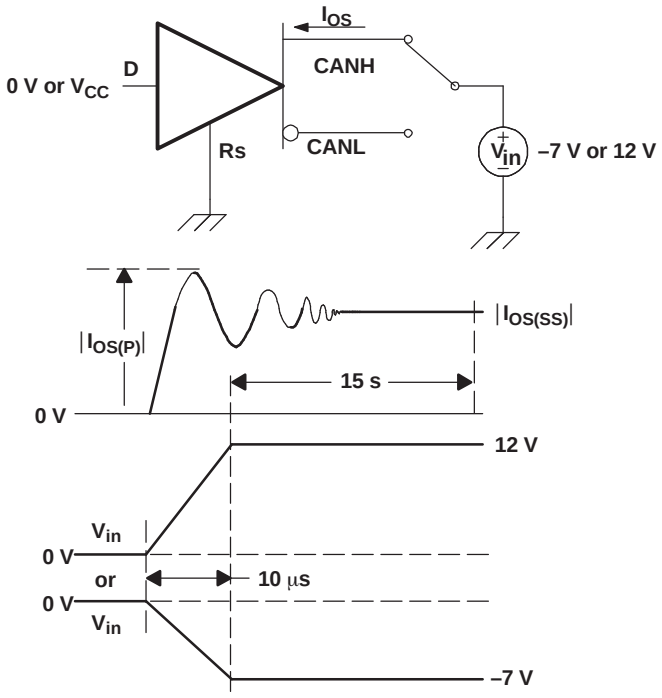
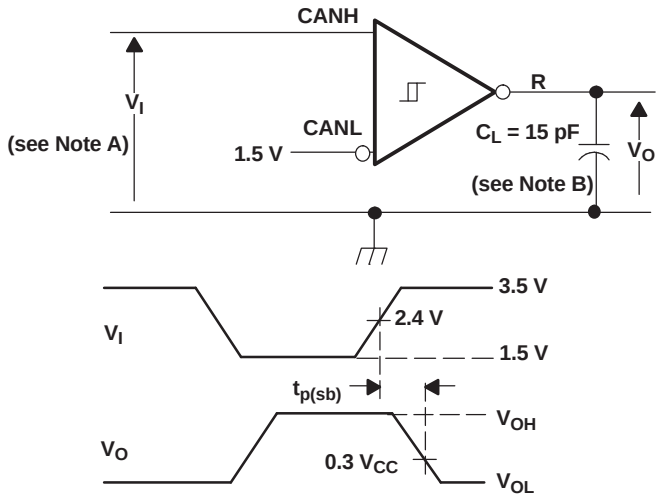


Figure 11. Driver Short-Circuit Test

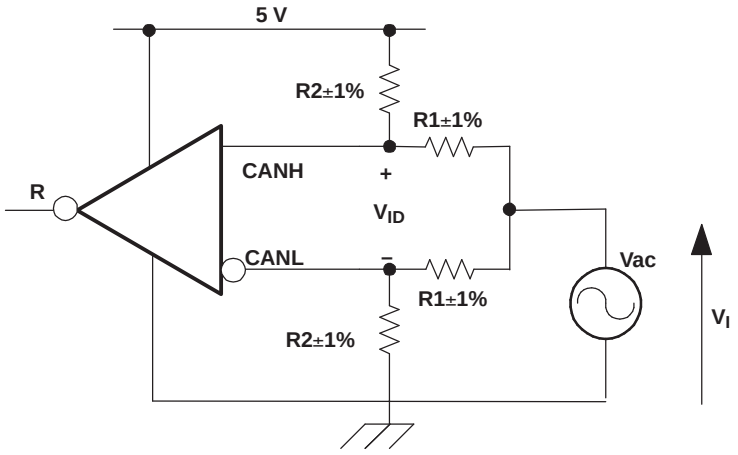


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50 Ω.

B. CL includes instrumentation and fixture capacitance within ±20%.

Figure 12. Receiver Propagation Delay in Standby Test Circuit and Waveform

DEVICE INFORMATION



V_{ID}	R1	R2
500 mV	50 Ω	450 Ω
900 mV	50 Ω	227 Ω

A. All input pulses are supplied by a generator having the following characteristics: f_{IN} < 1.5 MHz, T_A = 25°C, V_{CC} = 5 V.

B. The receiver output should not change state during application of the common-mode input waveform.

Figure 13. Common-Mode Input Voltage Rejection Test

FUNCTION TABLES

Table 2. DRIVER

INPUTS	Voltage at R_S, V_{Rs}	OUTPUTS		BUS STATE
D		CANH	CANL	
L	V_{Rs} < 1.2 V	H	L	Dominant
H	V_{Rs} < 1.2 V	Z	Z	Recessive
Open	X	Z	Z	Recessive
X	V_{Rs} > 0.75 V_{CC}	Z	Z	Recessive
X	Open	Z	Z	Recessive

Table 3. RECEIVER

DIFFERENTIAL INPUTS [V_{ID} = V(CANH) - V(CANL)]	OUTPUT R(1)
V_{ID} ≥ 0.9 V	L
0.5V < V_{ID} < 0.9 V	?
V_{ID} ≤ 0.5 V	H
Open	H

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

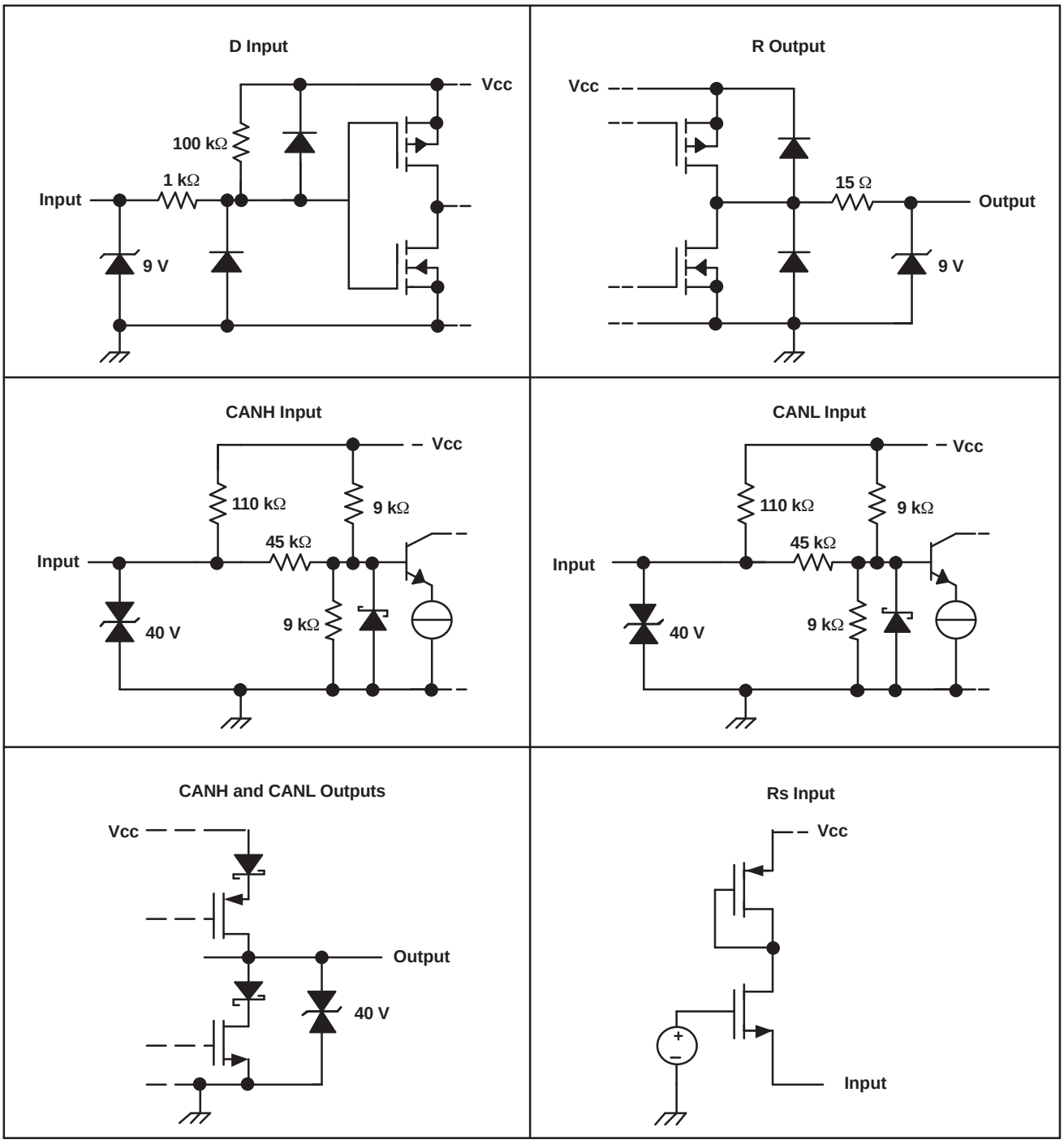


Figure 14. Equivalent Input and Output Schematic Diagrams

TYPICAL CHARACTERISTICS

RECESSIVE-TO-DOMINANT LOOP DELAY vs FREE-AIR TEMPERATURE

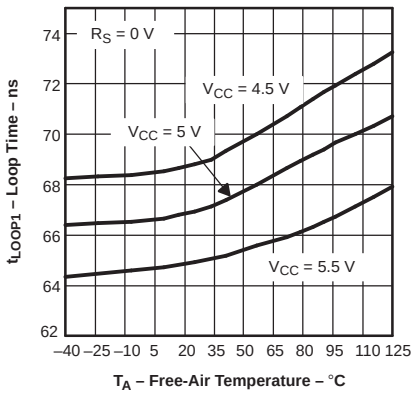


Figure 15.

DOMINANT-TO-RECESSIVE LOOP DELAY vs FREE-AIR TEMPERATURE

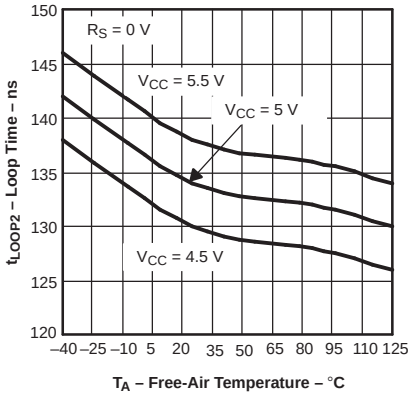


Figure 16.

SUPPLY CURRENT (RMS) vs SIGNALING RATE

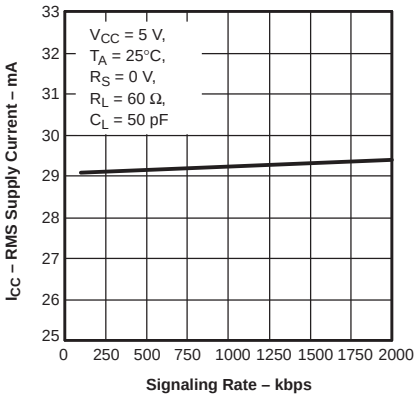


Figure 17.

DRIVER OUTPUT VOLTAGE vs OUTPUT CURRENT

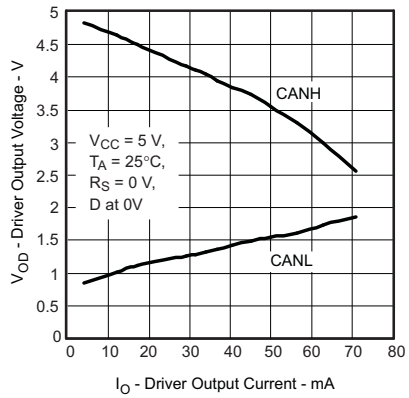


Figure 18.

DRIVER DRIFFERENTIAL OUTPUT VOLTAGE vs OUTPUT CURRENT

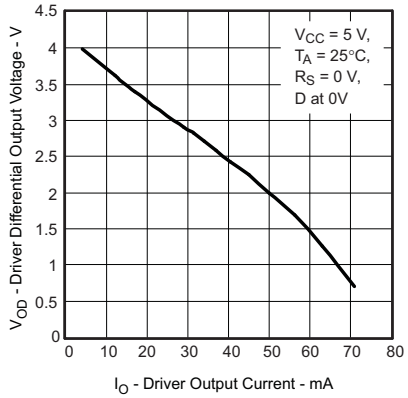


Figure 19.

DOMINANT DIFFERENTIAL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

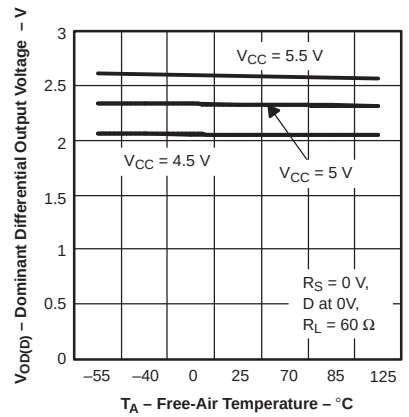


Figure 20.

DRIVER OUTPUT CURRENT vs SUPPLY VOLTAGE

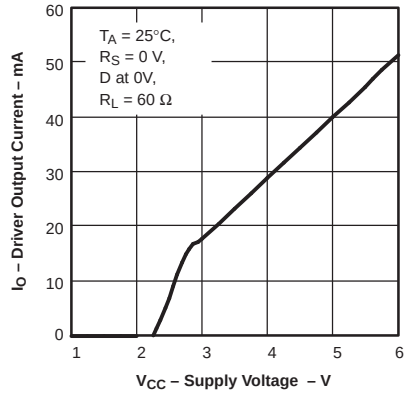


Figure 21.

DIFFERENTIAL OUTPUT TRANSITION TIME vs SLOPE RESISTANCE (Rs)

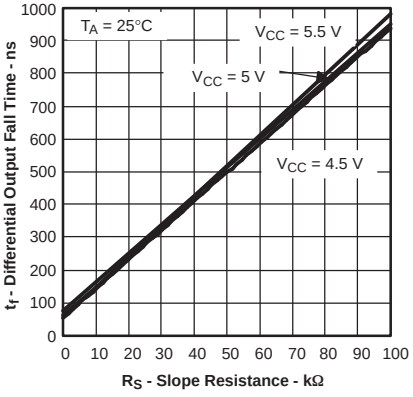


Figure 22.

INPUT RESISTANCE MATCHING vs FREE-AIR TEMPERATURE

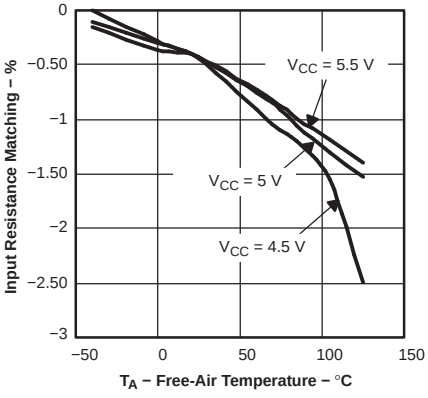


Figure 23.

APPLICATION INFORMATION

The basics of bus arbitration require that the receiver at the sending node designate the first bit as dominant or recessive after the initial wave of the first bit of a message travels to the most remote node on a network and back again. Typically, this *sample* is made at 75% of the bit width, and within this limitation, the maximum allowable signal distortion in a CAN network is determined by network electrical parameters.

Factors to be considered in network design include the 5 ns/m propagation delay of typical twisted-pair bus cable; signal amplitude loss due to the loss mechanisms of the cable; and the number, length, and spacing of drop-lines (stubs) on a network. Under strict analysis, variations among the different oscillators in a system must also be accounted for with adjustments in signaling rate and stub & bus length. Table 4 lists the maximum signaling rates achieved with the SN65HVD251 in high-speed mode with several bus lengths of category-5, shielded twisted-pair (CAT 5 STP) cable.

Table 4. Maximum Signaling Rates for Various Cable Lengths

BUS LENGTH (m)	SIGNALING RATE (kbps)
30	1000
100	500
250	250
500	125
1000	62.5

The ISO 11898 standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m with a maximum of 30 nodes. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes on a bus. (Note: Non-standard application may come with a trade-off in signaling rate.) A bus with a large number of nodes requires a transceiver with high input impedance such as the HVD251.

The Standard specifies the interconnect to be a single twisted-pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Zo). Resistors equal to the characteristic impedance of the line terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines connect nodes to the bus and should be kept as short as possible to minimize signal reflections.

Connectors, while not specified by the ISO 11898 standard, should have as little effect as possible on standard operating parameters such as capacitive loading. Although unshielded cable is used in many applications, data transmission circuits employing CAN transceivers are usually used in applications requiring a rugged interconnection with a wide common-mode voltage range. Therefore, shielded cable is recommended in these electronically harsh environments, and when coupled with the –2-V to 7-V common-mode range of tolerable ground noise specified in the standard, helps to ensure data integrity. The HVD251 extends data integrity beyond that of the standard with an extended –7-V to 12-V range of common-mode operation.

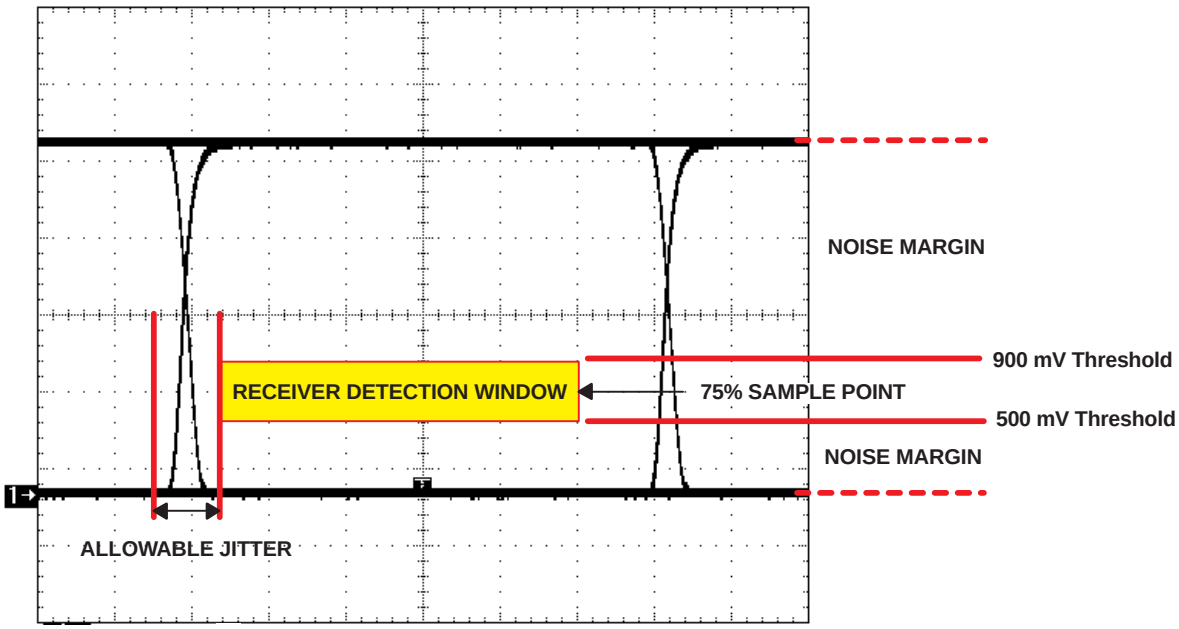


Figure 24. Typical CAN Differential Signal Eye-Pattern

An eye pattern is a useful tool for measuring overall signal quality. As displayed in Figure 24, the differential signal changes logic states in two places on the display, producing an *eye*. Instead of viewing only one logic crossing on the scope, an entire *bit* of data is brought into view. The resulting eye pattern includes all effects of systemic and random distortion, and displays the time during which a signal may be considered valid.

The height of the eye above or below the receiver threshold voltage level at the sampling point is the noise margin of the system. Jitter is typically measured at the differential voltage zero-crossing during the logic state transition of a signal. Note that jitter present at the receiver threshold voltage level is considered by some to be a more effective representation of the jitter at the input of a receiver.

As the sum of skew and noise increases, the eye closes and data is corrupted. Closing the width decreases the time available for accurate sampling, and lowering the height enters the 900 mV or 500 mV threshold of a receiver.

Different sources induce noise onto a signal. The more obvious noise sources are the components of a transmission circuit themselves; the signal transmitter, traces & cables, connectors, and the receiver. Beyond that, there is a termination dependency, cross-talk from clock traces and other proximity effects, VCC and ground bounce, and electromagnetic interference from near-by electrical equipment.

The balanced receiver inputs of the HVD251 mitigate most sources of signal corruption, and when used with a quality shielded twisted-pair cable, help meet data integrity.

Typical Application

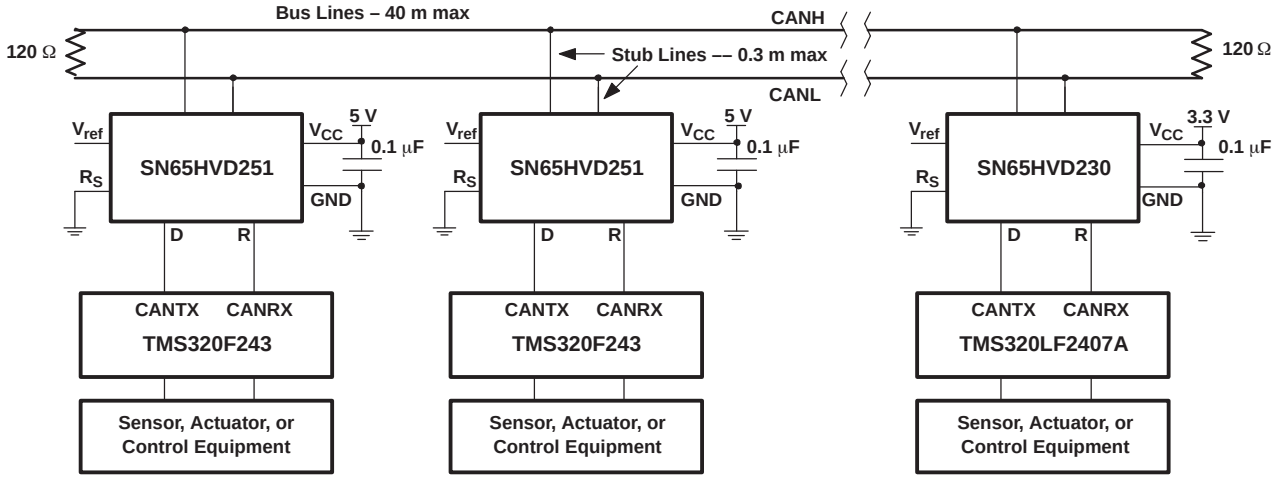


Figure 25. Typical HVD251 Application

REVISION HISTORY

Changes from Original (November 2002) to Revision A **Page**

- Changed multiple items within the document. 1

Changes from Revision A (September 2003) to Revision B **Page**

- Changed the front page format. 1
- Changed DESCRIPTION text From: and tolerance to transients of ±50 V To: and tolerance to transients of ±200 V 1

Changes from Revision B (September 2003) to Revision C **Page**

- Changed the front page format. 1
- Added the SN65HVD251P Package option to the Ordering Information table. 2
- Changed the ABSOLUTE MAXIMUM POWER DISSIPATION RATINGS table values 2
- Changed the THERMAL CHARACTERISTICS table values 3
- Changed Junction temperature, T_J - SOIC Package MAX value From 150°C To: 145°C 3

Changes from Revision C (September 2005) to Revision D **Page**

- Added device SN55HVD251 1
- Added the DRJ Package. 1
- Changed the data sheet title From: CAN TRANSCEIVER To: INDUSTRIAL CAN TRANSCEIVER 1
- Deleted APPLICATIONS bullets: DeviceNet™ Data Buses, Smart Distributed Systems (SDS™), and ISO 11783 Standard Data Bus Interface 1
- Deleted last paragraph from the DESCRIPTION - "The HVD251 may be used..." 1
- Added the SN55HVD251DRJ Package to the Ordering Information table. 2
- Added Electrical fast transient/burst to the Abs Max Ratings table 2
- Changed table title From: ABSOLUTE MAXIMUM POWER DISSIPATION RATINGS To: PACKAGE DISSIPATION RATINGS 2
- Added the SON (DRJ) option to the PACKAGE DISSIPATION RATINGS table 2
- Added DRJ to the Junction-to-board thermal resistance 3
- Added DRJ to the Junction-to-case thermal resistance 3
- Deleted the condition - over recommended operating conditions (unless otherwise noted). From the RECOMMENDED OPERATING CONDITIONS table 3
- Added SN55HVD251 to the Operating free-air temperature, T_A in the ROC table 3
- Added the SUPPLY CURRENT table 3
- Deleted ICC - Supply current from the DRIVER ELECTRICAL CHARACTERISTICS 4
- Added T ≥ -40°C to $V_{O(D)}$ Test Conditions in the DRIVER ELECTRICAL CHARACTERISTICS 4
- Added R_{NODE} = 330 Ω to Differential output voltage (Dominant) (second line of Test Conditions) in the DRIVER ELECTRICAL table 4
- Added a third line of Test Conditions to Differential output voltage (Dominant) in the DRIVER ELECTRICAL table 4
- Added T ≤ 85°C to $V_{OD(R)}$ Test Conditions in the DRIVER ELECTRICAL CHARACTERISTICS 4
- Added TYP values to the Differential output signal rise and fall times in the DRIVER SWITCHING CHARACTERISTIC table 4
- Deleted ICC - Supply current from the RECEIVER ELECTRICAL CHARACTERISTICS 5
- Added Receiver noise rejection row to the RECEIVER ELECTRICAL CHARACTERISTIC table 5
- Changed Figure 3 - Driver V_{OD}, lable R_{NODE} was 330Ω±1% 6

- Changed Table 1 header From: MEASURED To: DIFFERENTIAL INPUT 8
- Added Note B to Figure 13 11
- Added a row (X Open) to Table 2 - Driver 11
- Changed Figure 15 title From: $t_{LOOP1-LOOP}$ TIME To: RECESSIVE-TO-DOMINANT LOOP DELAY 13
- Changed Figure 16 title From: $t_{LOOP2-LOOP}$ TIME To: DOMINANT-TO-RECESSIVE LOOP DELAY 13
- Changed Figure 18 From: DRIVER LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE To: DRIVER OUTPUT VOLTAGE vs OUTPUT CURRENT 13
- Changed Figure 19 From: DRIVER HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE To: DRIVER DRIFFERENTIAL OUTPUT VOLTAGE vs OUTPUT CURRENT 13
- Changed Figure 22 title From: DIFFERENTIAL OUTPUT FALL TIME To: DIFFERENTIAL OUTPUT TRANSITION TIME 13

Changes from Revision D (February 2010) to Revision E **Page**

- Deleted device number SN65HVD251DR, added the Temperature Range to the ORDERING INFORMATION table 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN55HVD251DRJR	ACTIVE	SON	DRJ	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65HVD251D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD251DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD251DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD251DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD251P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65HVD251PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

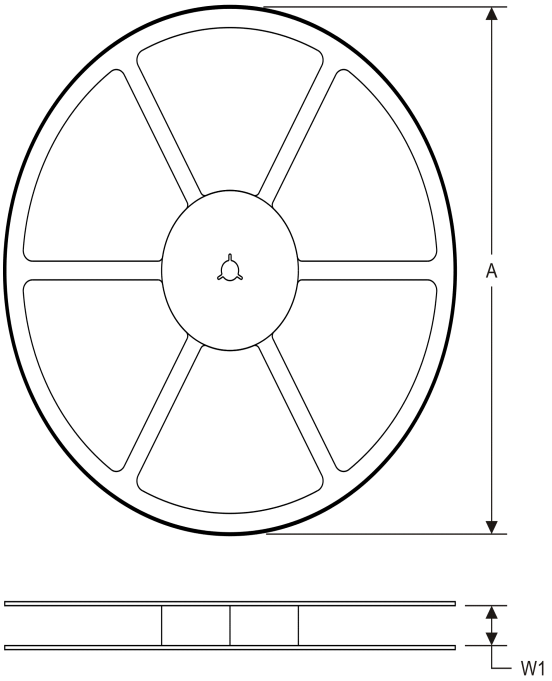
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF SN65HVD251 :
- Automotive: SN65HVD251-Q1

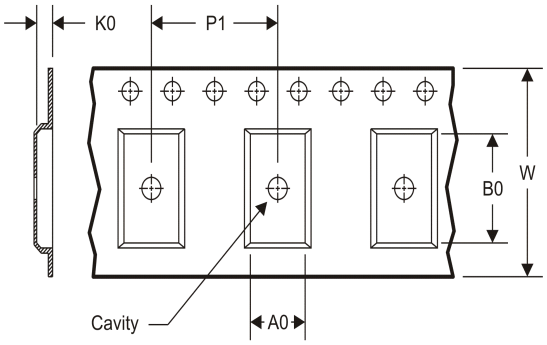
NOTE: Qualified Version Definitions:
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



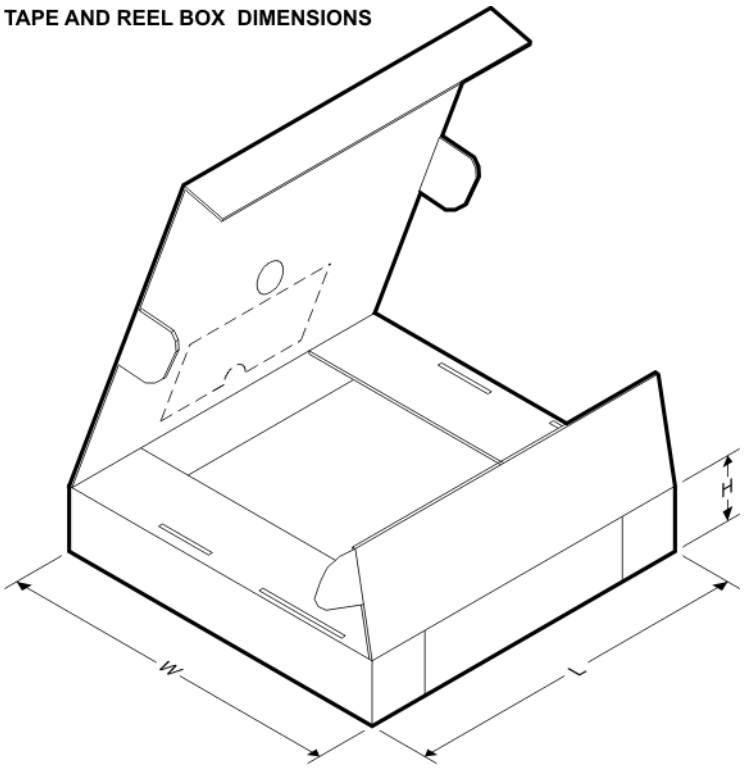
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN55HVD251DRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN65HVD251DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

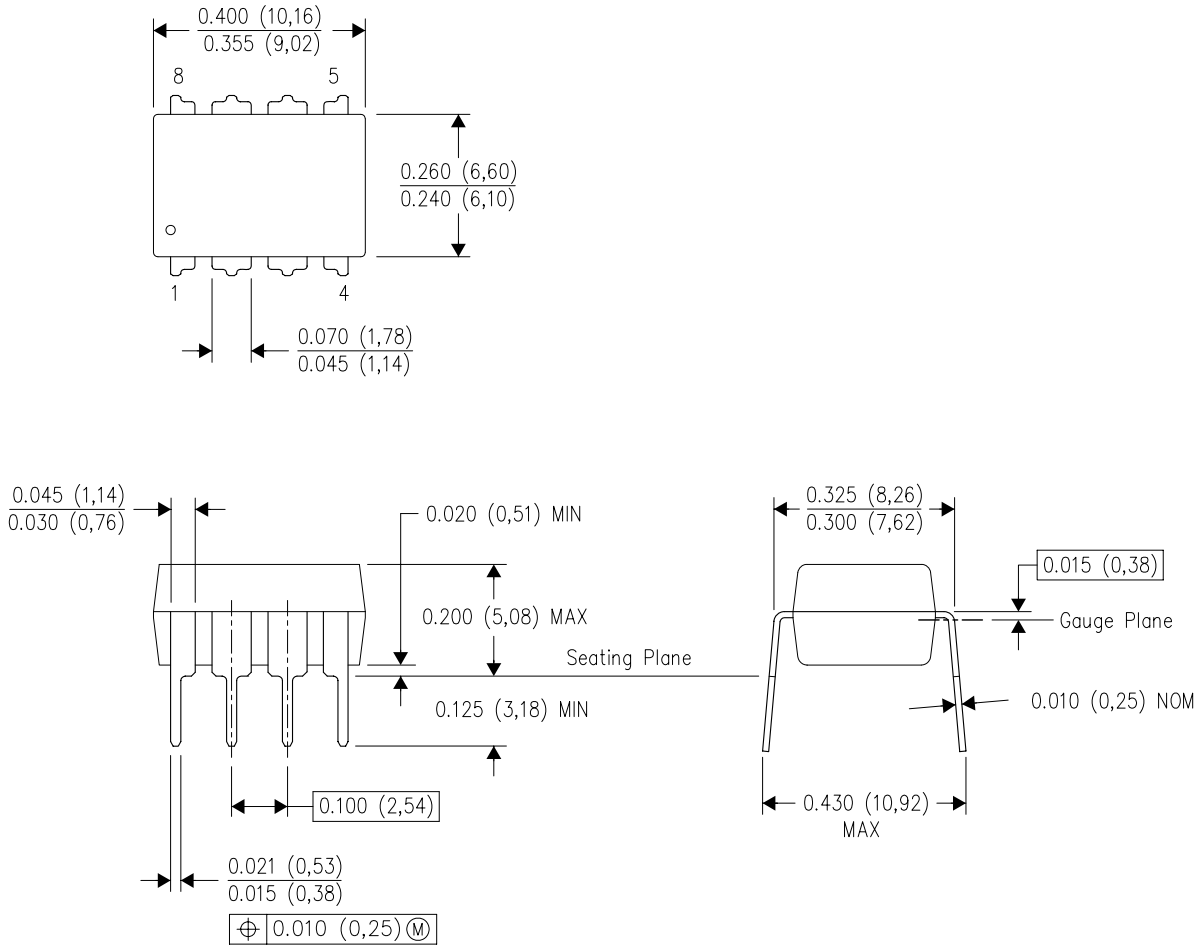
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

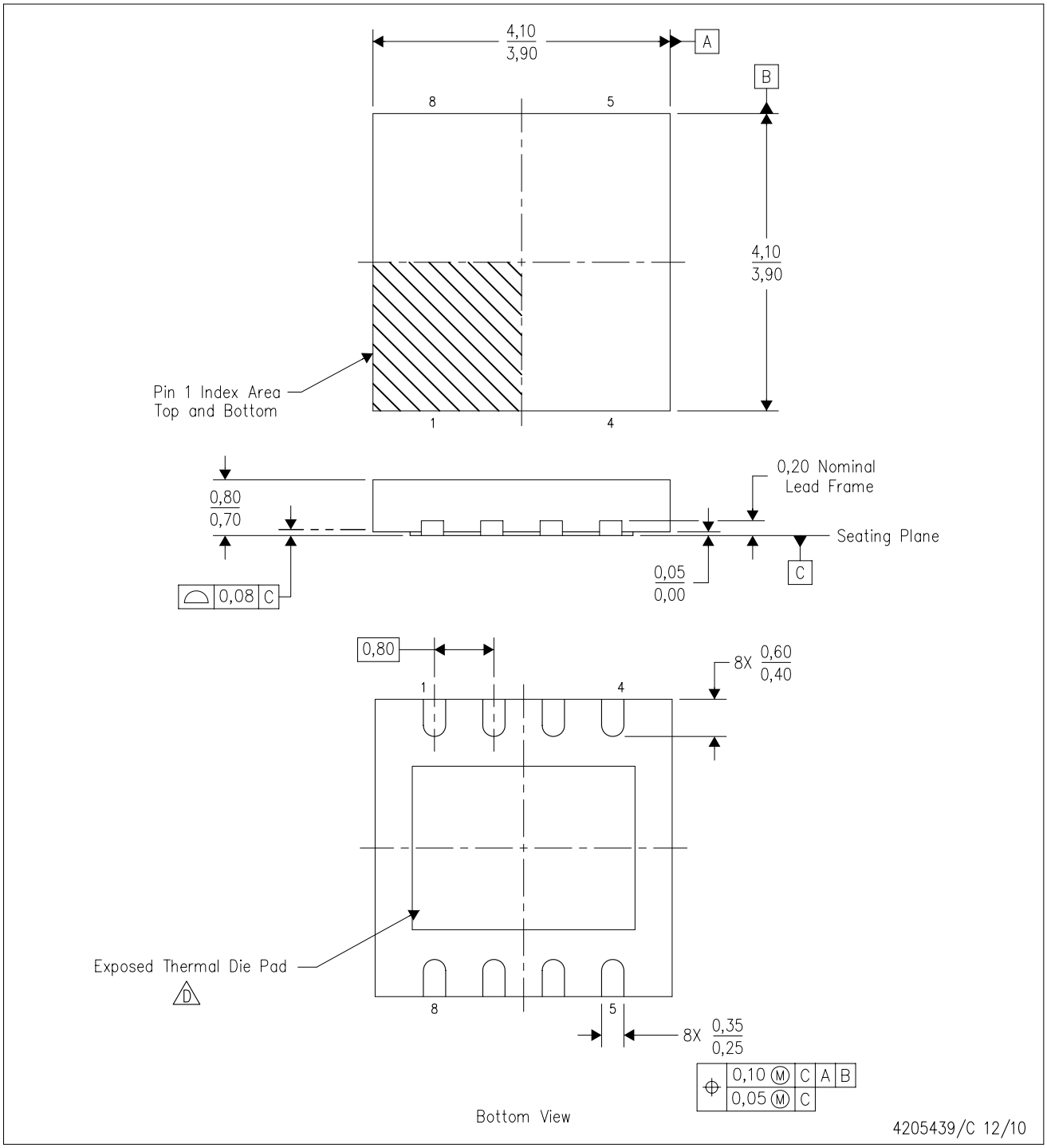
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN55HVD251DRJR	SON	DRJ	8	1000	210.0	185.0	35.0
SN65HVD251DR	SOIC	D	8	2500	340.5	338.1	20.6

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–229 variation WGGB.

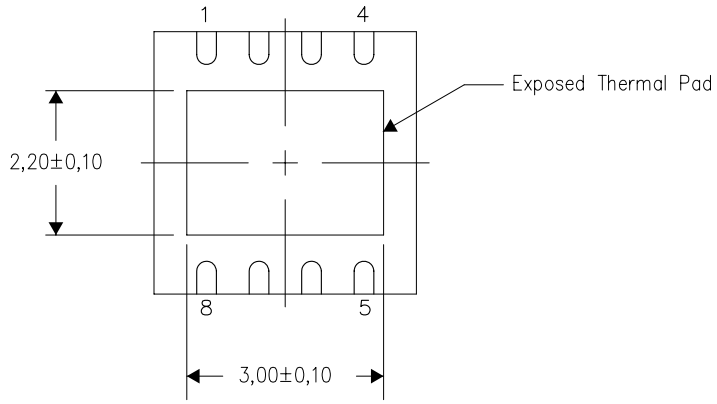
DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



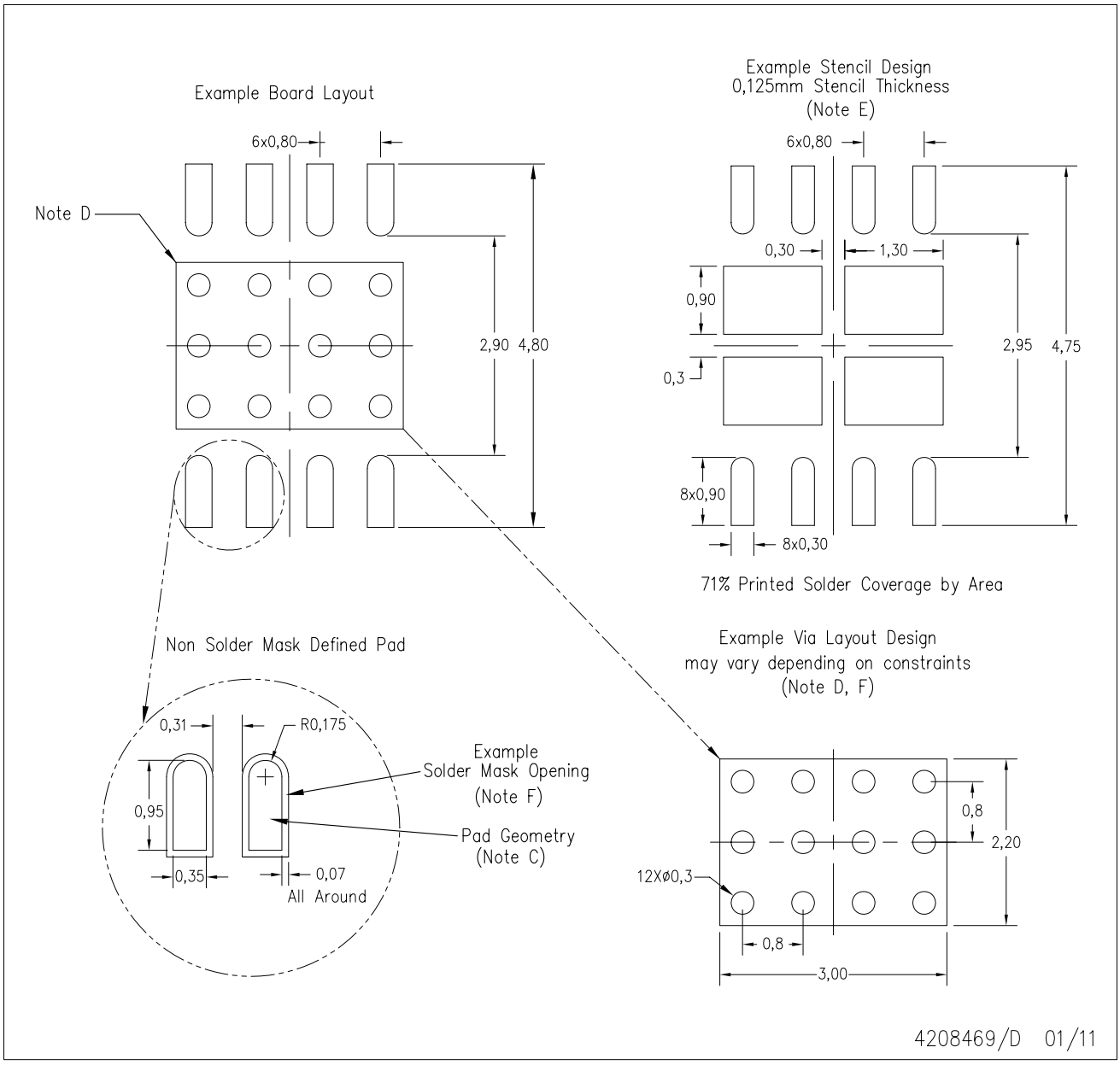
Bottom View

Exposed Thermal Pad Dimensions

4206882/F 01/11

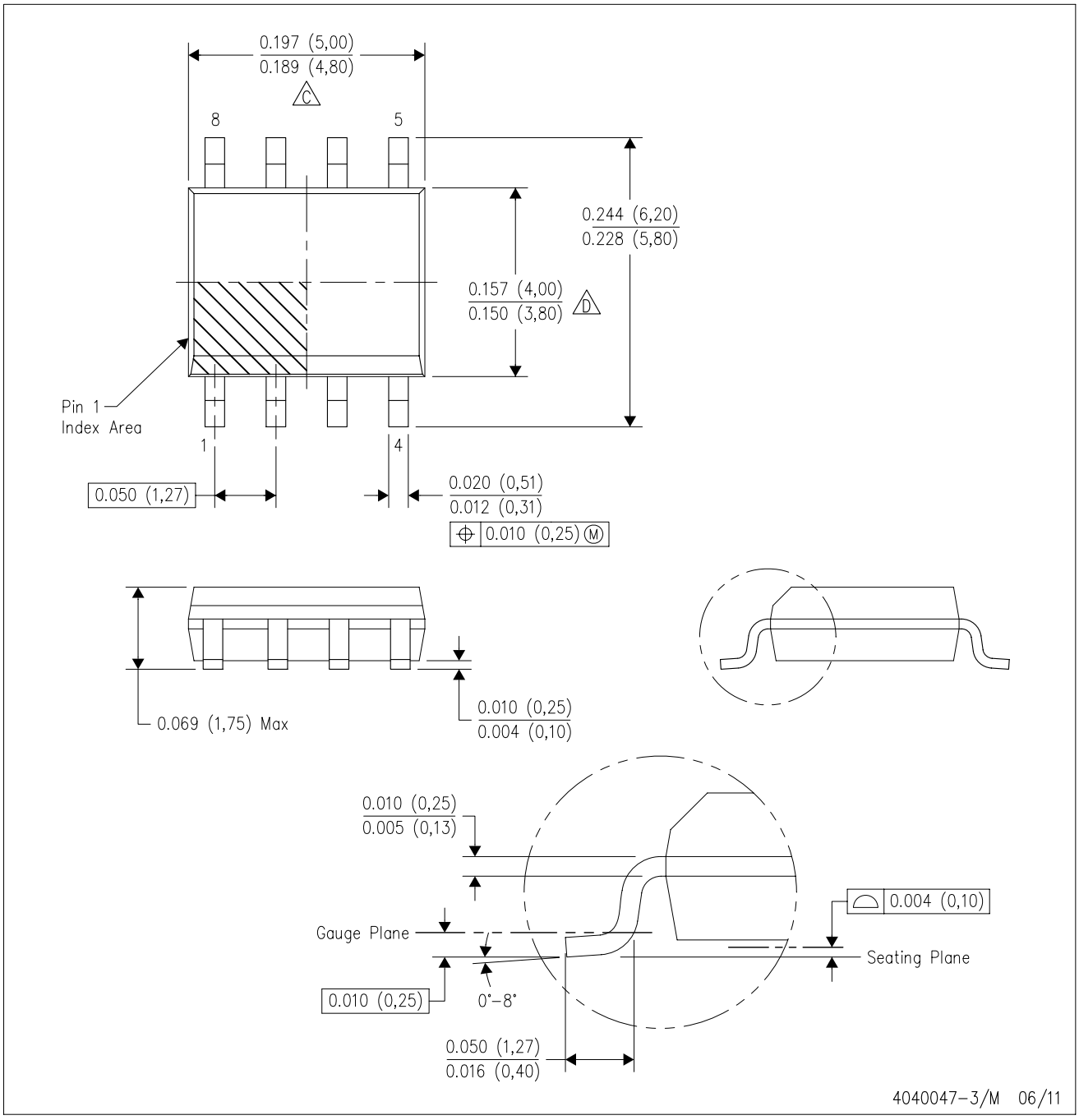
NOTE: All linear dimensions are in millimeters

DRJ (S–PWSON–N8) SMALL PACKAGE OUTLINE NO–LEAD



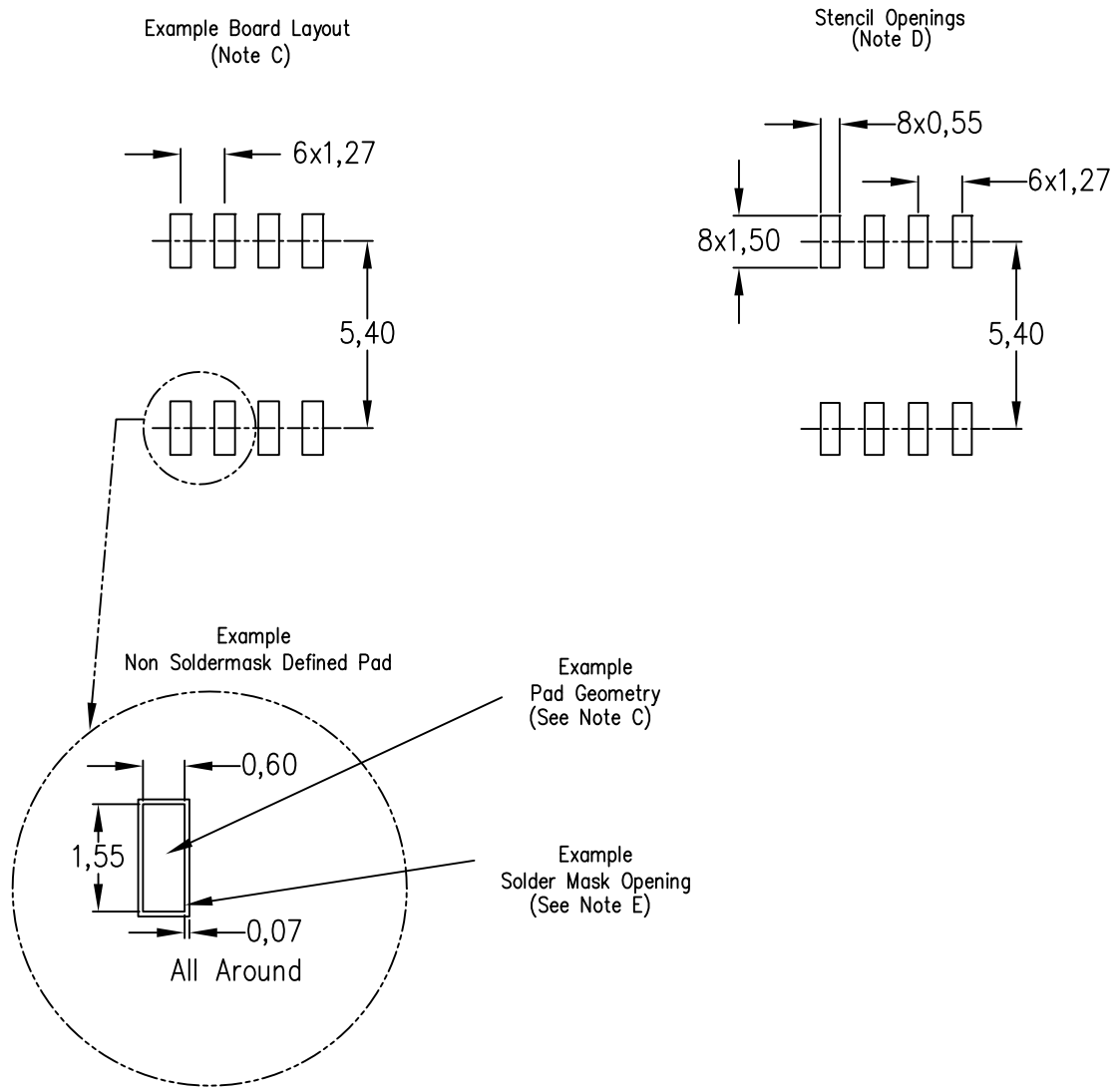
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances and vias tenting recommendations for vias placed in the thermal pad.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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