Fault-Protected RS-485 Transceivers with 3.3-V to 5-V Operation

Check for Samples: SN65HVD1780-Q1, SN65HVD1781-Q1, SN65HVD1782 -Q1

FEATURES

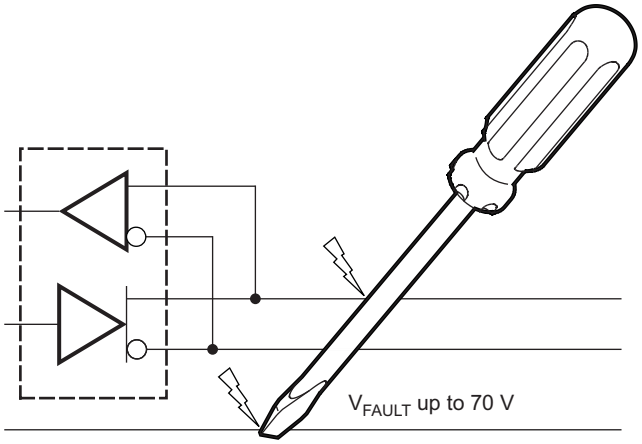
- **Qualified for Automotive Applications**
- **Bus-Pin Fault Protection to:**
  - **> ±70 V ('HVD1780, 81)**
  - **> ±30 V ('HVD1782)**
- **Operation With 3.3-V to 5-V Supply Range**
- **±16 kV HBM Protection on Bus Pins**
- **Reduced Unit Load for up to 320 Nodes**
- **Failsafe Receiver for Open-Circuit, Short-Circuit and Idle-Bus Conditions**
- **Low Power Consumption**
  - **Low Standby Supply Current, 1 μA Max**
  - **I_{CC} 4 mA Quiescent During Operation**
- **Pin-Compatible With Industry-Standard SN75176**
- **Signaling Rates of 115 kbps, 1 Mbps, and up to 10 Mbps**

DESCRIPTION

These devices are designed to survive overvoltage faults such as direct shorts to power supplies, mis-wiring faults, connector failures, cable crushes, and tool mis-applications. They are also robust to ESD events, with high levels of protection to the human-body-model specification.

These devices combine a differential driver and a differential receiver, which operate from a single power supply. In the 'HVD1782, the driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. This port features a wide common-mode voltage range, making the devices suitable for multipoint applications over long cable runs. These devices are characterized from –40°C to 125°C. These devices are pin-compatible with the industry-standard SN75176 transceiver, making them drop-in upgrades in most systems.

These devices are fully compliant with ANSI TIA/EIA 485-A with a 5-V supply and can operate with a 3.3-V supply with reduced driver output voltage for low-power applications. For applications where operation is required over an extended common-mode voltage range, see the SN65HVD1785 (SLLS872) data sheet.



M0092-02

Transceiver	Signaling Rate	Number of Nodes
HVD1780	Up to 115 kbps	Up to 320
HVD1781	Up to 1 Mbps	Up to 320
HVD1782	Up to 10 Mbps	Up to 64

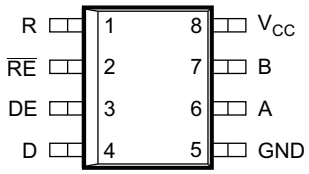
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

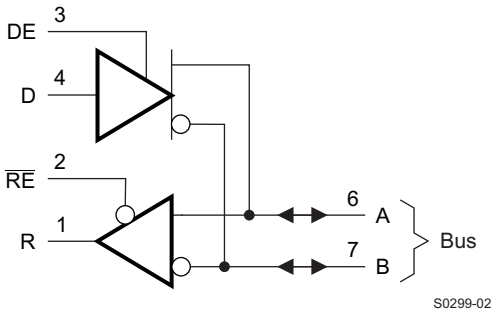
T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2500	SN65HVD1780QDRQ1 (3)	Product Preview
			SN65HVD1781QDRQ1	1781Q
			SN65HVD1782QDRQ1(3)	Product Preview

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Product Preview

D PACKAGE
(TOP VIEW)



LOGIC DIAGRAM (POSITIVE LOGIC)



DEVICE INFORMATION

DRIVER FUNCTION TABLE

Input	Enable	Outputs		Driver State
D	DE	A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled (1)
X	OPEN	Z	Z	Driver disabled by default (1)
OPEN	H	H	L	Actively drive bus High by default

(1) When both the driver and receiver are disabled, the device enters a low-power standby mode.

RECEIVER FUNCTION TABLE

Differential Input	Enable	Output	Receiver State
$V_{ID} = V_A - V_B$	RE	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled (1)
X	OPEN	Z	Receiver disabled by default (1)
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

(1) When both the driver and receiver are disabled, the device enters a low-power standby mode.

ABSOLUTE MAXIMUM RATINGS(1)

				VALUE	UNIT
V_{CC}	Supply voltage			–0.5 to 7	V
	Voltage range at bus pins	'HVD1780, 81	A, B pins	–70 to 70	V
		'HVD1782	A, B pins	–70 to 30	
	Input voltage range at any logic pin			–0.3 to V_{CC} + 0.3	V
	Transient overvoltage pulse through 100 Ω per TIA-485			–70 to 70	V
	Receiver output current			–24 to 24	mA
T_J	Junction temperature			170	°C
	Continuous total power dissipation			See Dissipation Rating Table	
ESD	Electrostatic discharge	Human-Body Model (HBM), IEC 60749-26.	Bus terminals and GND	±16	kV
		Human-Body Model (HBM). Test method based upon AEC-Q100-002	Bus terminals and GND	±16	kV
		Human-Body Model (HBM), AEC-Q100-002	All Pins	±4	kV
		Charged-Device Model (CDM), AEC-Q100-011	All Pins	±2	kV
		Machine Model (MM) , AEC-Q100-003	All Pins	±400	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS

PACKAGE(1)	JEDEC THERMAL MODEL	T_A < 25°C RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C RATING	T_A = 105°C RATING	T_A = 125°C RATING (3.3 V ONLY)
SOIC (D) 8-pin	High-K	905 mW	7.25 mW/°C	470 mW	325 mW	180 mW
	Low-K	516 mW	4.1 mW/°C	268 mW	186 mW	103 mW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15	5	5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)(1)		–7		12	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)		0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current, driver		–60		60	mA
	Output current, receiver		–8		8	mA
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
$1/t_{UI}$	Signaling rate	HVD1780			115	Mbps
		HVD1781			1	
		HVD1782			10	
T_A	Operating free-air temperature (See application section for thermal information)	5-V supply	–40		105	°C
		3.3-V supply	–40		125	
T_J	Junction Temperature		–40		150	

(1) By convention, the least positive (most negative) limit is designated as minimum in this data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, 4.75 V ≤ V_{CC} 375 Ω on each output to –7 V to 12 V Figure 1	T_A < 85°C		1.5			V
			T_A < 125°C		1.4			
		R_L = 54 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V	T_A < 85°C		1.7	2		
			T_A < 125°C		1.5			
		R_L = 54 Ω, 3.15 V ≤ V_{CC} ≤ 3.45 V			0.8	1		
		R_L = 100 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V	T_A < 85°C		2.2	2.5		
			T_A < 125°C		2			
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54 Ω			–50	0	50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage				1	V_{CC}/2	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage				–50	0	50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors, See Figure 2				500		mV
C_{OD}	Differential output capacitance					23		pF
V_{IT+}	Positive-going receiver differential input voltage threshold					–100	–35	mV
$V_{IT–}$	Negative-going receiver differential input voltage threshold				–180	–150		
V_{HYS}	Receiver differential input voltage threshold hysteresis (V_{IT+} – $V_{IT–}$)(1)				30	50		
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA			2.4	V_{CC} – 0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA	T_A < 85°C			0.2	0.4	V
			T_A < 125°C				0.5	
$I_{I(LOGIC)}$	Driver input, driver enable, and receiver enable input current				–50		50	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}			–1		1	µA
I_{OS}	Driver short-circuit output current				–200		200	mA
$I_{I(BUS)}$	Bus input current (disabled driver)	V_{CC} = 3.15 to 5.5 V or V_{CC} = 0 V, DE at 0 V	V_I = 12 V	1780, 1781		75	100	µA
				1782		400	500	
			V_I = –7 V	1780, 1781	–60	–40		
				1782	-400	-300		
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V_{CC}, RE = GND, no load			4	6	mA
		Driver enabled, receiver disabled	DE = V_{CC}, RE = V_{CC}, no load			3	5	
		Driver disabled, receiver enabled	DE = GND, RE = GND, no load			2	4	
		Driver and receiver disabled, standby mode	DE = GND, D = open, RE = V_{CC}, no load, T_A < 85°C			0.15	1	µA
			DE = GND, D = open, RE = V_{CC}, no load, T_A < 125°C				12	
	Supply current (dynamic)	See the *Typical Characteristics* section						

(1) Ensured by design. Not production tested.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER (HVD1780)							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 3	3.15 V < V_{CC} < 3.45 V	0.4	1.4	1.8	µs
			3.15 V < V_{CC} < 5.5 V	0.4	1.7	2.6	µs
t_{PHL}, t_{PLH}	Driver propagation delay				0.8	2	µs
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$				20	250	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 4 and Figure 5		0.1	5	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			0.2	3	µs
		Receiver disabled			3	12	
DRIVER (HVD1781)							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 3		50		300	ns
t_{PHL}, t_{PLH}	Driver propagation delay					200	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$					25	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 4 and Figure 5			3	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled				300	ns
		Receiver disabled				10	µs
DRIVER (HVD1782)							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	All V_{CC} and Temp			50	ns
			V_{CC} > 4.5V and T < 105°C		16		
t_{PHL}, t_{PLH}	Driver propagation delay		See Figure 3			55	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$					10	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 4 and Figure 5			3	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled				300	ns
		Receiver disabled				9	µs
RECEIVER (ALL DEVICES UNLESS OTHERWISE NOTED)							
t_r, t_f	Receiver output rise/fall time (1)	C_L = 15 pF, See Figure 6	All devices		4	15	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time		HVD1780, HVD1781		100	200	ns
			HVD1782			80	
$t_{SK(P)}$	Receiver output pulse skew, $\|t_{PHL} - t_{PLH}\|$		HVD1780, HVD1781		6	20	ns
			HVD1782			5	
t_{PLZ}, t_{PHZ}	Receiver disable time (1)	Driver enabled, See Figure 7			15	100	ns
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled, See Figure 7			80	300	ns
		Driver disabled, See Figure 8			3	9	µs

(1) Ensured by design. Not production tested.

THERMAL INFORMATION

PARAMETER		TEST CONDITIONS	VALUE	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance (no airflow)	SOIC-8	JEDEC high-K model	138	°C/W
		JEDIC low-K model	242	
$R_{\theta JB}$ Junction-to-board thermal resistance	SOIC-8		62	°C/W
$R_{\theta JC}$ Junction-to-case thermal resistance	SOIC-8		61	°C/W
P_D Power dissipation		V_{CC} = 3.6V, T_J = 150°C, R_L = 300 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 3.3-V supply, unterminated(1)	75	mW
		V_{CC} = 3.6V, T_J = 150°C, R_L = 100 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 3.3-V supply, RS-422 load(1)	95	
		V_{CC} = 3.6V, T_J = 150°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 3.3-V supply, RS-485 load(1)	115	
		V_{CC} = 5.5V, T_J = 150°C, R_L = 300 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, unterminated(1)	290	
		V_{CC} = 5.5V, T_J = 150°C, R_L = 100 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-422 load(1)	320	
		V_{CC} = 5.5V, T_J = 150°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-485 load(1)	400	
T_{SD} Thermal-shutdown junction temperature			170	°C

(1) Driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: 1 Mbps.

APPLICATION INFORMATION

Hot-Plugging

These devices are designed to operate in "hot swap" or "hot pluggable" applications. Key features for hot-pluggable applications are power-up, power-down glitch free operation, default disabled input/output pins, and receiver failsafe. As shown in Figure 9, an internal Power-On Reset circuit keeps the driver outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no problems will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in the device FUNCTION TABLE, the enable inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

Receiver Failsafe

The differential receiver is "failsafe" to invalid bus states caused by open bus conditions such as, a disconnected connector, shorted bus conditions caused by damaged cabling, or idle bus conditions that occur when no driver is actively driving a valid RD-485 bus state on the network. In any of these cases, the differential receiver will output a failsafe HIGH state, so that small noise signals do not cause problems at the receiver output.

PARAMETER MEASUREMENT INFORMATION

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.

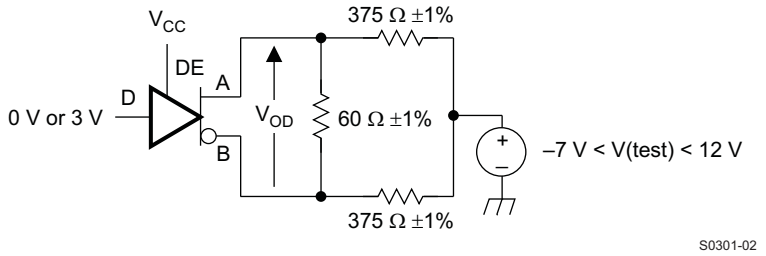


Figure 1. Measurement of Driver Differential Output Voltage With Common-Mode Load

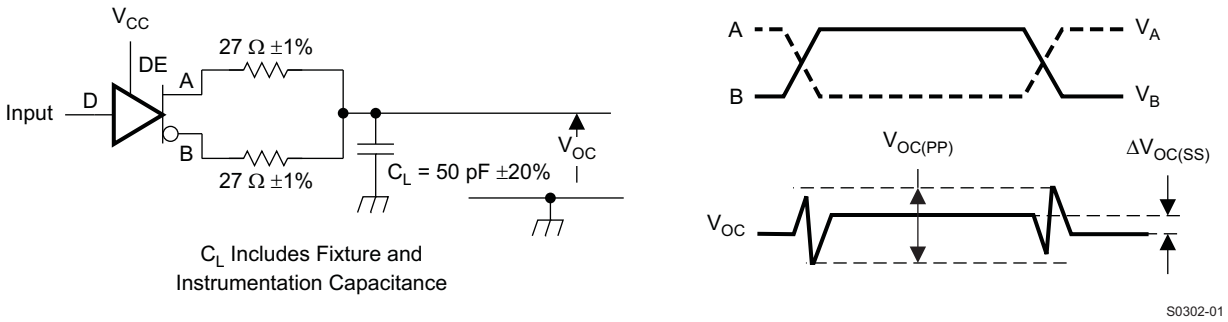


Figure 2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

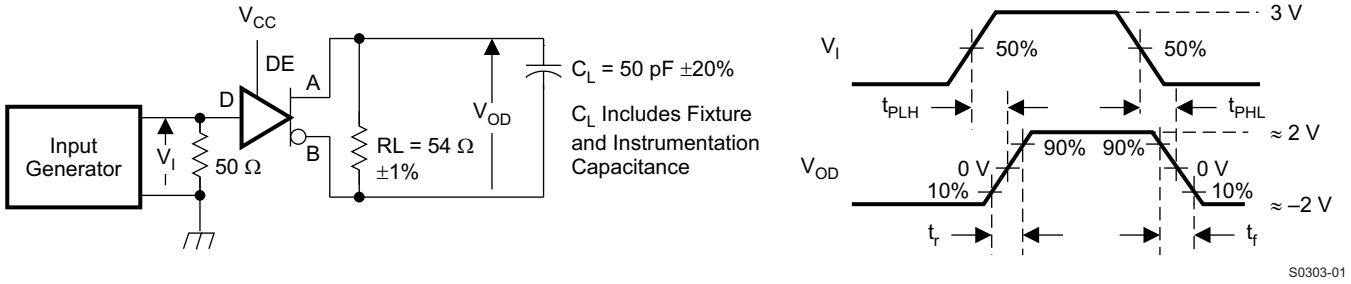
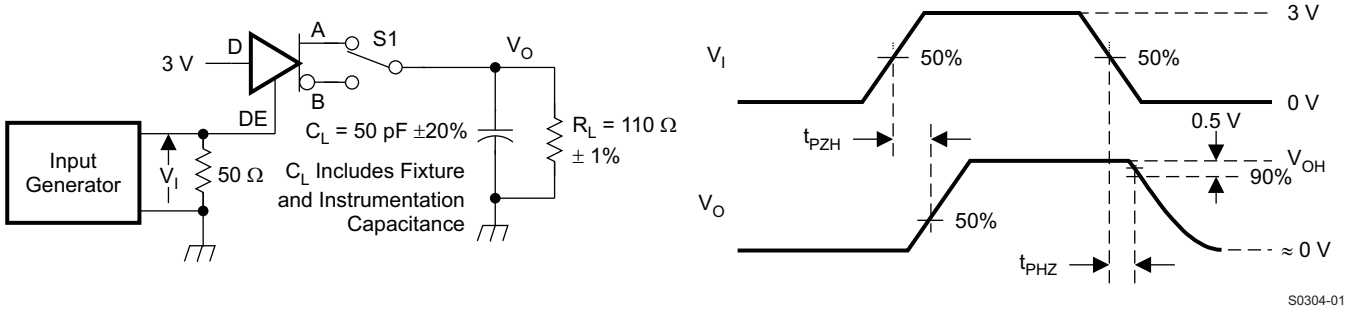


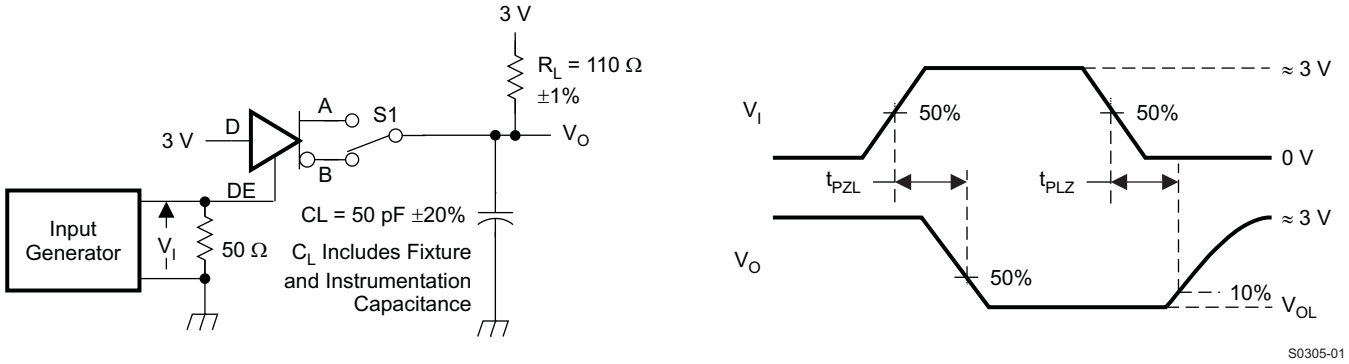
Figure 3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



NOTE: D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 4. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: D at 0 V to test non-inverting output, D at 3 V to test inverting output.

Figure 5. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load

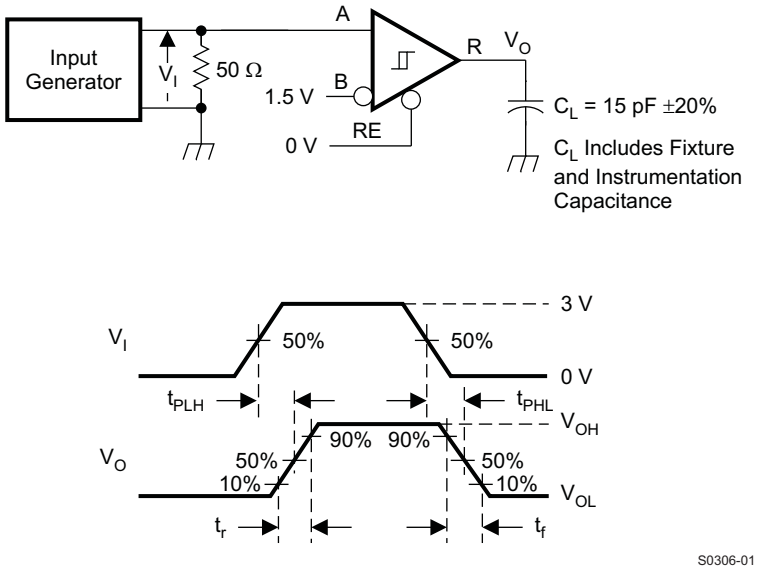


Figure 6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

PARAMETER MEASUREMENT INFORMATION (continued)

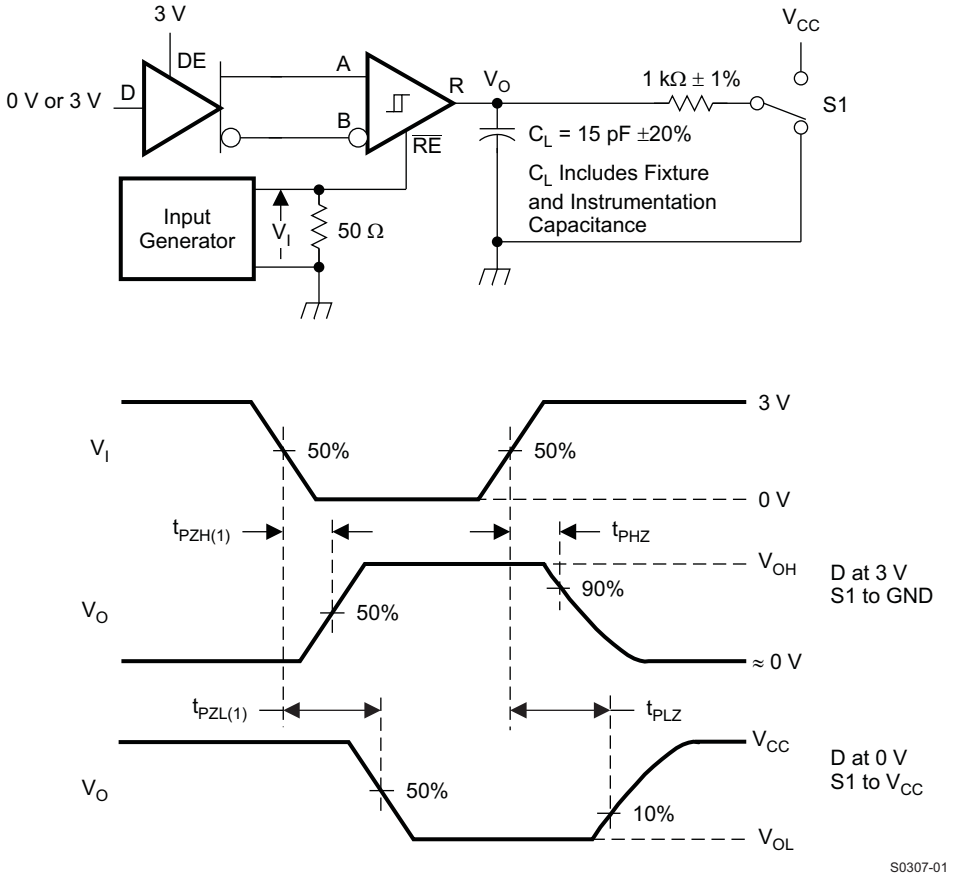


Figure 7. Measurement of Receiver Enable/Disable Times With Driver Enabled

PARAMETER MEASUREMENT INFORMATION (continued)

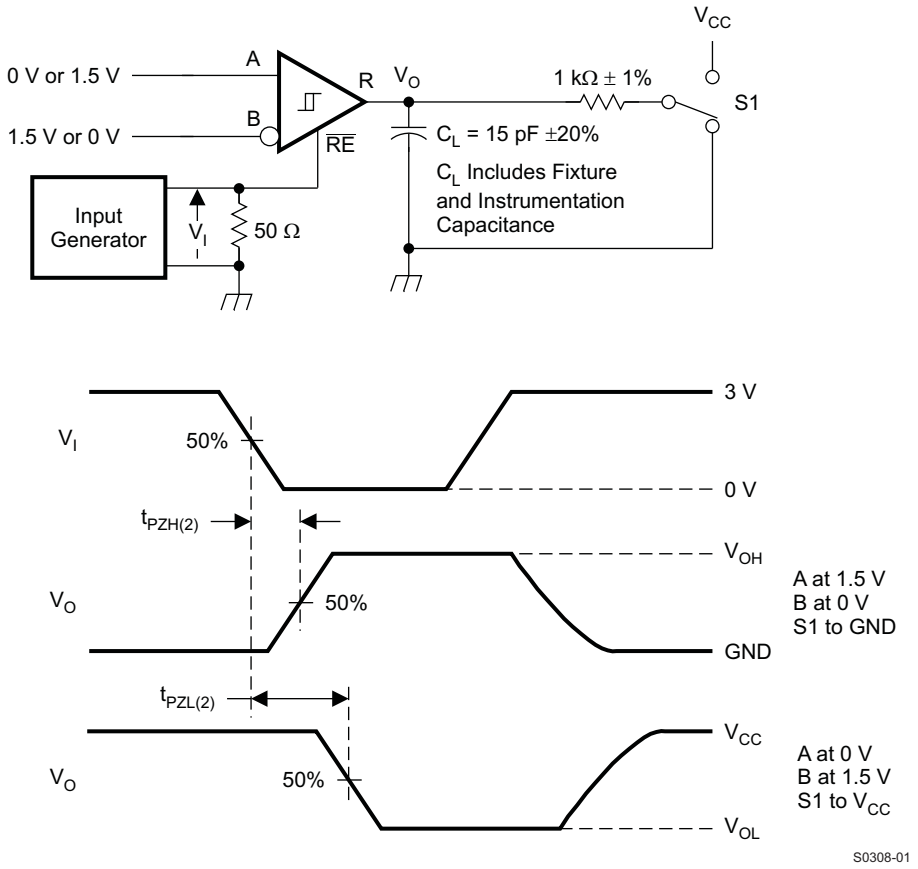


Figure 8. 'HVD1781 Measurement of Receiver Enable Times With Driver Disabled

TYPICAL CHARACTERISTICS

DRIVER OUTPUT CURRENT vs SUPPLY VOLTAGE

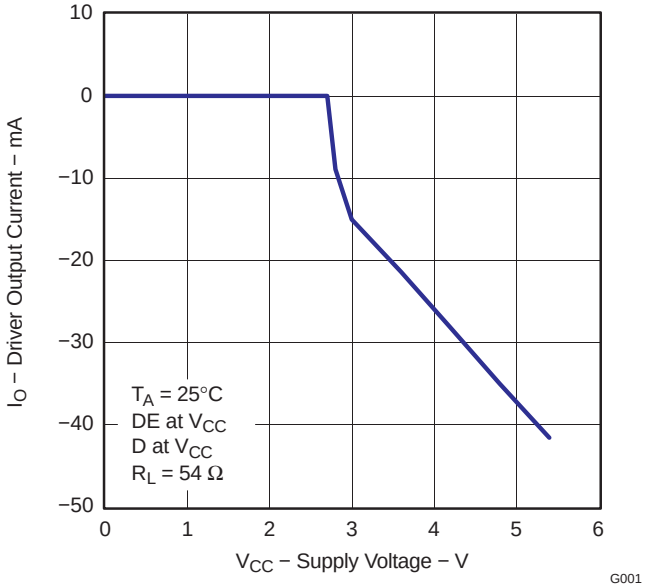


Figure 9.

RMS SUPPLY CURRENT vs SIGNALING RATE

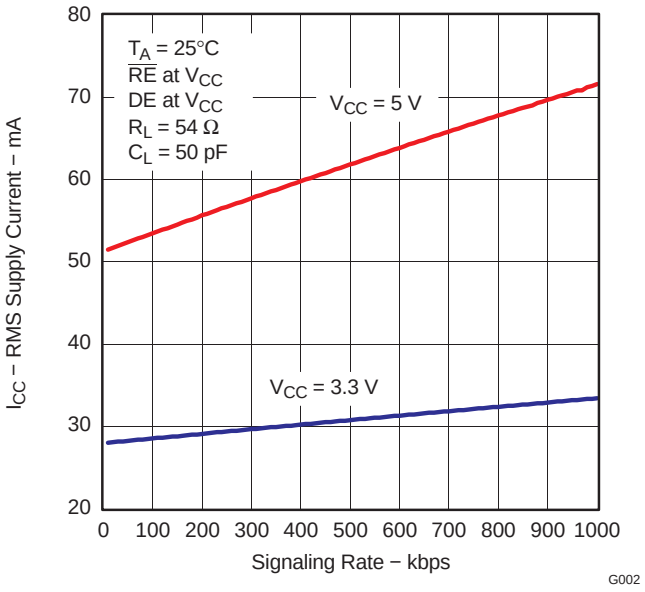


Figure 10.

DIFFERENTIAL OUTPUT VOLTAGE vs DIFFERENTIAL LOAD CURRENT

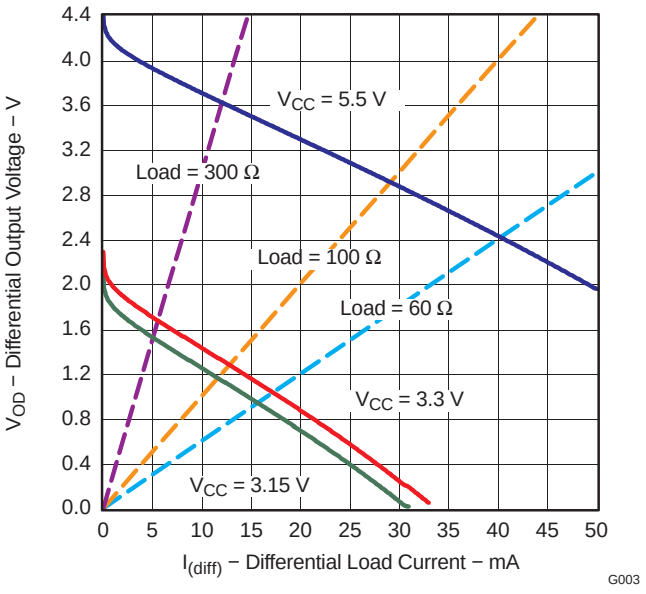


Figure 11.

HVD1782 RISE/FALL TIME

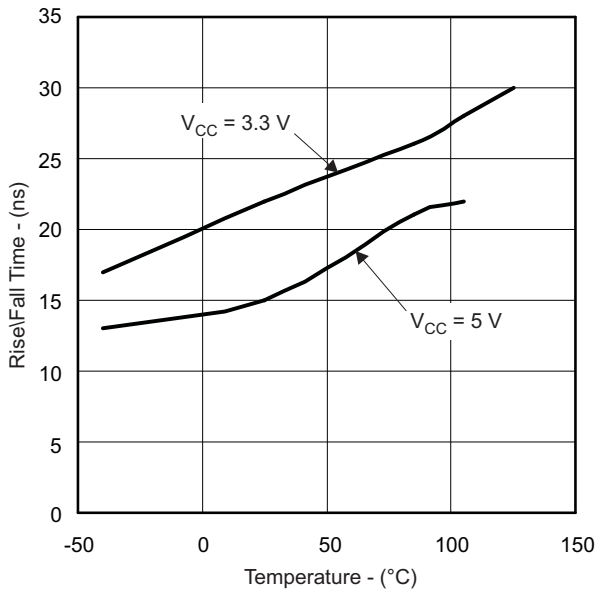


Figure 12.

TYPICAL CHARACTERISTICS (continued)

HVD1780 DIFFERENTIAL OUTPUT AMPLITUDE and TRANSITION TIME vs SUPPLY VOLTAGE

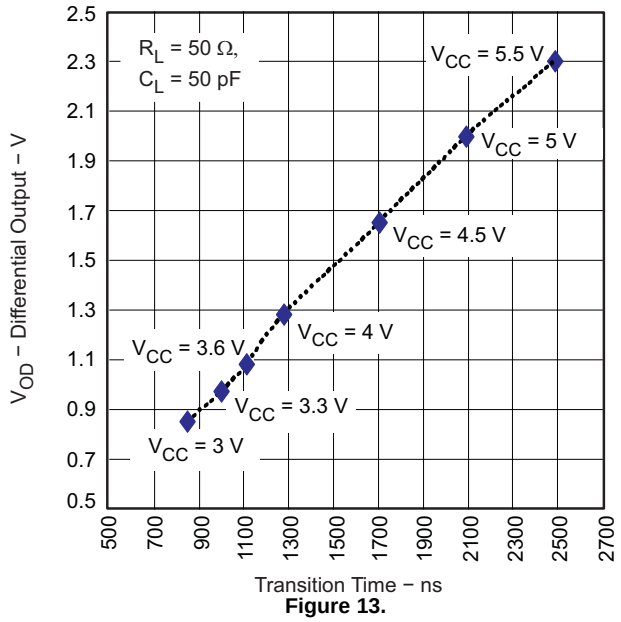


Figure 13.

70-V Fault-Protection

The SN65HVD17xx family of RS-485 devices is designed to survive bus pin faults up to ±70V. The devices designed for fast signaling rate (10 Mbps) will not survive a bus pin fault with a direct short to voltages above 30V when:

1. the device is powered on AND

2a. the driver is enabled (DE=HIGH) AND D=HIGH AND the bus fault is applied to the A pin OR

2b. the driver is enabled (DE=HIGH) AND D=LOW AND the bus fault is applied to the B pin

Under other conditions, the device will survive shorts to bus pin faults up to 70V. Table 1 summarizes the conditions under which the device may be damaged, and the conditions under which the device will not be damaged.

Table 1. Device Conditions

POWER	DE	D	A	B	RESULTS
OFF	X	X	-70V < V_A < 70V	-70V < V_B < 70V	Device survives
ON	LO	X	-70V < V_A < 70V	-70V < V_B < 70V	Device survives
ON	HI	L	-70V < V_A < 70V	-70V < V_B < 30V	Device survives
ON	HI	L	-70V < V_A < 70V	30V < V_B	Damage may occur
ON	HI	H	-70V < V_A < 30V	-70V < V_B < 30V	Device survives
ON	HI	H	30V < V_A	-70V < V_B < 30V	Damage may occur

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65HVD1781QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1781Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

OTHER QUALIFIED VERSIONS OF SN65HVD1781-Q1 :

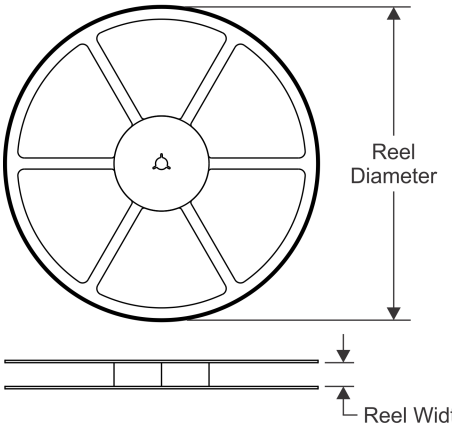
- Catalog: SN65HVD1781

NOTE: Qualified Version Definitions:

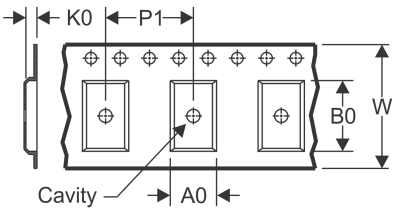
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

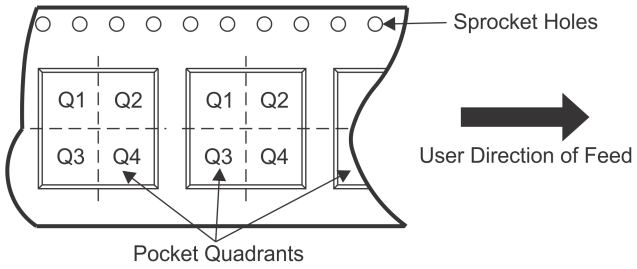


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

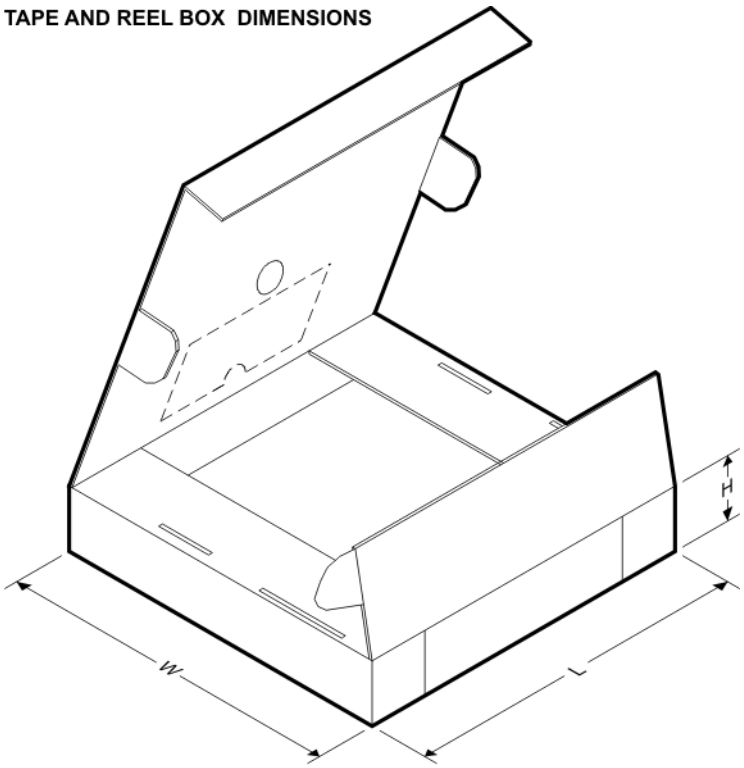
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1781QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

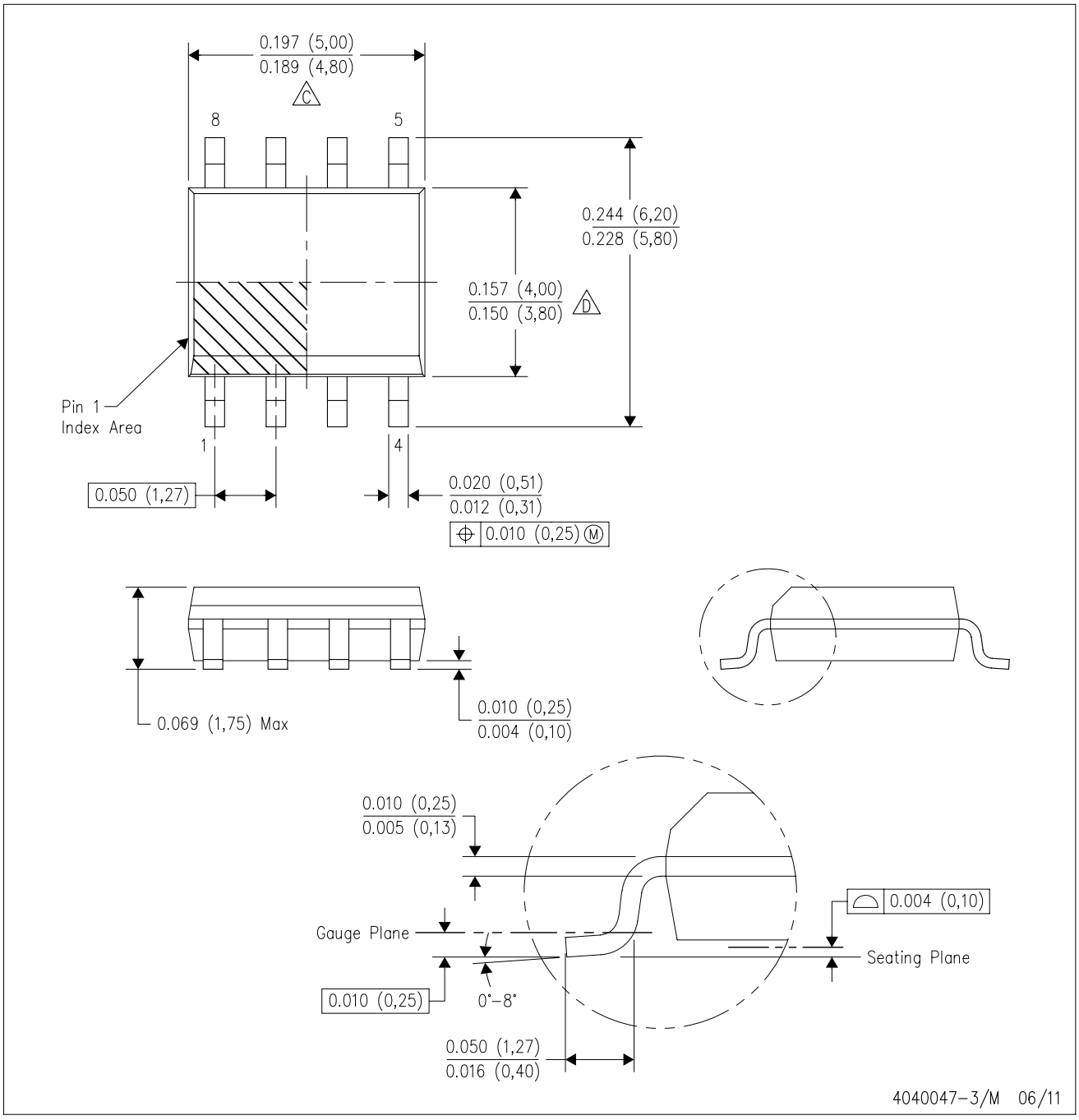
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

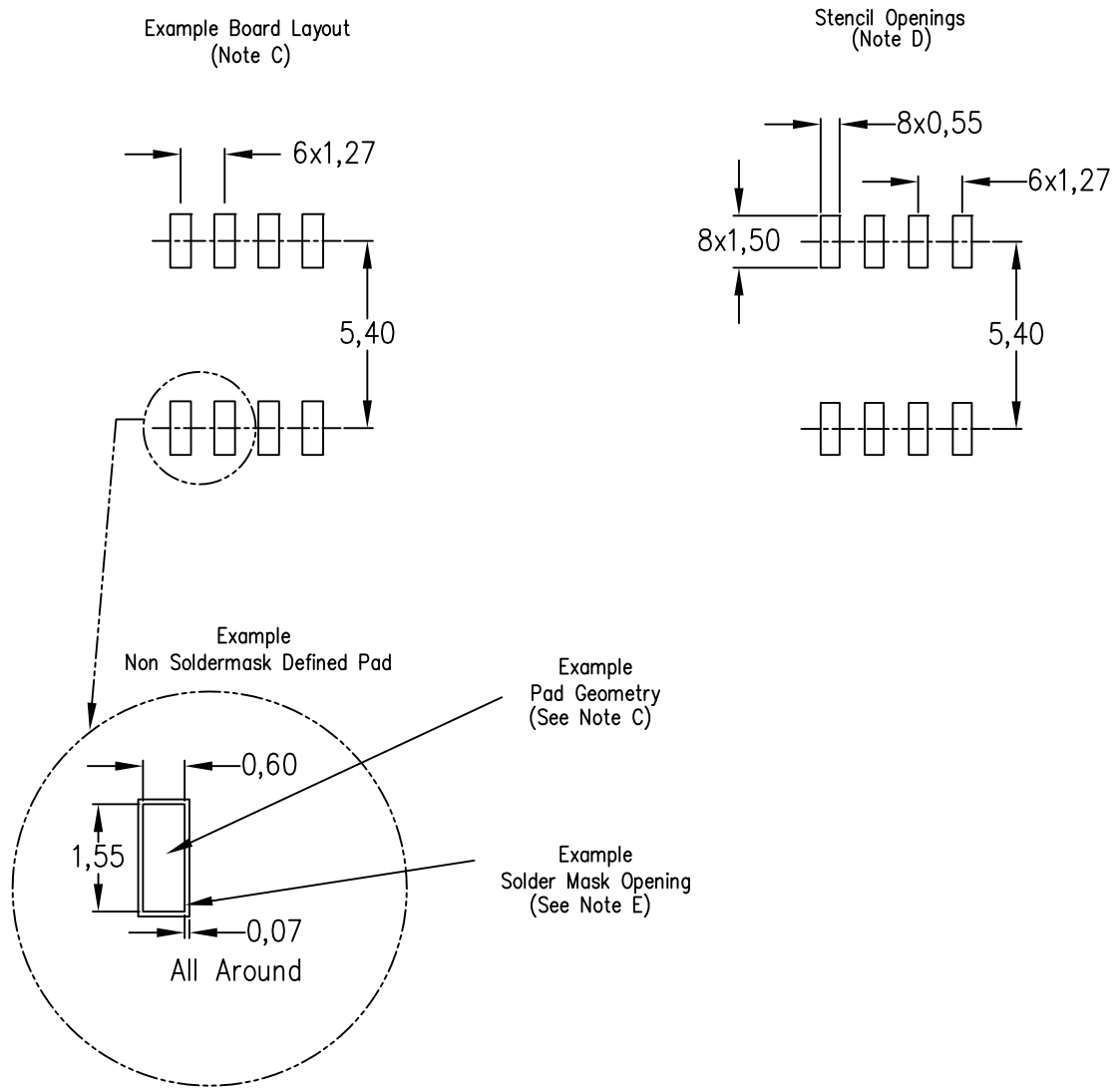
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1781QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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