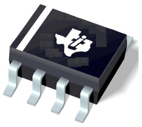


3.3-V CAN TRANSCEIVER

FEATURES

- **Bus-Pin Fault Protection Exceeds ±36 V**
- **Bus-Pin ESD Protection Exceeds 16-kV HBM**
- **Compatible With ISO 11898**
- **Signaling Rates(1) up to 1 Mbps**
- **Extended –7-V to 12-V Common-Mode Range**
- **High-Input Impedance Allows for 120 Nodes**
- **LVTTL I/Os Are 5-V Tolerant**
- **Adjustable Driver Transition Times for Improved Signal Quality**
- **Unpowered Node Does Not Disturb the Bus**
- **Low-Current Standby Mode . . . 200-μA Typical**
- **Thermal Shutdown Protection**
- **Power-Up/Down Glitch-Free Bus Inputs and Outputs**
  - **High Input Impedance With Low V_{CC}**
  - **Monolithic Output During Power Cycling**
- **Loopback for Diagnostic Functions Available**
- **DeviceNet Vendor ID #806**

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range(1)**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Additional temperature ranges available - contact factory

APPLICATIONS

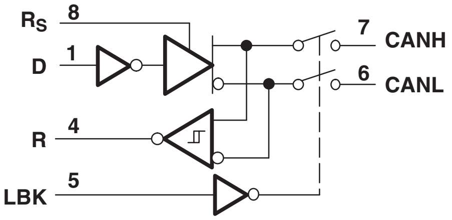
- **CAN Data Bus**
- **Industrial Automation**
  - **DeviceNet™ Data Buses**
  - **Smart Distributed Systems (SDS™)**
- **SAE J1939 Standard Data Bus Interface**
- **NMEA 2000 Standard Data Bus Interface**
- **ISO 11783 Standard Data Bus Interface**

DESCRIPTION

The SN65HVD233 is used in applications employing the controller area network (CAN) serial communication physical layer in accordance with the ISO 11898 standard. As a CAN transceiver, it provides transmit and receive capability between the differential CAN bus and a CAN controller, with signaling rates up to 1 Mbps.

Designed for operation in especially harsh environments, the device features cross-wire, overvoltage and loss of ground protection to ±36 V, with overtemperature protection and common-mode transient protection of ±100 V. This device operates over a –7-V to 12-V common-mode range with a maximum of 60 nodes on a bus.

FUNCTIONAL BLOCK DIAGRAM



This device has limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

If the common-mode range is restricted to the ISO-11898 Standard range of –2 V to 7 V, up to 120 nodes may be connected on a bus. This transceiver interfaces the single-ended CAN controller with the differential CAN bus found in industrial, building automation, and automotive applications.

The R_S (pin 8) of the SN65HVD233 provides for three modes of operation: high-speed, slope control, or low-power standby mode. The high-speed mode of operation is selected by connecting R_S directly to ground, allowing the driver output transistors to switch on and off as fast as possible with no limitation on the rise and fall slope. The rise and fall slope can be adjusted by connecting a resistor to ground at R_S, since the slope is proportional to the pin's output current. Slope control is implemented with a resistor value of 10 kΩ to achieve a slew rate of ≈ 15 V/µs and a value of 100 kΩ to achieve ≈ 2.0 V/µs slew rate. For more information about slope control, refer to the application information section.

The SN65HVD233 enters a low-current standby mode during which the driver is switched off and the receiver remains active if a high logic level is applied to R_S. The local protocol controller reverses this low-current standby mode when it needs to transmit to the bus.

A logic high on the loopback LBK (pin 5) of the SN65HVD233 places the bus output and bus input in a high-impedance state. The remaining circuit remains active and available for driver to receiver loopback, self-diagnostic node functions without disturbing the bus.

AVAILABLE OPTIONS

PART NUMBER	LOW POWER MODE	SLOPE CONTROL	DIAGNOSTIC LOOPBACK	AUTOBAUD LOOPBACK
SN65HVD233	200-µA standby mode	Adjustable	Yes	No

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – D	Reel of 2500	SN65HVD233MDREP	H233EP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD	$T_A \le 25°C$ POWER RATING	DERATING FACTOR[1] ABOVE T_A = 25°C	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	Low-K	596.6 mW	5.7 mW/°C	255.7 mW	28.4 mW
D	High-K	1076.9 mW	10.3 mW/°C	461.5 mW	51.3 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

				VALUE	UNIT
V_{CC}	Supply voltage range			–0.3 to 7	V
	Voltage range at any bus terminal (CANH or CANL)			–36 to 36	V
	Voltage input range, transient pulse, CANH and CANL, through 100 Ω (see Figure 7)			–100 to 100	V
V_I	Input voltage range, (D, R, R_S, LBK)			–0.5 to 7	V
I_O	Receiver output current			–10 to 10	mA
	Electrostatic discharge	Human Body Model(3)	CANH, CANL and GND	16	kV
	Electrostatic discharge	Human Body Model(3)	All pins	3	kV
		Charged-Device Mode(4)	All pins	1	kV
	Continuous total power dissipation			See Dissipation Rating Table	
T_J	Operating junction temperature			150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		3		3.6	V
	Voltage at any bus terminal (separately or common mode)		–7		12	
V_{IH}	High-level input voltage	D, LBK	2		5.5	
V_{IL}	Low-level input voltage	D, LBK	0		0.8	
V_{ID}	Differential input voltage		–6		6	
	Resistance from R_S to ground		0		100	kΩ
$V_{I(Rs)}$	Input Voltage at R_S for standby		0.75 V_{CC}		5.5	V
I_{OH}	High-level output current	Driver	–50			mA
		Receiver	–10			
I_{OL}	Low-level output current	Driver			50	mA
		Receiver			10	
T_J	Operating junction temperature				150	°C
T_A	Operating free-air temperature(1)		-55		125	°C

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

DRIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	D = 0 V, R_S = 0 V, See Figure 1 and Figure 2	2.45		V_{CC}	V
		CANL		0.5		1.25	
V_O	Bus output voltage (Recessive)	CANH	D = 3 V, R_S = 0 V, See Figure 1 and Figure 2		2.3		V
		CANL			2.3		
$V_{OD(D)}$	Differential output voltage (Dominant)		D = 0 V, R_S = 0 V, See Figure 1 and Figure 2	1.5	2	3	V
			D = 0 V, R_S = 0 V, See Figure 2 and Figure 3	1.2	2	3	
V_{OD}	Differential output voltage (Recessive)		D = 3 V, R_S = 0 V, See Figure 1 and Figure 2	–120		12	mV
			D = 3 V, R_S = 0 V, No load	–0.5		0.05	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage		See Figure 9		1		V
I_{IH}	High-level input current	D,LBK	D = 2 V	–30		30	μA
I_{IL}	Low-level input current	D, LBK	D = 0.8 V	–30		30	μA
I_{OS}	Short-circuit output current		V_{CANH} = –7 V, CANL Open, See Figure 12	–250			mA
			V_{CANH} = 12 V, CANL Open, See Figure 12			1	
			V_{CANL} = –7 V, CANH Open, See Figure 12	–1			
			V_{CANL} = 12 V, CANH Open, See Figure 12			250	
C_O	Output capacitance		See receiver input capacitance				
$I_{IRs(s)}$	R_S input current for standby		R_S = 0.75 V_{CC}	–10			μA
I_{CC}	Supply current	Standby	R_S = V_{CC}, D = V_{CC}, LBK = 0 V		200	600	μA
		Dominant	D = 0 V, No load, LBK = 0 V, R_S = 0 V			6	mA
		Recessive	D = V_{CC}, No load, LBK = 0 V, R_S = 0 V			6	

(1) All typical values are at 25°C and with a 3.3 V supply.

DRIVER SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_S = 0 V, See Figure 4		35	95	ns
		R_S with 10 kΩ to ground, See Figure 4		70	125	
		R_S with 100 kΩ to ground, See Figure 4		500	870	
t_{PHL}	Propagation delay time, high-to-low-level output	R_S = 0 V, See Figure 4		70	120	ns
		R_S with 10 kΩ to ground, See Figure 4		130	180	
		R_S with 100 kΩ to ground, SeeFigure 4		870	1200	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)	R_S = 0 V, See Figure 4		35		ns
		R_S with 10 kΩ to ground, See Figure 4		60		
		R_S with 100 kΩ to ground, SeeFigure 4		370		
t_r	Differential output signal rise time	R_S = 0 V, See Figure 4	20		70	ns
t_f	Differential output signal fall time		20		70	
t_r	Differential output signal rise time	R_S with 10 kΩ to ground, See Figure 4	30		135	ns
t_f	Differential output signal fall time		30		135	
t_r	Differential output signal rise time	R_S with 100 kΩ to ground, See Figure 4	300		1400	ns
t_f	Differential output signal fall time		300		1400	
$t_{en(s)}$	Enable time from standby to dominant	See Figure 8		0.6	1.5	µs

(1) All typical values are at 25°C and with a 3.3 V supply. Timing parameters are characterized but not production tested.

RECEIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage[2]		LBK = 0 V, See Table 1			750	900	mV
V_{IT-}	Negative-going input threshold voltage[2]				500	650		
V_{hys}	Hysteresis voltage (V_{IT+} – V_{IT-})					100		
V_{OH}	High-level output voltage		I_O = –4 mA, See Figure 6		2.4			V
V_{OL}	Low-level output voltage		I_O = 4 mA, See Figure 6				0.4	
I_I	Bus input current		CANH or CANL = 12 V	Other bus pin = 0 V, D = 3 V, LBK = 0 V, R_S = 0 V	150		500	µA
			CANH or CANL = 12 V, V_{CC} = 0 V		200		600	
			CANH or CANL = –7 V		–610		–150	
			CANH or CANL = –7 V, V_{CC} = 0 V		–450		–130	
C_I	Input capacitance (CANH or CANL)		Pin-to-ground, V_I = 0.4 sin (4E6πt) + 0.5V, D = 3 V, LBK = 0 V			40		pF
C_{ID}	Differential input capacitance		Pin-to-pin, V_I = 0.4 sin (4E6πt) + 0.5V, D = 3 V, LBK = 0 V			20		
R_{ID}	Differential input resistance		D = 3 V, LBK = 0 V		40		100	kΩ
R_{IN}	Input resistance (CANH or CANL)				20		50	
I_{CC}	Supply current	Sleep	D = V_{CC}, R_S = 0 V or V_{CC}			0.05	2	µA
		Standby	R_S = V_{CC}, D = V_{CC}, LBK = 0 V			200	600	
		Dominant	D = 0 V, No load, R_S = 0 V, LBK = 0 V				6	mA
		Recessive	D = V_{CC}, No load, R_S = 0 V, LBK = 0 V				6	

(1) All typical values are at 25°C and with a 3.3 V supply.
(2) Characterized but not production tested.

RECEIVER SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 6		35	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	60	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} – t_{PLH} \rvert$)			7		
t_r	Output signal rise time			2	6.5	
t_f	Output signal fall time			2	6.5	

(1) All typical values are at 25°C and with a 3.3 V supply. Timing parameters are characterized but not production tested.

DEVICE SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
$t_{(LBK)}$	Loopback delay, driver input to receiver output	HVD233	See Figure 11		7.5	13	ns
$t_{(loop1)}$	Total loop delay, driver input to receiver output, recessive to dominant		R_S = 0 V, See Figure 10		70	135	ns
			R_S with 10 kΩ to ground, See Figure 10		105	190	
			R_S with 100 kΩ to ground, See Figure 10		535	1000	
$t_{(loop2)}$	Total loop delay, driver input to receiver output, dominant to recessive		R_S = 0 V, See Figure 10		70	135	ns
			R_S with 10 kΩ to ground, See Figure 10		105	190	
			R_S with 100 kΩ to ground, See Figure 10		535	1100	

(1) All typical values are at 25°C and with a 3.3 V supply. Timing parameters are characterized but not production tested.

PARAMETER MEASUREMENT INFORMATION

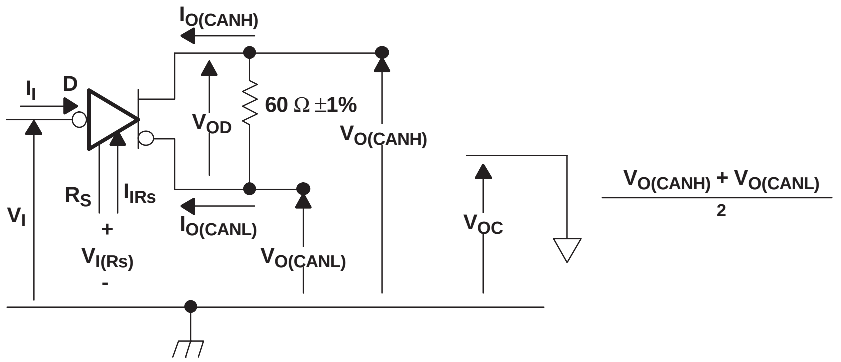


Figure 1. Driver Voltage, Current, and Test Definition

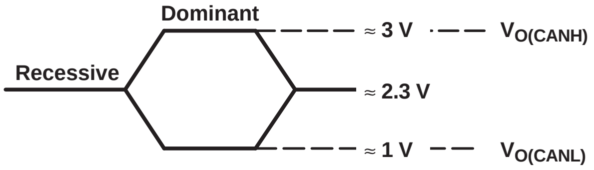


Figure 2. Bus Logic State Voltage Definitions

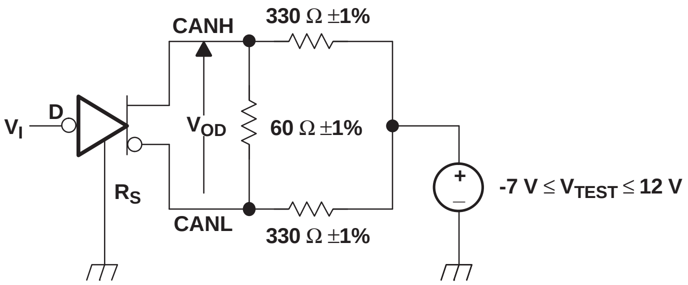
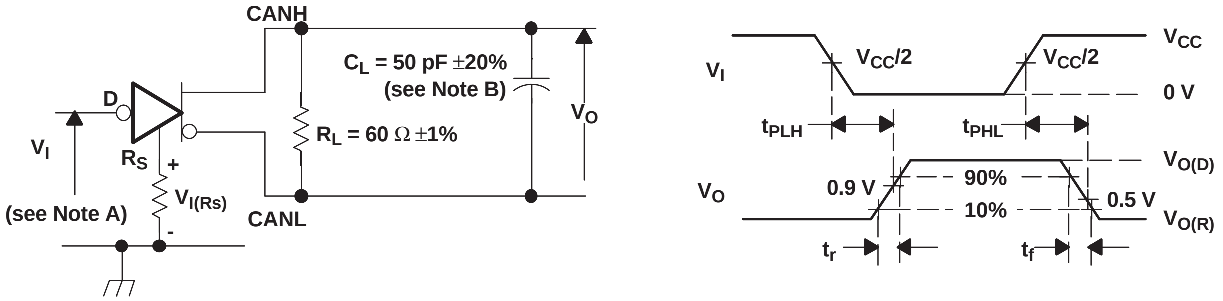


Figure 3. Driver V_{OD}



A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes fixture and instrumentation capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

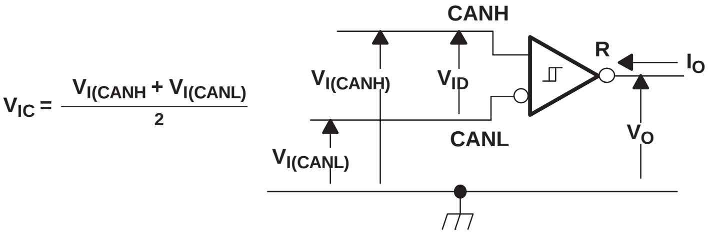
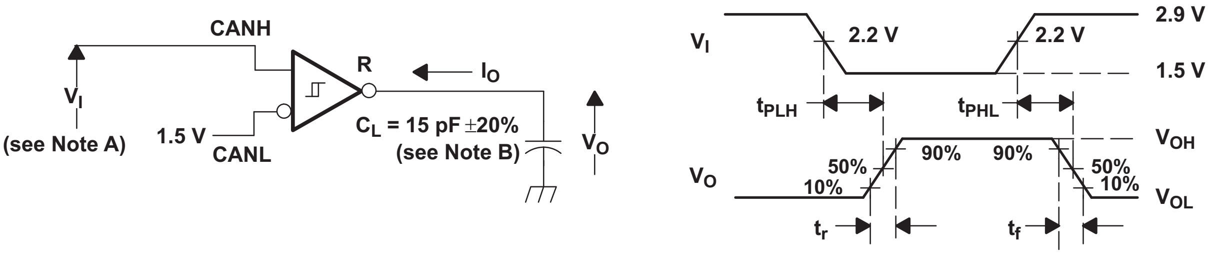


Figure 5. Receiver Voltage and Current Definitions



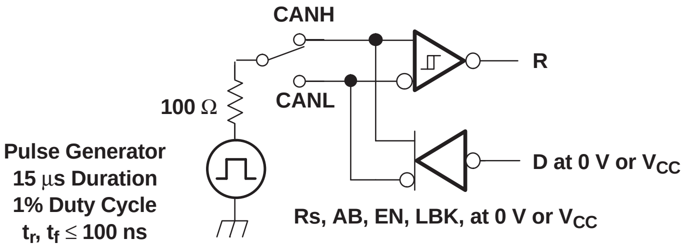
A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50\ \Omega$.

B. C_L includes fixture and instrumentation capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

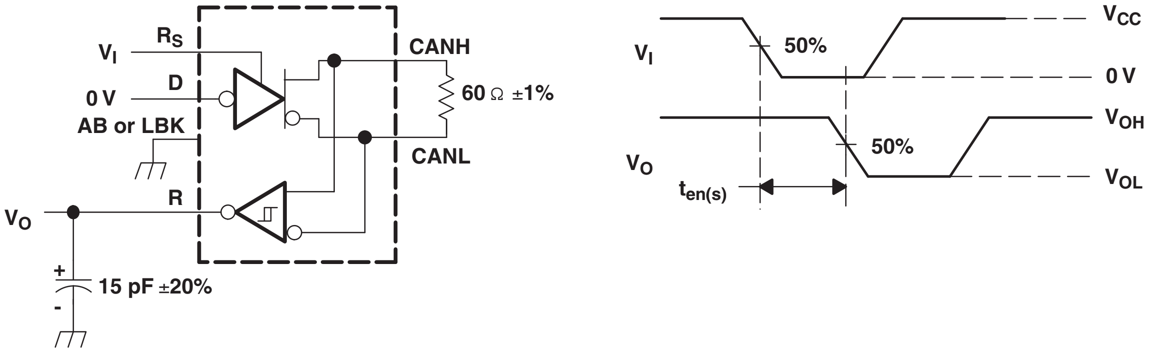
Table 1. Differential Input Voltage Threshold Test

INPUT		OUTPUT		MEASURED
V_{CANH}	V_{CANL}	R		$\lvert V_{ID} \rvert$
–6.1 V	–7 V	L	V_{OL}	900 mV
12 V	11.1 V	L		900 mV
–1 V	–7 V	L		6 V
12 V	6 V	L		6 V
–6.5 V	–7 V	H	V_{OH}	500 mV
12 V	11.5 V	H		500 mV
–7 V	–1 V	H		6 V
6 V	12 V	H		6 V
Open	Open	H		X



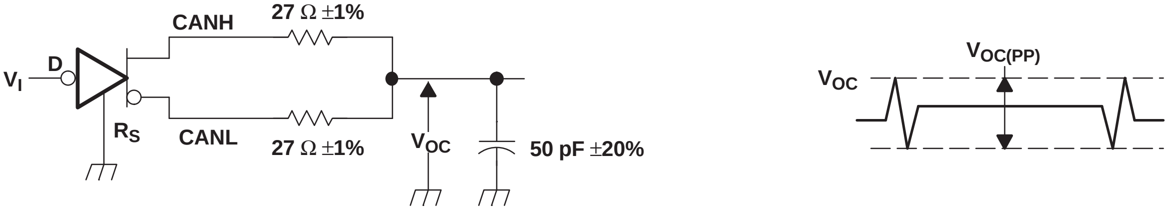
NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 7. Test Circuit, Transient Over Voltage Test



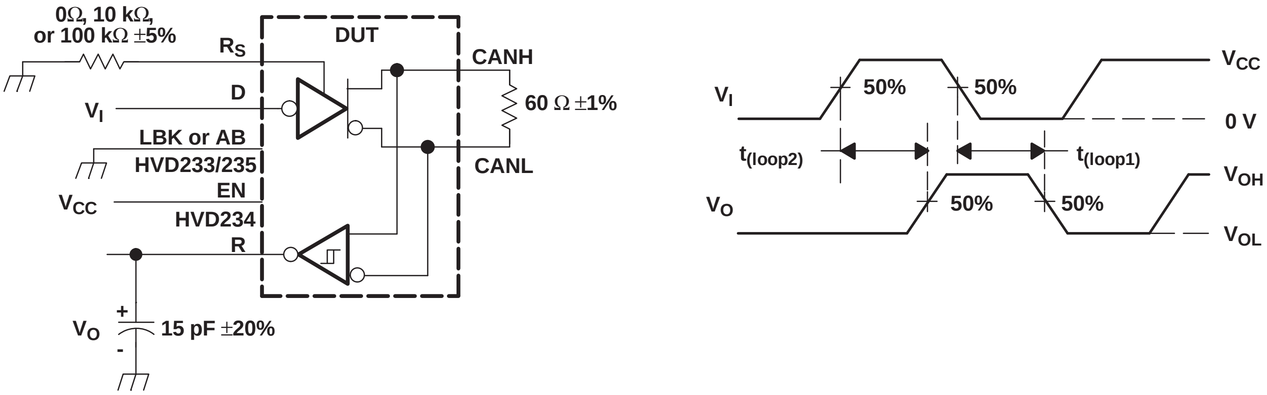
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8. $t_{en(s)}$ Test Circuit and Voltage Waveforms



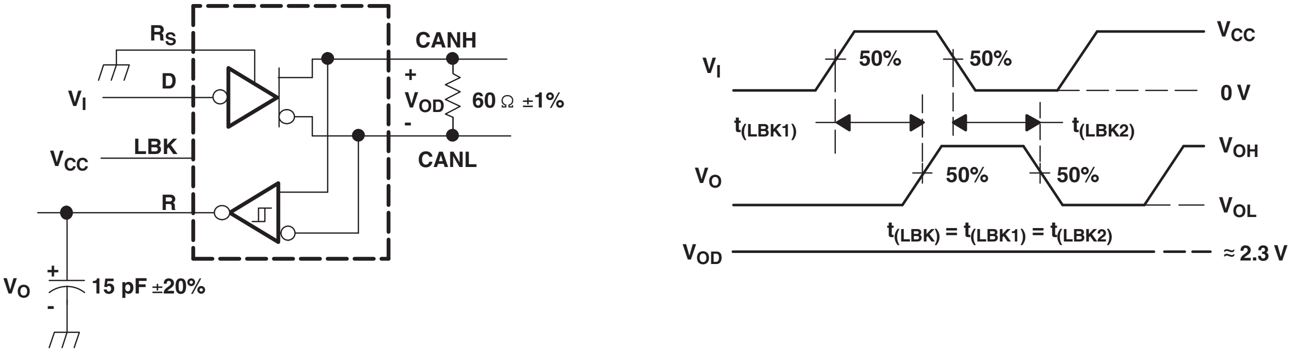
NOTE: All V_I input pulses are supplied by a generator having the following characteristics:
t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 9. $V_{OC(pp)}$ Test Circuit and Voltage Waveforms



NOTE: All V_I input pulses are supplied by a generator having the following characteristics:
t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 10. $t_{(loop)}$ Test Circuit and Voltage Waveforms



NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 11. $t_{(LBK)}$ Test Circuit and Voltage Waveforms

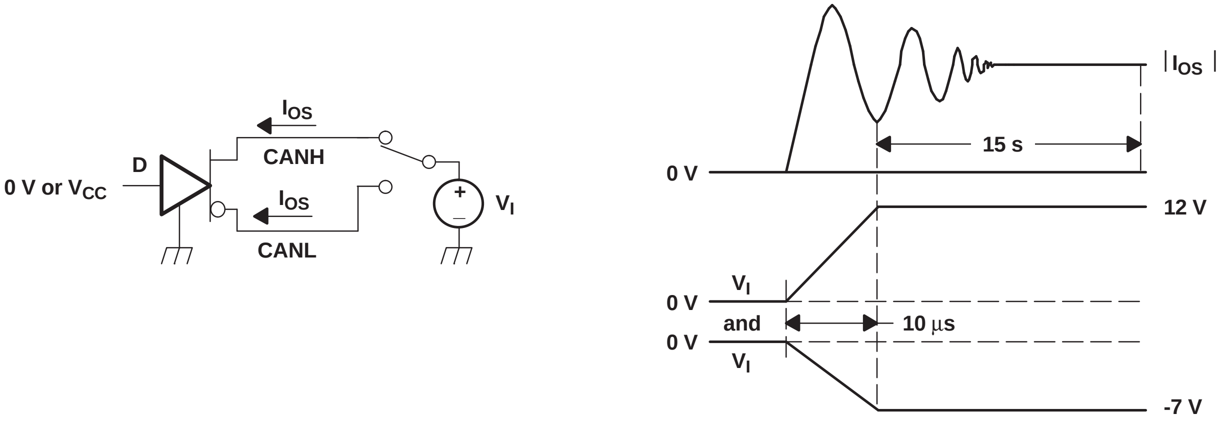
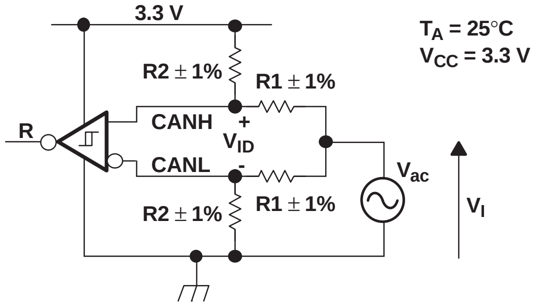
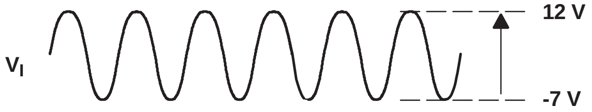


Figure 12. I_{OS} Test Circuit and Waveforms



The R Output State Does Not Change During Application of the Input Waveform.

V_{ID}	R1	R2
500 mV	50 Ω	280 Ω
900 mV	50 Ω	130 Ω

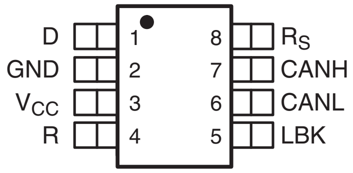


NOTE: All input pulses are supplied by a generator with f ≤ 1.5 MHz.

Figure 13. Common-Mode Voltage Rejection

DEVICE INFORMATION

SN65HVD233D
(TOP VIEW)



EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

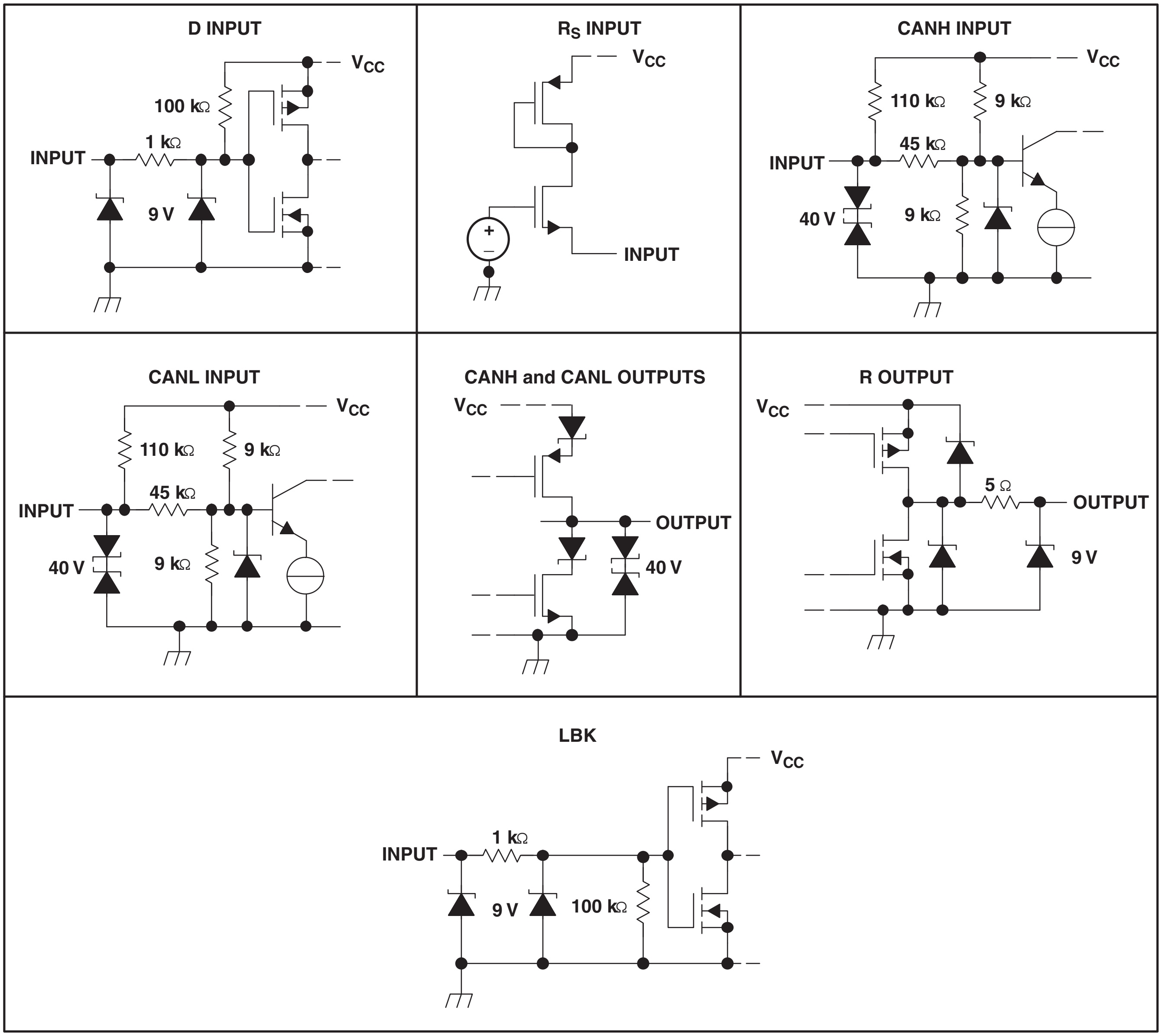


Table 2. Thermal Characteristics

PARAMETERS		TEST CONDITIONS	VALUE	UNIT
θ_{JA}	Junction-to-ambient thermal resistance[1]	Low-K[2] board, no air flow	185	°C/W
		High-K[3] board, no air flow	101	
θ_{JB}	Junction-to-board thermal resistance	High-K[3] board, no air flow	82.8	°C/W
θ_{JC}	Junction-to-case thermal resistance		26.5	°C/W
$P_{(AVG)}$	Average power dissipation	R_L = 60 Ω, R_S at 0 V, input to D a 1-MHz 50% duty cycle square wave V_{CC} at 3.3 V, T_A = 25°C	36.4	mW
$T_{(SD)}$	Thermal shutdown junction temperature		170	°C

(1) See TI literature number SZZA003 for an explanation of this parameter.
(2) JESD51-3 low effective thermal conductivity test board for leaded surface mount packages.
(3) JESD51-7 high effective thermal conductivity test board for leaded surface mount packages.

FUNCTION TABLES

DRIVER(1)

INPUTS			OUTPUTS		
D	**LBK/AB**	**R_S**	**CANH**	**CANL**	**BUS STATE**
X	X	> 0.75 V_{CC}	Z	Z	Recessive
L	L or open	≤ 0.33 V_{CC}	H	L	Dominant
H or open	X		Z	Z	Recessive
X	H	≤ 0.33 V_{CC}	Z	Z	Recessive

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

RECEIVER(1)

INPUTS				OUTPUT
BUS STATE	**$V_{ID} = V_{(CANH)}–V_{(CANL)}$**	**LBK**	**D**	**R**
Dominant	V_{ID} ≥ 0.9 V	L or open	X	L
Recessive	V_{ID} ≤ 0.5 V or open	L or open	H or open	H
?	0.5 V < V_{ID} <0.9 V	L or open	H or open	?
X	X	H	L	L
X	X		H	H

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

TYPICAL CHARACTERISTICS

RECESSIVE-TO-DOMINANT LOOP TIME vs FREE-AIR TEMPERATURE

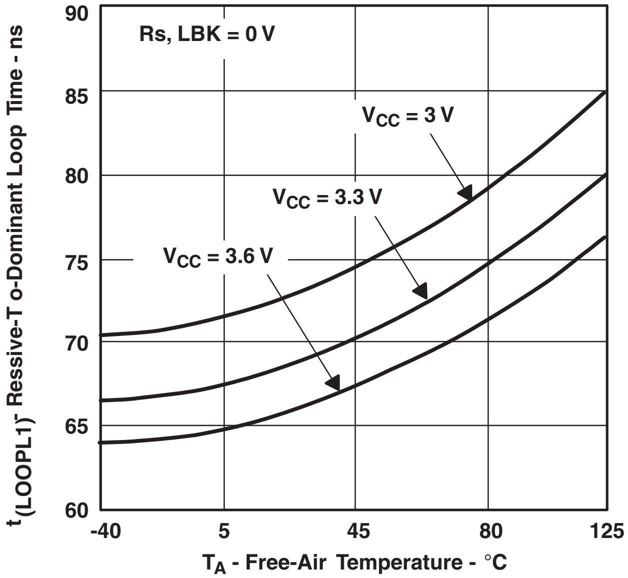


Figure 14.

DOMINANT-TO-RECESSIVE LOOP TIME vs FREE-AIR TEMPERATURE

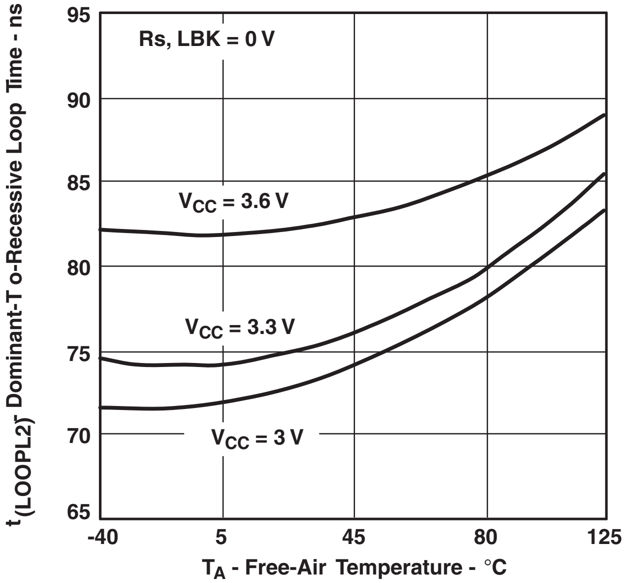


Figure 15.

SUPPLY CURRENT vs FREQUENCY

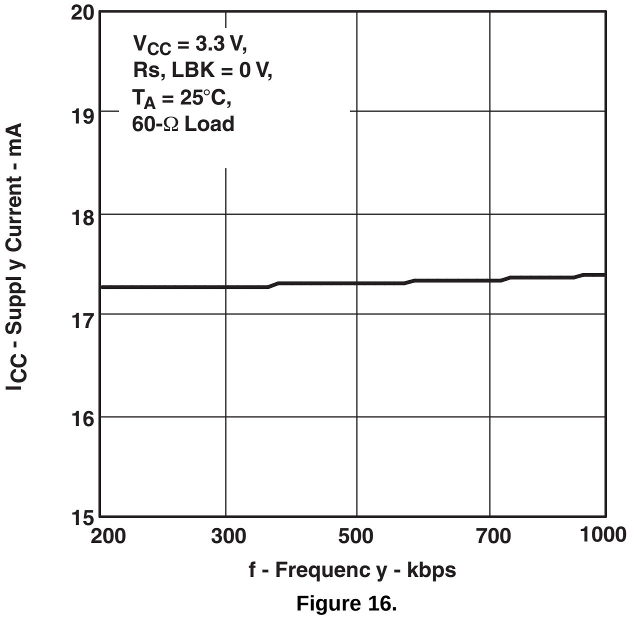


Figure 16.

DRIVER LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

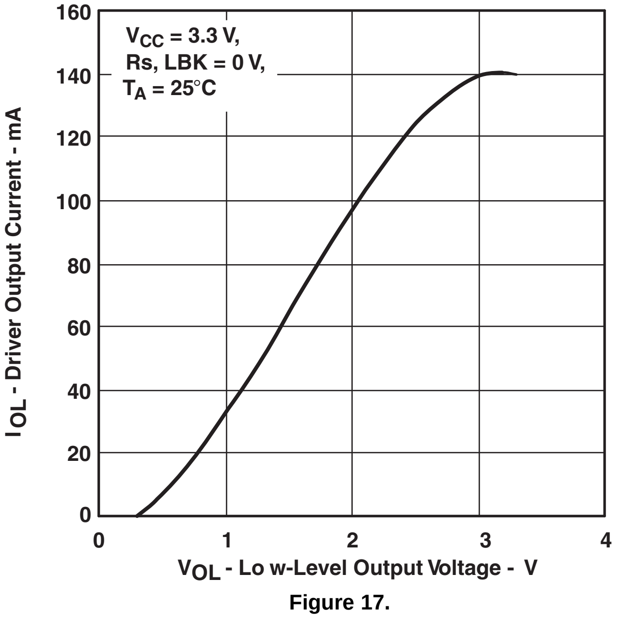


Figure 17.

TYPICAL CHARACTERISTICS (continued)

DRIVER HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

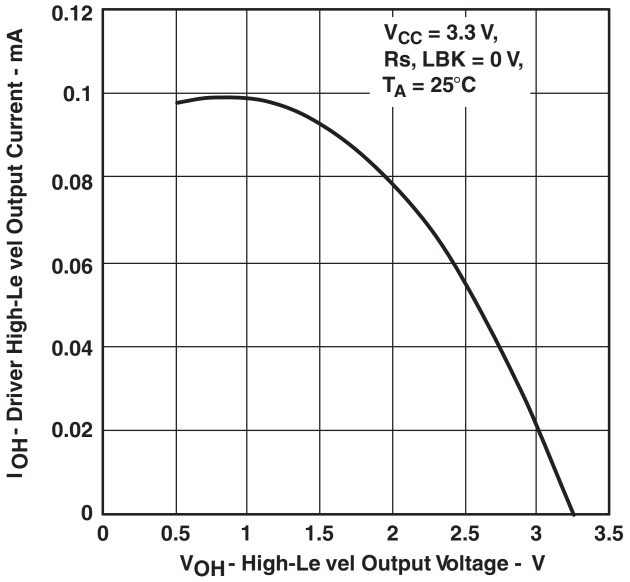


Figure 18.

DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

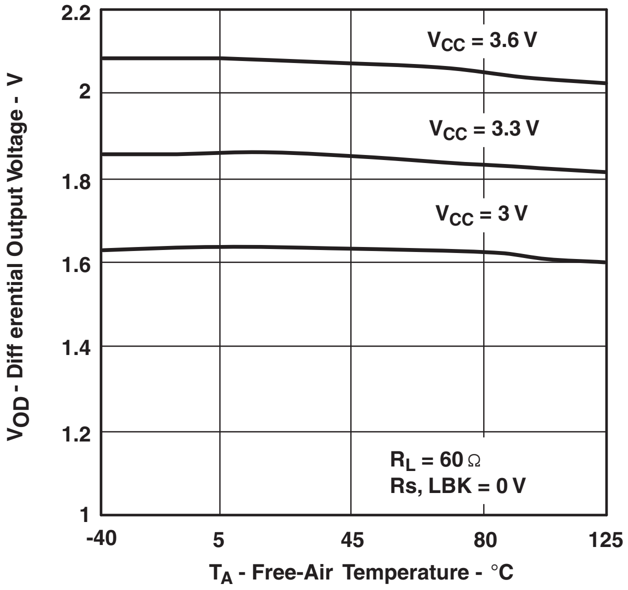


Figure 19.

RECEIVER LOW-TO-HIGH PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

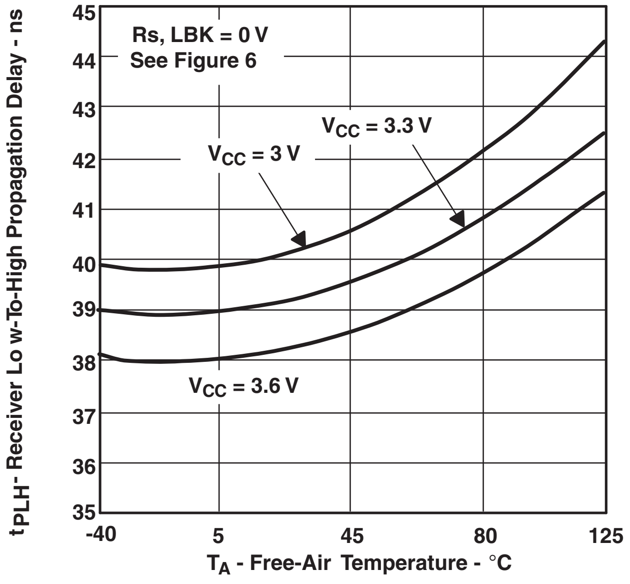


Figure 20.

RECEIVER HIGH-TO-LOW PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

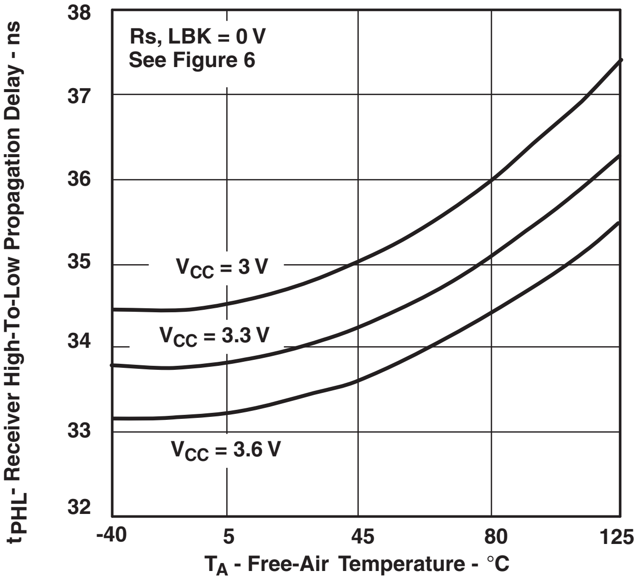


Figure 21.

TYPICAL CHARACTERISTICS (continued)

DRIVER LOW-TO-HIGH PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

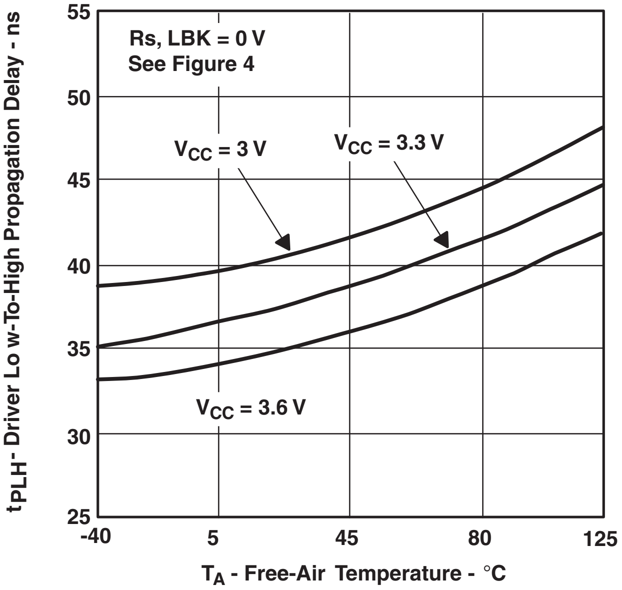


Figure 22.

DRIVER HIGH-TO-LOW PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

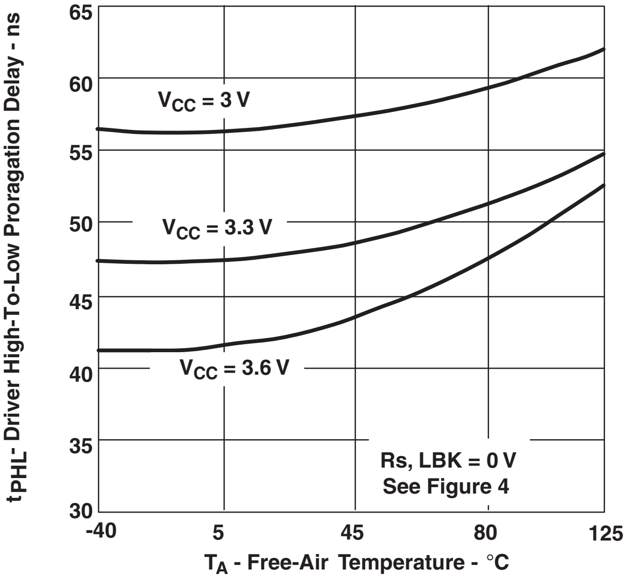


Figure 23.

DRIVER OUTPUT CURRENT
vs
SUPPLY VOLTAGE

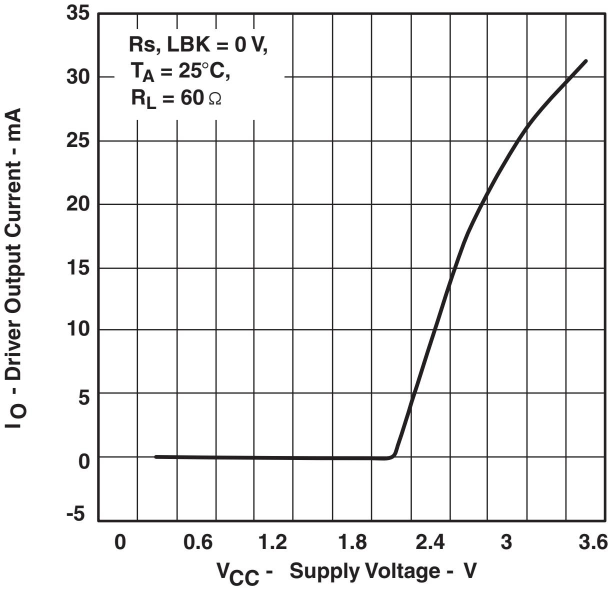


Figure 24.

APPLICATION INFORMATION

DIAGNOSTIC LOOPBACK (SN65HVD233)

The loopback function of the SN65HVD233 is enabled with a high-level input to LBK. This forces the driver into a recessive state and redirects the data (D) input at pin 1 to the received-data output (R) at pin 4. This allows the host controller to input and read back a bit sequence to perform diagnostic routines without disturbing the CAN bus. A typical CAN bus application is displayed in Figure 25.

If the LBK pin is not used it may be tied to ground (GND). However, it is pulled low internally (defaults to a low-level input) and may be left open if not in use.

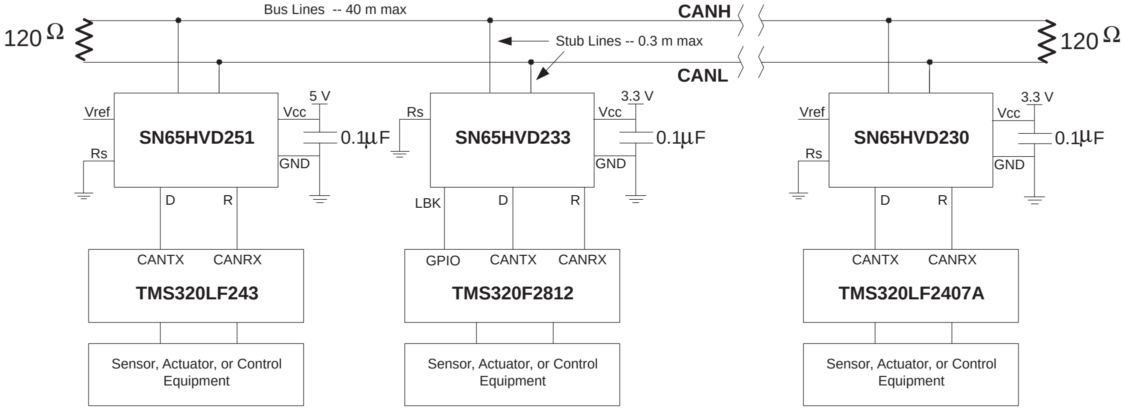


Figure 25. Typical HVD233 Application

ISO 11898 COMPLIANCE OF SN65HVD230 FAMILY OF 3.3-V CAN TRANSCEIVERS

Introduction

Many users value the low power consumption of operating their CAN transceivers from a 3.3 V supply. However, some are concerned about the interoperability with 5-V supplied transceivers on the same bus. This report analyzes this situation to address those concerns.

Differential Signal

CAN is a differential bus where complementary signals are sent over two wires and the voltage difference between the two wires defines the logical state of the bus. The differential CAN receiver monitors this voltage difference and outputs the bus state with a single-ended output signal.

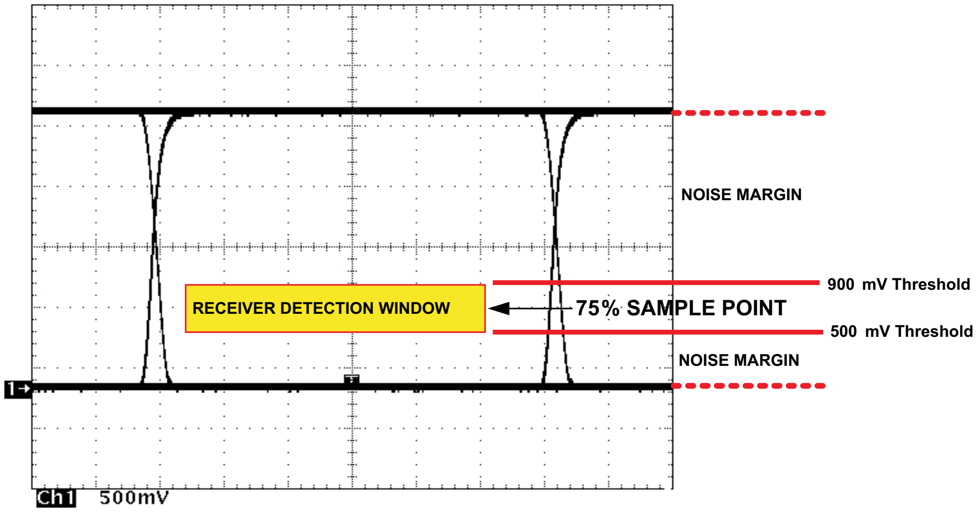


Figure 26. Typical SN65HVD230 Differential Output Voltage Waveform

The CAN driver creates the difference voltage between CANH and CANL in the dominant state. The dominant differential output of the SN65HVD230 is greater than 1.5 V and less than 3 V across a 60-ohm load. The minimum required by ISO 11898 is 1.5 V and maximum is 3 V. These are the same limiting values for 5-V supplied CAN transceivers. The bus termination resistors drive the recessive bus state and not the CAN driver.

A CAN receiver is required to output a recessive state with less than 500 mV and a dominant state with more than 900 mV difference voltage on its bus inputs. The CAN receiver must do this with common-mode input voltages from -2 V to 7 V. The SN65HVD230 family receivers meet these same input specifications as 5-V supplied receivers.

Common-Mode Signal

A common-mode signal is an average voltage of the two signal wires that the differential receiver rejects. The common-mode signal comes from the CAN driver, ground noise, and coupled bus noise. Obviously, the supply voltage of the CAN transceiver has nothing to do with noise. The SN65HVD230 family driver lowers the common-mode output in a dominant bit by a couple hundred millivolts from that of most 5-V drivers. While this does not fully comply with ISO 11898, this small variation in the driver common-mode output is rejected by differential receivers and does not effect data, signal noise margins or error rates.

Interoperability of 3.3-V CAN in 5-V CAN Systems

The 3.3-V supplied SN65HVD23x family of CAN transceivers are electrically interchangeable with 5-V CAN transceivers. The differential output is the same. The recessive common-mode output is the same. The dominant common-mode output voltage is a couple hundred millivolts lower than 5-V supplied drivers, while the receivers exhibit identical specifications as 5-V devices.

Electrical interoperability does not assure interchangeability however. Most implementers of CAN buses recognize that ISO 11898 does not sufficiently specify the electrical layer and that strict standard compliance alone does not ensure interchangeability. This comes only with thorough equipment testing.

BUS CABLE

The ISO-11898 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m with a maximum of 30 nodes. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires a transceiver with high input impedance such as the SN65HVD233.

The standard specifies the interconnect to be a single twisted-pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections.

SLOPE CONTROL

The rise and fall slope of the SN65HVD233 driver output can be adjusted by connecting a resistor from R_s (pin 8) to ground (GND), or to a low-level input voltage as shown in Figure 27.

The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor value of 10 kΩ to achieve a ≈15 V/µs slew rate, and up to 100 kΩ to achieve a ≈2.0 V/µs slew rate as displayed in Figure 28. Typical driver output waveforms with slope control are displayed in Figure 29.

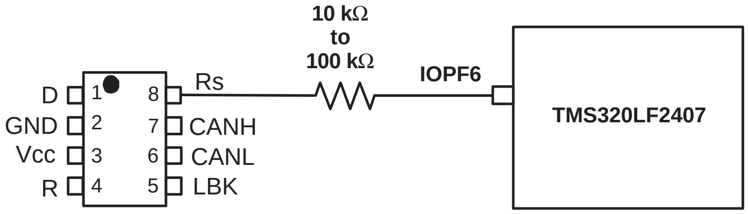


Figure 27. Slope Control/Standby Connection to a DSP

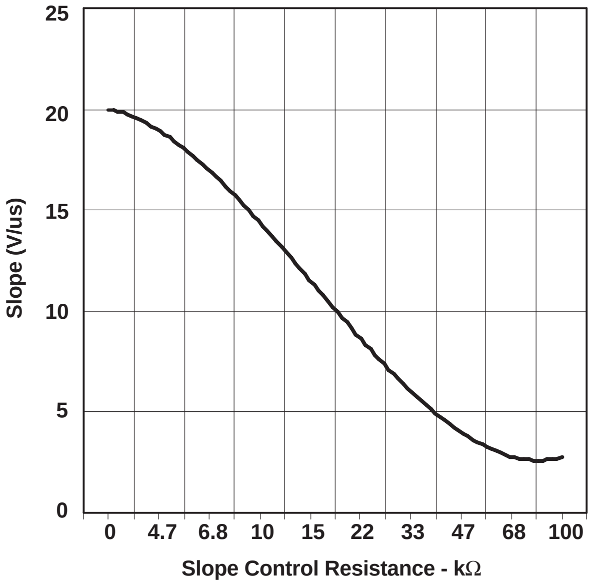


Figure 28. SN65HVD233 Driver Output Signal Slope vs Slope Control Resistance Value

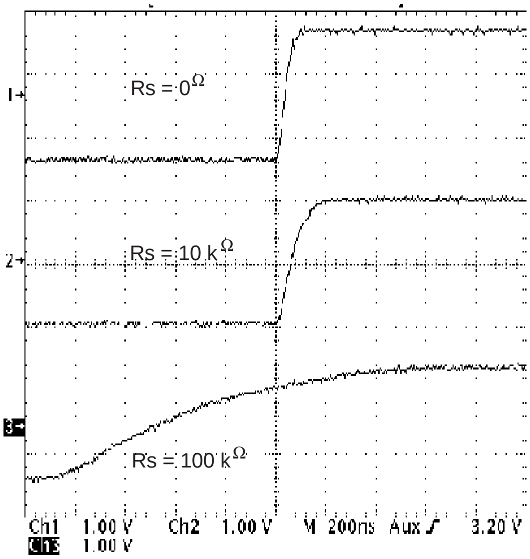


Figure 29. Typical SN65HVD233 250-kbps Output Pulse Waveforms With Slope Control

STANDBY

If a high-level input (> 0.75 V_{CC}) is applied to Rs (pin 8), the circuit enters a low-current, *listen only* standby mode during which the driver is switched off and the receiver remains active. The local controller can reverse this low-power standby mode when the rising edge of a dominant state (bus differential voltage >900 mV typical) occurs on the bus.

PACKAGE OPTION ADDENDUM

31-May-2014

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD233MDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	H233EP	Samples
V62/09611-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	H233EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN65HVD233-EP :

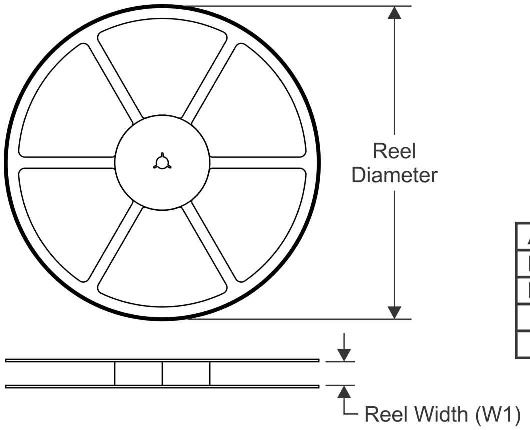
- Catalog: SN65HVD233

NOTE: Qualified Version Definitions:

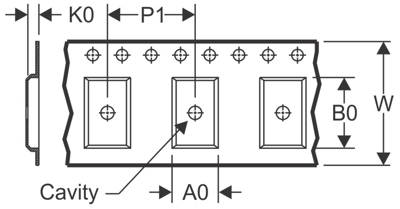
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

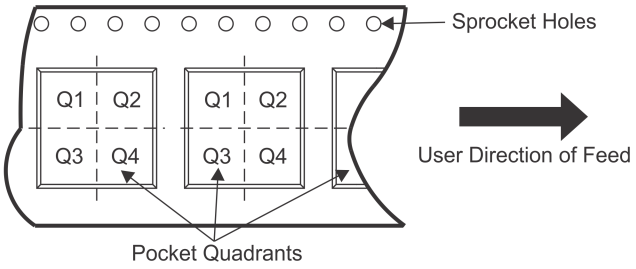


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

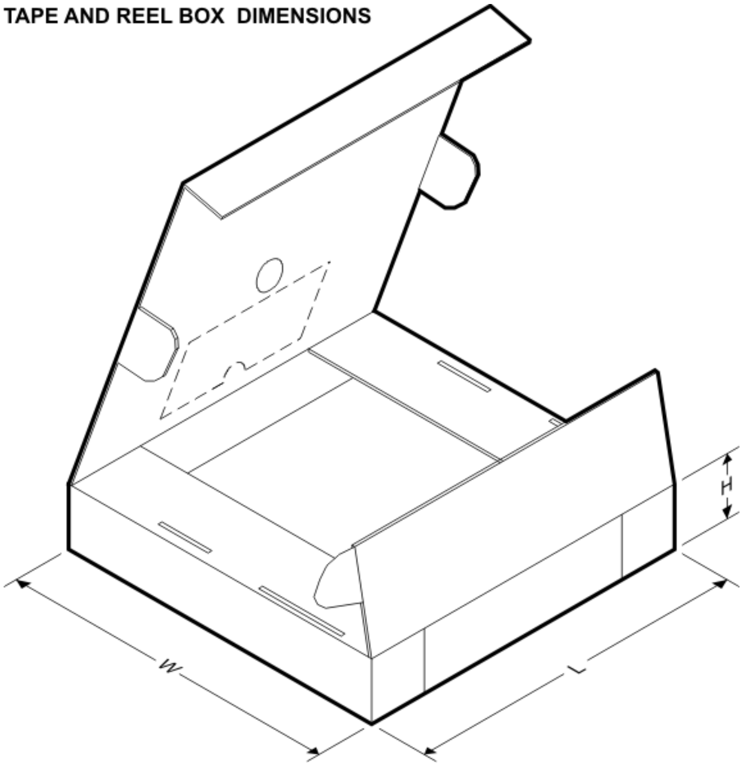
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD233MDREP	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

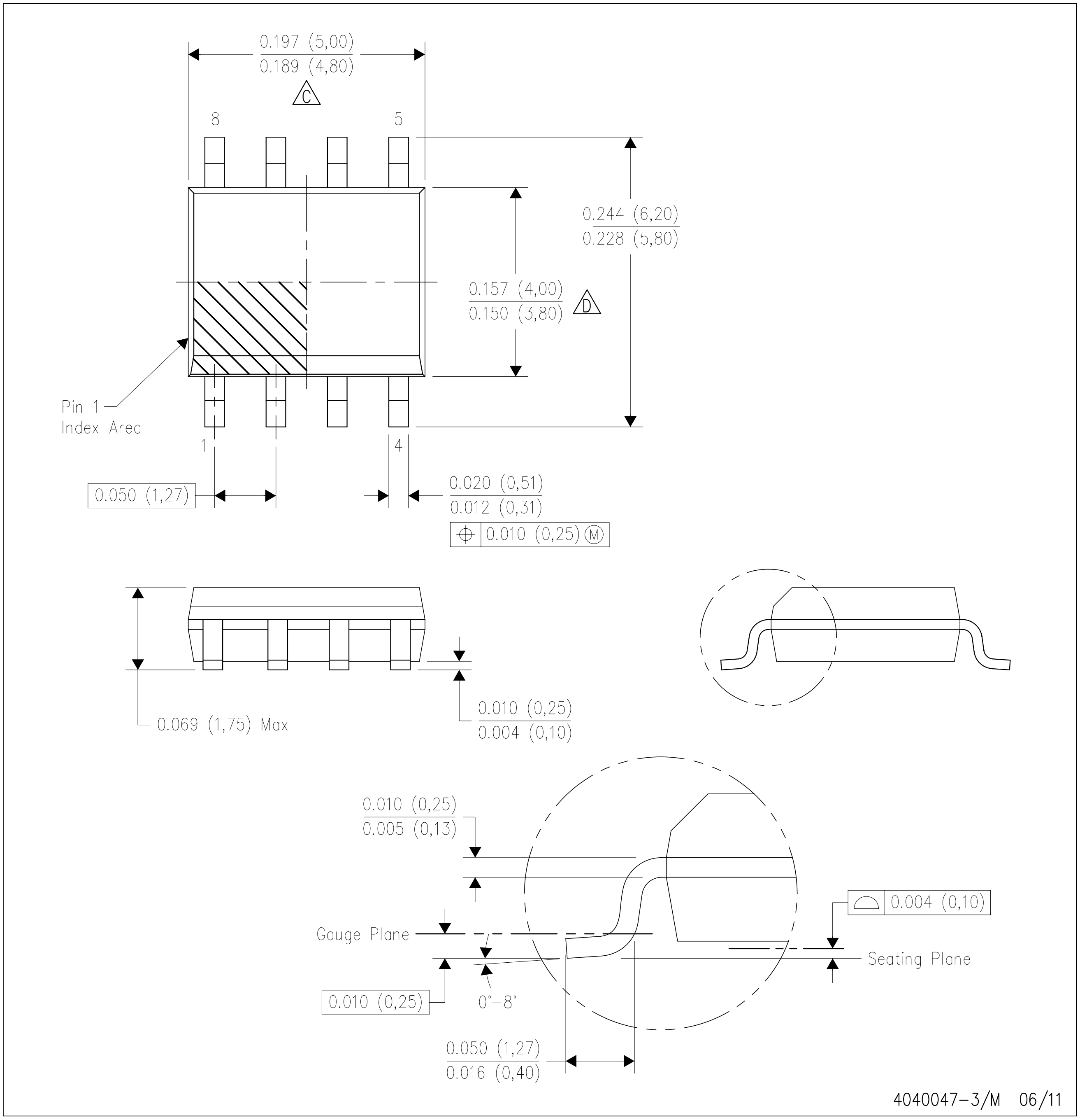
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

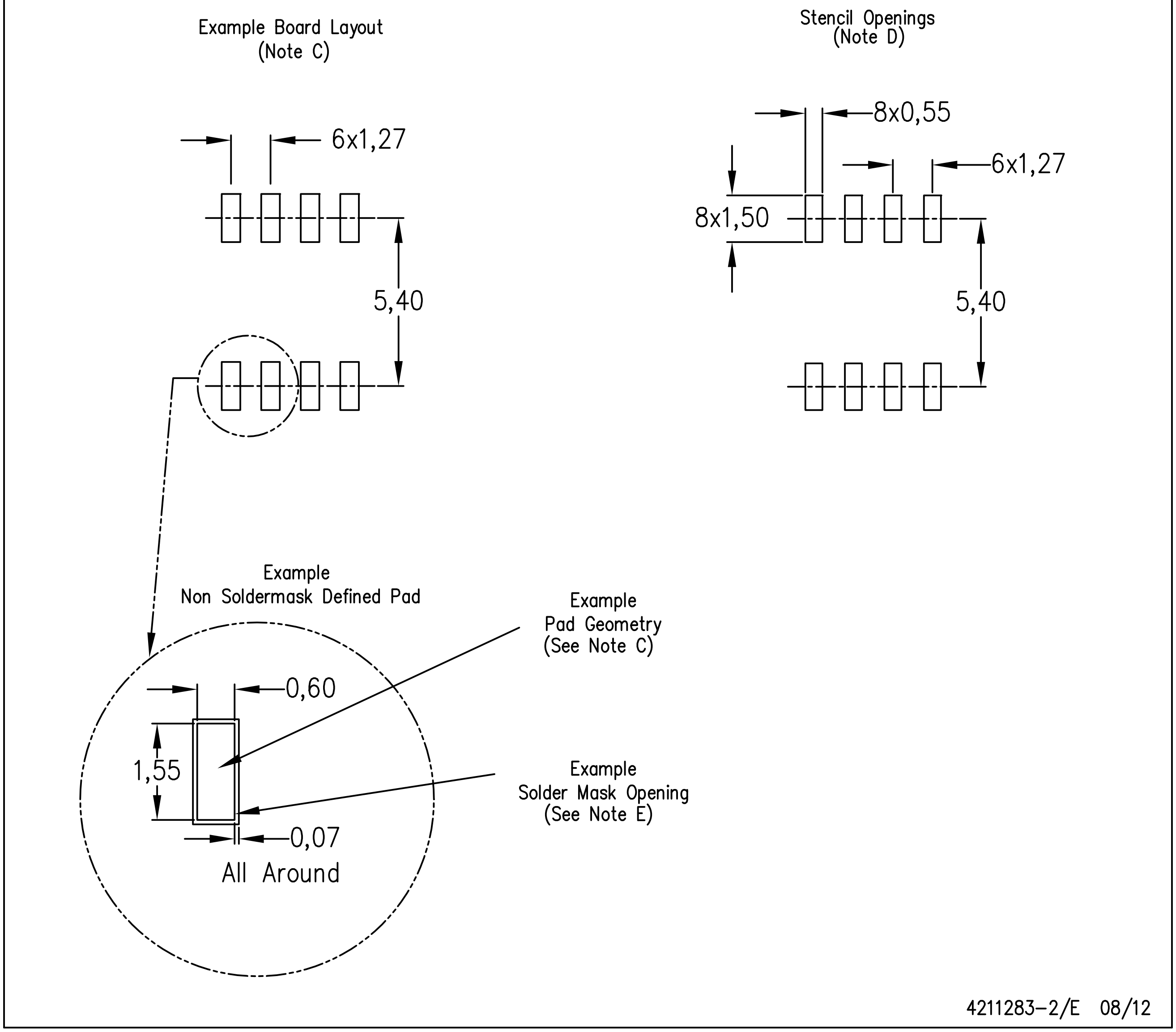
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD233MDREP	SOIC	D	8	2500	340.5	338.1	20.6

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- △D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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