

## Gigabit 4 x 4 CROSSPOINT SWITCH

### FEATURES

- Up to 2.5-Gbps Operation
- Non-Blocking Architecture Allows Each Output to Be Connected to Any Input
- 30 ps of Deterministic Jitter
- Selectable Transmit Preemphasis Per Lane
- Selectable Receive Equalization
- Available Packaging: 48-Pin QFN
- Propagation Delay Times: 500 ps Typical
- Inputs Electrically Compatible With CML Signal Levels
- Operates From a Single 3.3-V Supply
- Ability to Place Outputs in High-Impedance State
- Low Power: 560 mW
- Integrated Termination Resistors

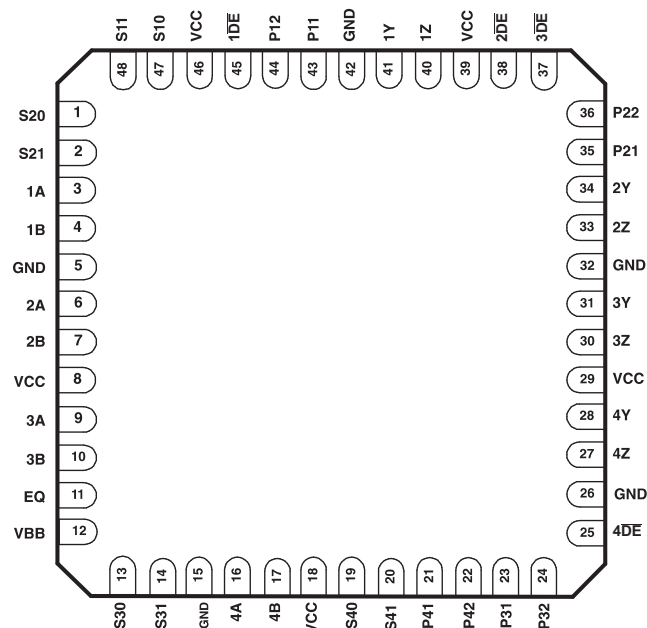
### APPLICATIONS

- Clock Buffering/Clock MUXing
- Wireless Base Stations
- High-Speed Network Routing
- Telecom/Datacom

### DESCRIPTION

The SN65LVCP204 is a 4x4 non-blocking crosspoint switch in a flow-through pinout that allows for ease in PCB layout. VML signaling is used to achieve a high-speed data throughput while using low power. Each of the output drivers includes a 4:1 multiplexer to allow any input to be routed to any output. Internal signal paths are fully differential to achieve high signaling speeds while maintaining low signal skews. The SN65LVCP204 incorporates 100-Ω termination resistors for those applications where board space is at a premium. Transmit preemphasis and receive equalization are built in for superior signal integrity performance.

The SN65LVCP204 is characterized for operation from –40°C to 85°C.

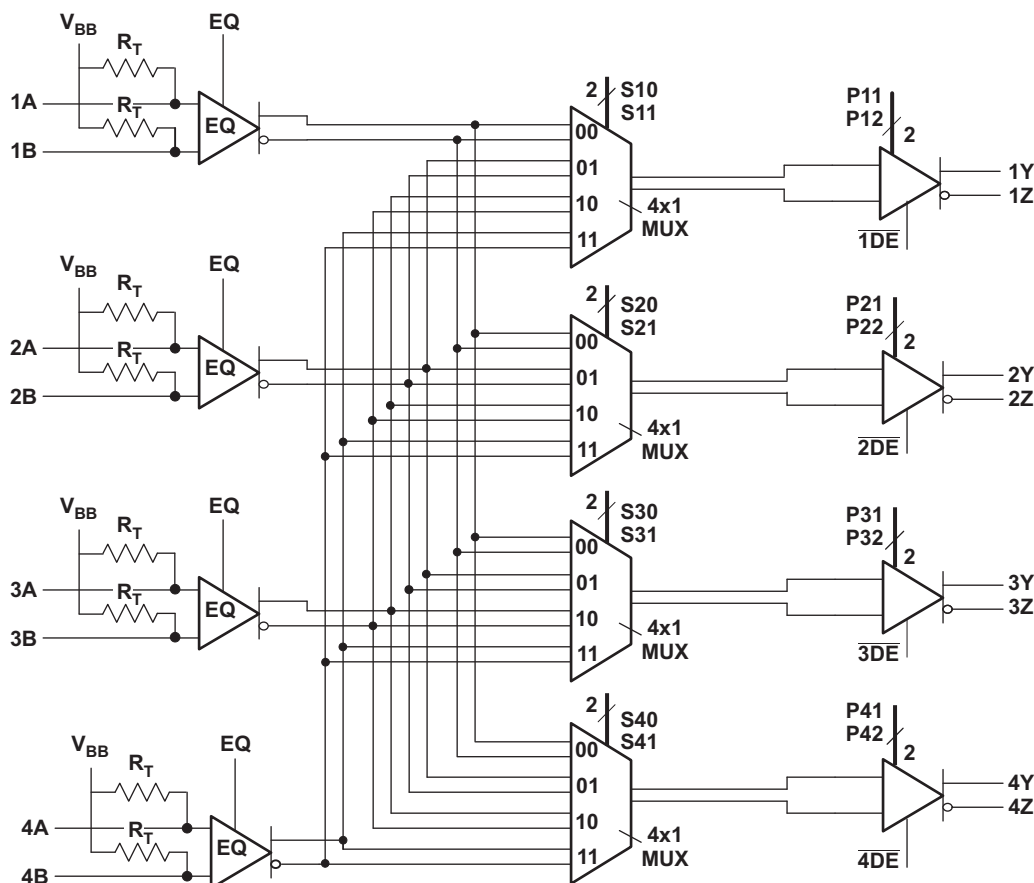


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### LOGIC DIAGRAM



**Note:**

**V<sub>BB</sub>:** Receiver input internal biasing voltage (allows ac coupling)

**EQ:** Input equalizer (compensates for frequency dependent transmission line loss of backplanes)

**R<sub>T</sub>:** Internal 50-Ω receiver termination (100-Ω differential)

**Preemphasis:** Output precompensation for transmission line losses

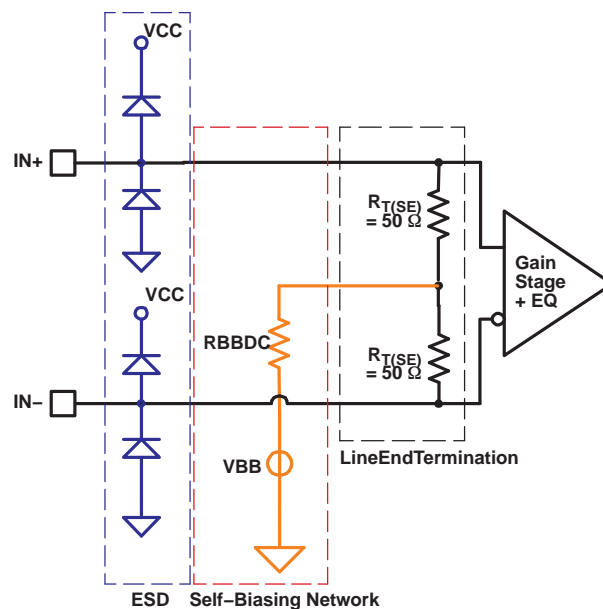
### TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
High Speed I/O			
xA xB	3, 6, 9, 16 4, 7, 10, 17	Differential inputs (with 50-Ω termination to V <sub>BB</sub> ) xA = P; xB = N	Line-side differential inputs, CML compatible
xY xZ	41, 34, 31, 28 40, 33, 30, 27	Differential output xY = P; xZ = N	Switch-side differential outputs, VML
Control Signals			
x $\overline{\text{DE}}$	45, 38, 37, 25	Input	Data enable; active low; LVTTTL; when not enabled, the ouput is in the high-impedance state for power savings.
S10–S41	47, 48, 1, 2, 13, 14, 19, 20	Input; S1x = channel 1, bit x	Switching selection; LVTTTL

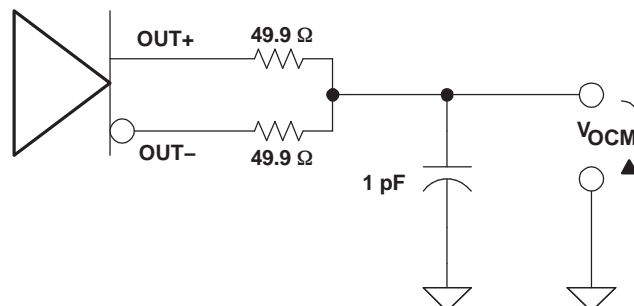
### TERMINAL FUNCTIONS (continued)

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
P11–P42	43, 44, 35, 36, 23, 24, 21, 22	Input; P1x = channel 1, bit x	Output preemphasis control; LVTTTL
EQ	11	Input; selection for receive equalization setting	EQ = 1 (default) is for the 5-dB setting, EQ = 0 is for the 12-dB setting
<b>Power Supply</b>			
VCC	8, 18, 29, 39, 46	Power	Power supply 3.3 V $\pm 5\%$
GND	5, 15, 26, 32, 42		Ground
Thermal pad			The ground center pad of the package must be connected to GND plane.
V <sub>BB</sub>	12	Input	Receiver input biasing voltage

### EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



**Figure 1. Equivalent Input Circuit Design**



**Figure 2. Common-Mode Output Voltage Test Circuit**

**Table 1. CROSSPOINT LOGIC TABLES**

OUTPUT CHANNEL 1			OUTPUT CHANNEL 2			OUTPUT CHANNEL 3			OUTPUT CHANNEL 4		
CONTROL PINS		INPUT SELECTED	CONTROL PINS		INPUT SELECTED	CONTROL PINS		INPUT SELECTED	CONTROL PINS		INPUT SELECTED
S10	S11	1Y/1Z	S20	S21	2Y/2Z	S30	S31	3Y/3Z	S40	S41	4Y/4Z
0	0	1A/1B	0	0	1A/1B	0	0	1A/1B	0	0	1A/1B
0	1	2A/2B	0	1	2A/2B	0	1	2A/2B	0	1	2A/2B
1	0	3A/3B	1	0	3A/3B	1	0	3A/3B	1	0	3A/3B
1	1	4A/4B	1	1	4A/4B	1	1	4A/4B	1	1	4A/4B

**AVAILABLE OPTIONS**

T <sub>A</sub>	DESCRIPTION	PACKAGED DEVICE <sup>(1)</sup>
		RGZ (48-Pin) (Orderable)
–40°C to 85°C	Serial multiplexer	SN65LVCP204RGZ

(1) The package is available taped and reeled. Add an R suffix to device types (e.g., SN65LVCP204RGZR).

**PACKAGE THERMAL CHARACTERISTICS**

PACKAGE THERMAL CHARACTERISTICS <sup>(1)</sup>		NOM	UNIT
θ <sub>JA</sub> (junction-to-ambient)	Four-layer JEDEC board (JESD51-7) using eight GND-vias of 0.3-mm diameter on the center pad as shown in the section: <i>Recommended PCB footprint</i> with boundary and environment conditions of JEDEC board (JESD51-2)	33	°C/W
θ <sub>JB</sub> (junction-to-board)		20	°C/W
θ <sub>JC</sub> (junction-to-case)		23.6	°C/W
Ψ <sub>jt</sub> (junction-to-top pseudo)		0.6	°C/W
Ψ <sub>jb</sub> (junction-to-board pseudo)		19.4	°C/W
θ <sub>JP</sub> (junction-to-pad)		5.4	°C/W

(1) See the *IC Package Thermal Metrics* application report [SPRA953](#) for a detailed explanation of thermal parameters.

**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

				UNIT
V <sub>CC</sub>	Supply-voltage range <sup>(2)</sup>			–0.5 V to 6 V
Voltage range			Control inputs, all outputs	–0.5 V to (V <sub>CC</sub> + 0.5 V)
			Receiver inputs	–0.5 V to 4 V
ESD	Human-body model <sup>(3)</sup>		All pins	3 kV
	Charged-device model <sup>(4)</sup>		All pins	500 V
T <sub>J</sub>	Maximum junction temperature			See <i>Package Thermal Characteristics</i> table
Moisture sensitivity level				2
Reflow temperature package soldering, 4 seconds				260°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to the ground terminals.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.

(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

## RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
dR	Operating data rate				2.5	Gbps
V <sub>CC</sub>	Supply voltage		3.135	3.3	3.465	V
V <sub>CC(N)</sub>	Supply-voltage noise amplitude	10 Hz to 1.25 GHz			20	mV
T <sub>J</sub>	Junction temperature				125	°C
T <sub>A</sub>	Operating free-air temperature <sup>(1)</sup>		–40		85	°C
<b>DIFFERENTIAL INPUTS</b>						
V <sub>ID</sub>	Receiver peak-to-peak differential input voltage <sup>(2)</sup>	dR <sub>(in)</sub> ≤ 1.25 Gbps	100		1750	mV <sub>PP</sub>
		1.25 Gbps < dR <sub>(in)</sub> ≤ 2.5 Gbps	100		1560	mV <sub>PP</sub>
		dR <sub>(in)</sub> > 2.5 Gbps	100		1000	mV <sub>PP</sub>
V <sub>ICM</sub>	Receiver common-mode input voltage	Note: for best jitter performance, ac coupling is recommended.	1.5	1.6	V <sub>CC</sub> – $\frac{ V_{ID} }{2}$	V
<b>CONTROL INPUTS</b>						
V <sub>IH</sub>	High-level input voltage		2		V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Low-level input voltage		–0.3		0.8	V
<b>DIFFERENTIAL OUTPUTS</b>						
R <sub>L</sub>	Differential load resistance		80	100	120	Ω

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

(2) Differential input voltage V<sub>ID</sub> is defined as |IN+ – IN–|.

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>DIFFERENTIAL INPUTS</b>					
V <sub>IT+</sub>	Positive-going differential input, high threshold			50	mV
V <sub>IT–</sub>	Negative-going differential input, low threshold	–50			mV
A <sub>(EQ)</sub>	Equalizer gain	at 1.25 GHz (EQ = 0)	12		dB
R <sub>T(D)</sub>	Termination resistance, differential	80	100	120	Ω
V <sub>BB</sub>	Open-circuit input voltage (input self-bias voltage)	AC-coupled inputs	1.6		V
R <sub>(BBDC)</sub>	Biasing network dc impedance		30		kΩ
R <sub>(BBAC)</sub>	Biasing network ac impedance	375 MHz	42		Ω
<b>DIFFERENTIAL OUTPUTS</b>					
V <sub>ODH</sub>	High-level output voltage	R <sub>L</sub> = 100 Ω ±1%, Px2 = Px1 = 0; 2.5 Gbps alternating 1010-pattern; <a href="#">Figure 3</a>	650		mV <sub>PP</sub>
V <sub>ODL</sub>	Low-level output voltage		–650		mV <sub>PP</sub>
V <sub>ODB(PP)</sub>	Output differential voltage without preemphasis <sup>(2)</sup>		1000	1300 1500	mV <sub>PP</sub>
V <sub>OCM</sub>	Output common-mode voltage	See <a href="#">Figure 2</a>	1.65		V
ΔV <sub>OC(SS)</sub>	Change in steady-state common-mode output voltage between logic states		1		mV

(1) All typical values are at T<sub>A</sub> = 25°C and V<sub>CC</sub> = 3.3-V supply unless otherwise noted. They are for reference purposes and are not production tested.

(2) Differential output voltage V<sub>ODB</sub> is defined as |OUT+ – OUT–|.

## ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>(PE)</sub>	Output preemphasis voltage $\frac{V_{\text{ODB(PP)}}}{V_{\text{ODPE(PP)}}}$ ratio,	R <sub>L</sub> = 100 Ω±1%; x = L or S; See <a href="#">Figure 3</a>	Px2:Px1 = 00		0		dB
			Px2:Px1 = 01		3		
			Px2:Px1 = 10		6		
			Px2:Px1 = 11		9		
t <sub>(PRE)</sub>	Preemphasis duration measurement	Output preemphasis is set to 9 dB during test; Pxx = 1; Measured with a 100-MHz clock signal; R <sub>L</sub> = 100 Ω ±1%, See <a href="#">Figure 4</a>			175		ps
R <sub>O</sub>	Output resistance	Differential on-chip termination between OUT+ and OUT–			100		Ω
CONTROL INPUTS							
I <sub>IH</sub>	High-level input current	V <sub>IN</sub> = VCC				5	μA
I <sub>IL</sub>	Low-level input current	V <sub>IN</sub> = GND		–125	–90		μA
R <sub>(PU)</sub>	Pullup resistance				35		kΩ
POWER CONSUMPTION							
P <sub>D</sub>	Device power dissipation	All outputs terminated 100 Ω			560	750	mW
P <sub>Z</sub>	Device power dissipation in high-impedance state	All outputs in high-impedance state				600	mW
I <sub>CC</sub>	Device current consumption	All outputs terminated 100 Ω PRBS 2 <sup>7</sup> – 1 pattern at 2.5 Gbps				220	mA

## SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>MULTIPLEXER</b>						
$t_{(SM)}$	Multiplexer switch time	Multiplexer to valid output		3	6	ns
<b>DIFFERENTIAL OUTPUTS</b>						
$t_{PLH}$	Low-to-high propagation delay	Propagation delay, input to output See <a href="#">Figure 6</a>		0.5	0.7	ns
$t_{PHL}$	High-to-low propagation delay			0.5	0.7	ns
$t_r$	Rise time	20% to 80% of $V_{O(DB)}$ ; test pattern: 100-MHz clock signal; see <a href="#">Figure 5</a> and <a href="#">Figure 8</a>		110		ps
$t_f$	Fall time			110		ps
$t_{sk(p)}$	Pulse skew, $ t_{PHL} - t_{PLH} ^{(2)}$				20	ps
$t_{sk(o)}$	Output skew <sup>(3)</sup>	All outputs terminated with 100 $\Omega$		25	100	ps
$t_{sk(pp)}$	Part-to-part skew <sup>(4)</sup>				300	ps
$t_{zd}$	Switch time, hi-Z state to disable	50 $\Omega$ to $V_{cm}$ and 150-pF load on each output			20	ns
$t_{ze}$	Switch time, hi-Z state to enable	50 $\Omega$ to $V_{cm}$ and 150-pF load on each output			10	ns
RJ	Device random jitter, rms	See <a href="#">Figure 8</a> for test circuit. BERT setting 10 <sup>–15</sup> Alternating 10-pattern.		0.8	2	ps-rms

(1) All typical values are at 25°C and with 3.3-V supply, unless otherwise noted.

(2)  $t_{sk(p)}$  is the magnitude of the time difference between the  $t_{PLH}$  and  $t_{PHL}$  of any output of a single device.

(3)  $t_{sk(o)}$  is the magnitude of the time difference between the  $t_{PLH}$  and  $t_{PHL}$  of any two outputs of a single device.

(4)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

**SWITCHING CHARACTERISTICS (continued)**

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP <sup>(1)</sup>	MAX	UNIT
DJ	Intrinsic deterministic device jitter <sup>(5)(6)</sup> , peak-to-peak	0 dB preemphasis (PREx_x = 0); See Figure 8 for the test circuit.	PRBS 2 <sup>7</sup> – 1 pattern	2.5 Gbps			30	ps
	Absolute deterministic output jitter <sup>(7)</sup> , peak-to-peak	0 dB preemphasis (PREx_x = 0); See Figure 8 for the test circuit.	PRBS 2 <sup>7</sup> – 1 pattern	1.25 Gbps; EQ = 1 Over 25-inch (63,5-cm) FR4 trace		7		ps

- (5) Intrinsic deterministic device jitter is a measurement of the deterministic jitter contribution from the device. It is derived by the equation  $(DJ_{(OUT)} - DJ_{(IN)})$ , where  $DJ_{(OUT)}$  is the total peak-to-peak deterministic jitter measured at the output of the device in PSPP.  $DJ_{(IN)}$  is the peak-to-peak deterministic jitter of the pattern generator driving the device.
- (6) The SN65LVCP204 built-in passive input equalizer compensates for ISI. For a 25-inch (63,5-cm) FR4 transmission line with 8-mil (0,2-mm) trace width, the SN65LVCP204 typically reduces jitter by 60 ps from the device input to the device output.
- (7) Absolute deterministic output jitter reflects the deterministic jitter measured at the SN65LVCP204 output. The value is a real value measured with a bit-error tester as described in Figure 8. The absolute DJ reflects the sum of all deterministic jitter components accumulated over the link:  $DJ_{(absolute)} = DJ_{(Signal\ generator)} + DJ_{(transmission\ line)} + DJ_{(intrinsic(LVCP204))}$ .

**Table 2. Preemphasis Controls PL2, PL1, PS2, and PS1**

Px2 <sup>(1)</sup>	Px1 <sup>(1)</sup>	OUTPUT PREEMPHASIS LEVEL IN dB	OUTPUT LEVEL IN mVpp		TYPICAL FR4 TRACE LENGTH
			DE-EMPHASIZED	PREEMPHASIZED	
0	0	0 dB	1200	1200	10 inches (25,4 cm) of FR4 trace
0	1	3 dB	850	1200	20 inches (50,8 cm) of FR4 trace
1	0	6 dB	600	1200	30 inches (76,2 cm) of FR4 trace
1	1	9 dB	425	1200	40 inches (101,6 cm) of FR4 trace

(1) x = L or S

**Table 3. Receive Equalization Settings**

EQ	EQUALIZATION	TYPICAL TRACE
1	5 dB	25 inches (63,5 cm) of FR4
0	12 dB	43 inches (109,2 cm) of FR4

## PARAMETER MEASUREMENT INFORMATION

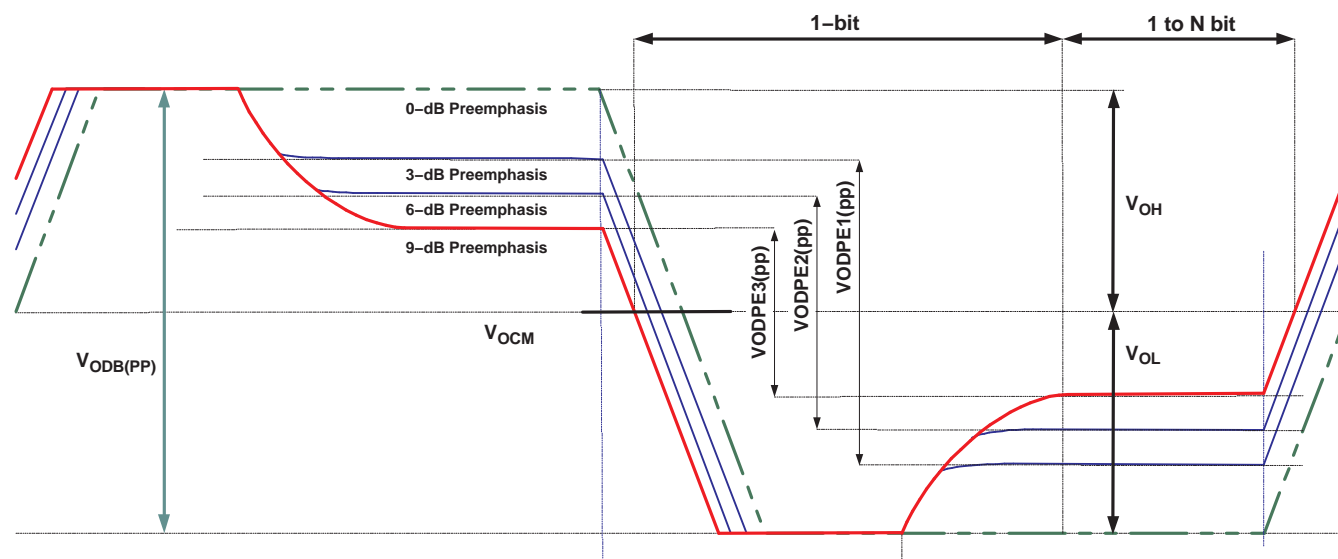


Figure 3. Preemphasis and Output Voltage Waveforms and Definitions

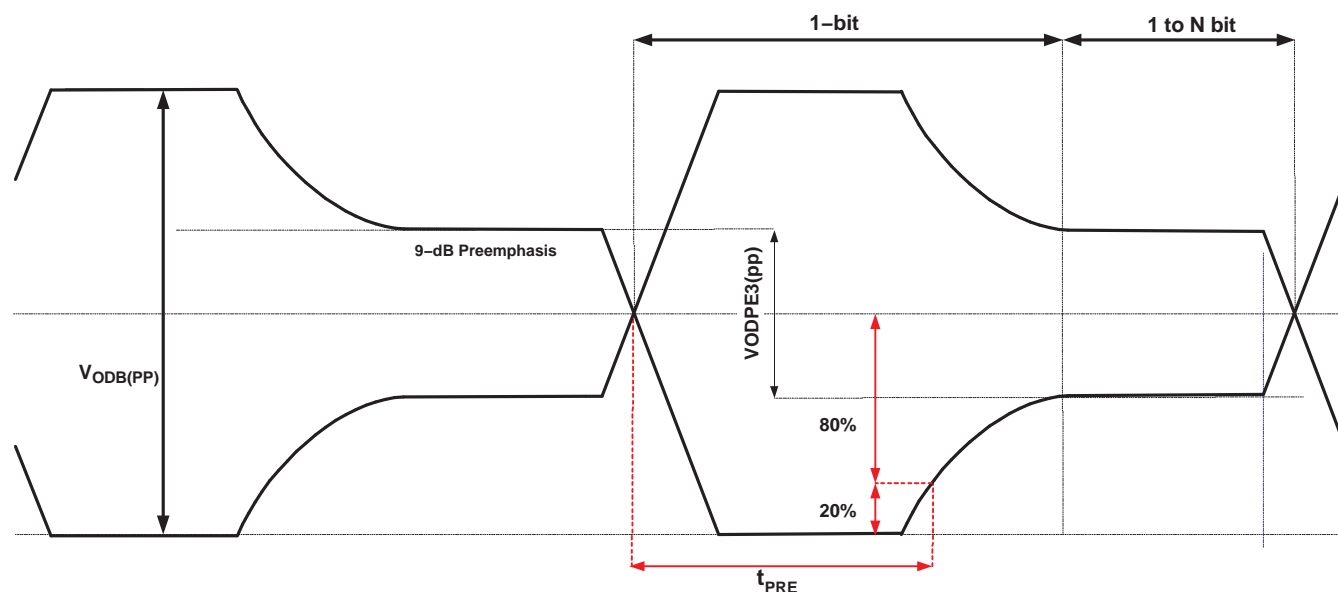


Figure 4.  $t_{PRE}$  Preemphasis Duration Measurement

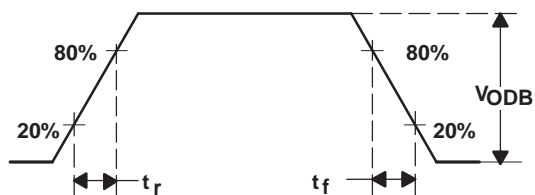


Figure 5. Driver Output Transition Time



## PARAMETER MEASUREMENT INFORMATION (continued)

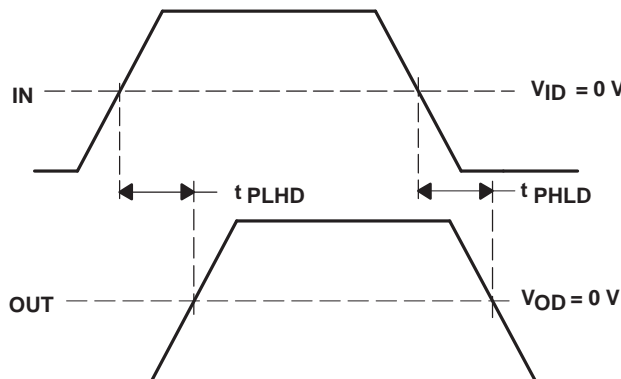
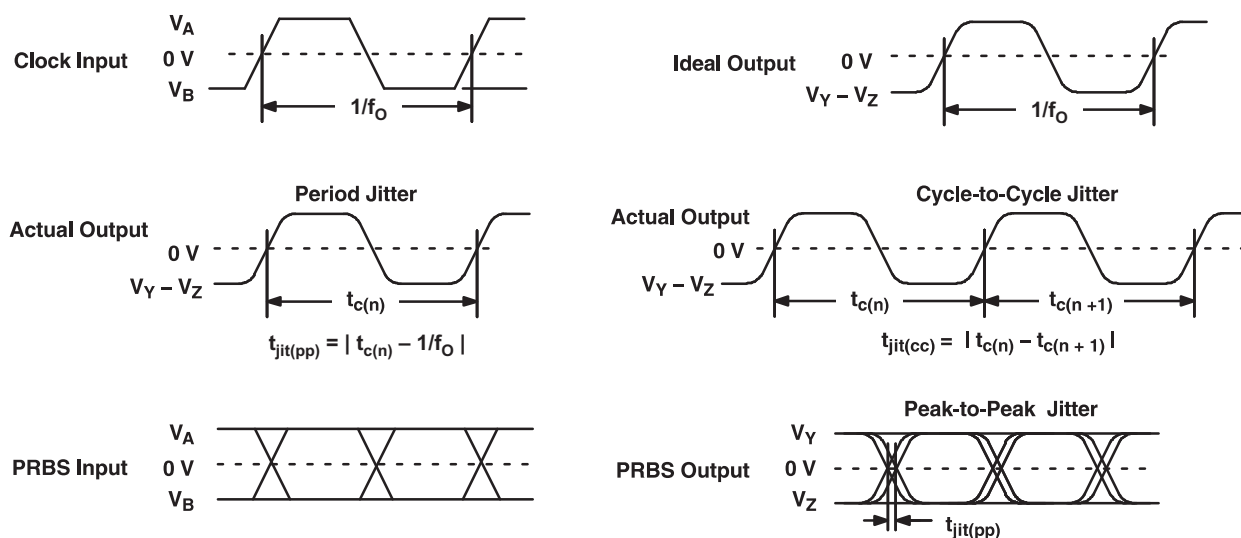


Figure 6. Propagation Delay Input to Output



- A. All input pulses are supplied by an Agilent 81250 Stimulus System.  
B. The measurement is made with the AgilentParBert measurement software.

Figure 7. Driver Jitter Measurement Waveforms

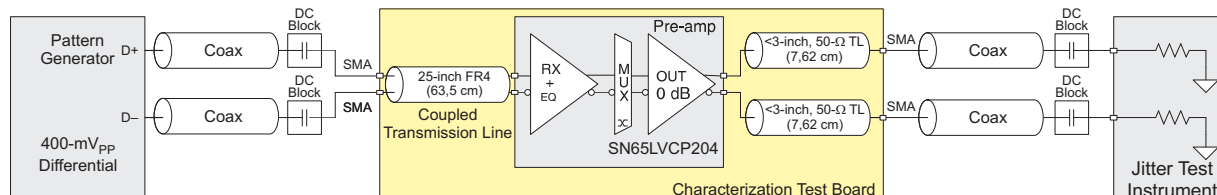
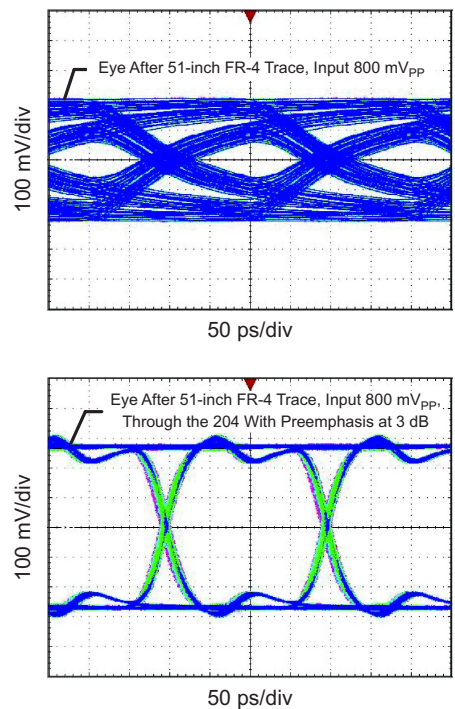


Figure 8. AC Test Circuit — Jitter and Output Rise Time Test Circuit

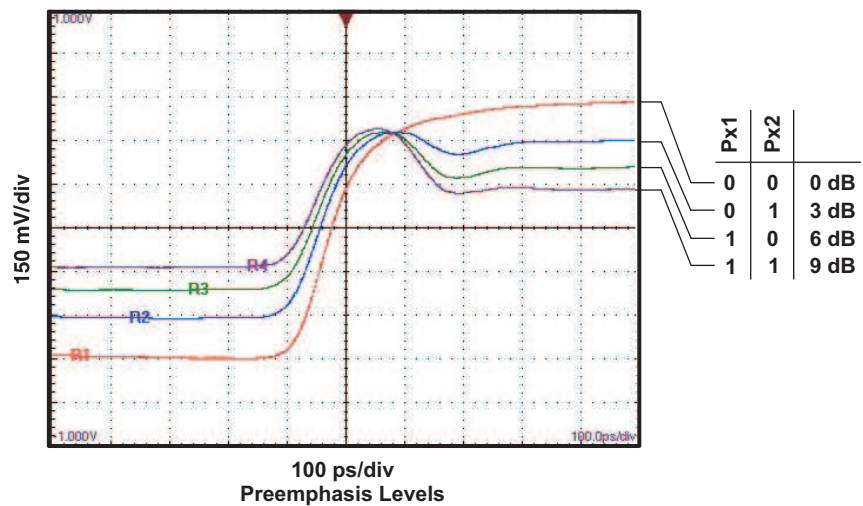
The SN65LVCP204 input equalizer provides 5-dB frequency gain to compensate for the frequency loss of a shorter backplane transmission line. For characterization purposes, a 25-inch (63.5 cm) FR-4 coupled transmission line is used in place of the backplane trace. The 25-inch trace provides roughly 5 dB of attenuation between 375 MHz and 2.125 GHz, representing closely the characteristics of a short backplane trace. The loss tangent of the FR4 in the test board is 0.018 with an effective  $\epsilon(r)$  of 4.1.

**TYPICAL DEVICE BEHAVIOR**

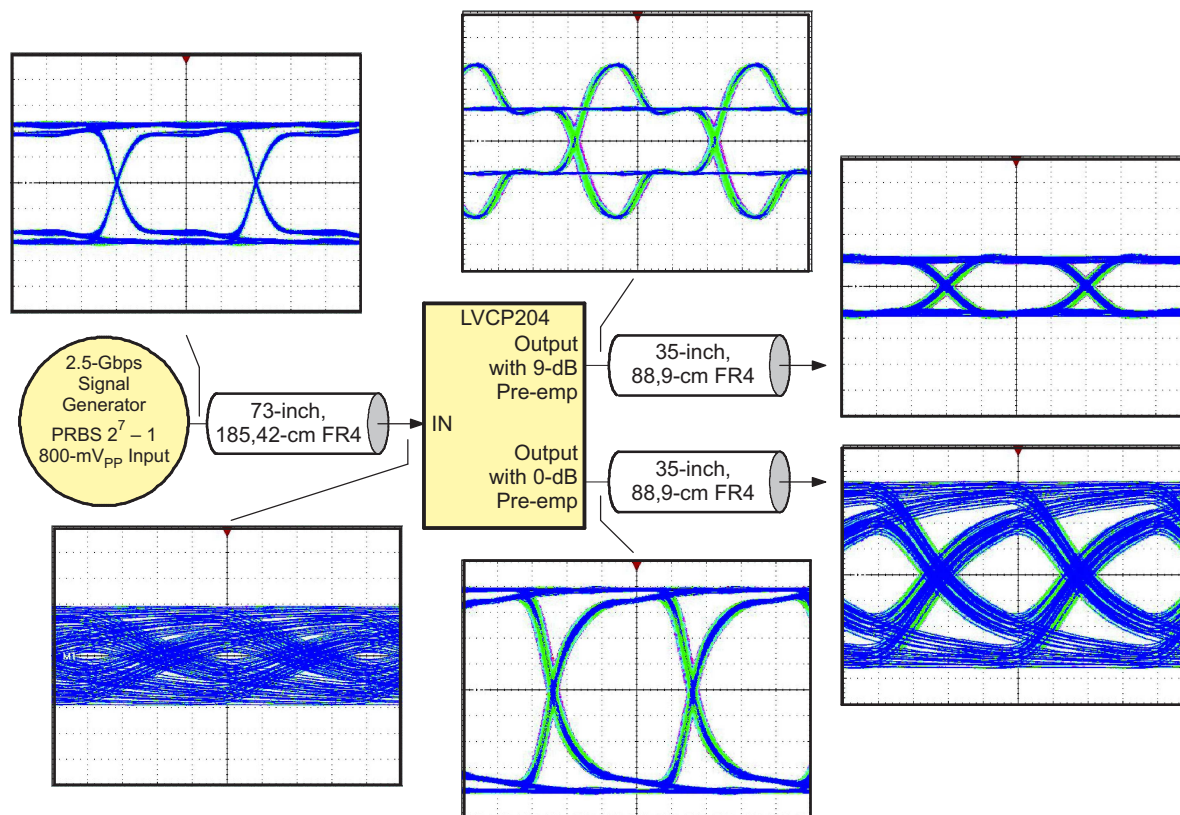


NOTE: 51-Inch (129,54-cm) input trace, dR = 2.5 Gbps;  $2^7 - 1$  PRBS

**Figure 9. Data Input and Output Pattern**



**Figure 10. Preemphasis Signal Shape**



**Figure 11. Data Output Pattern**

## TYPICAL CHARACTERISTICS

**DETERMINISTIC OUTPUT JITTER  
vs  
DATA RATE**

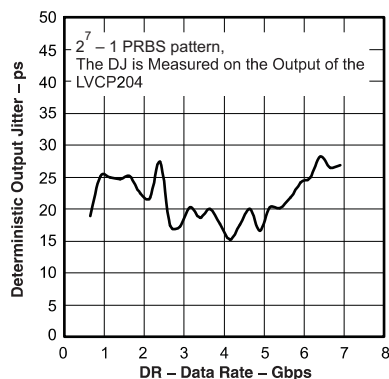


Figure 12.

**DETERMINISTIC OUTPUT JITTER  
vs  
DIFFERENTIAL INPUT AMPLITUDE**

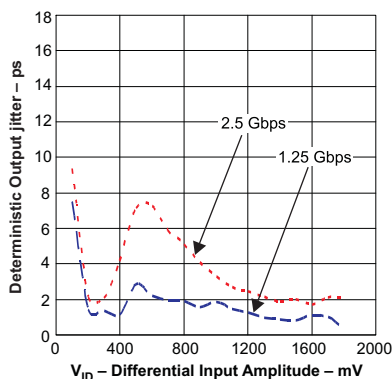


Figure 13.

**DIFFERENTIAL OUTPUT VOLTAGE  
vs  
DATA RATE**

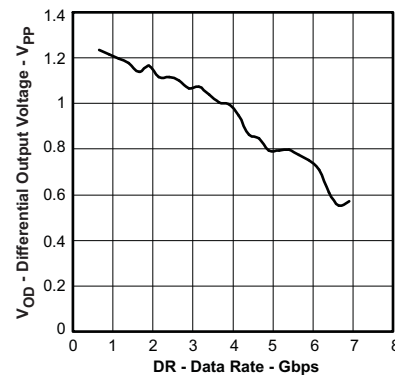


Figure 14.

**DETERMINISTIC OUTPUT JITTER  
vs  
DATA RATE  
(SUPPLY NOISE IMPACT)**

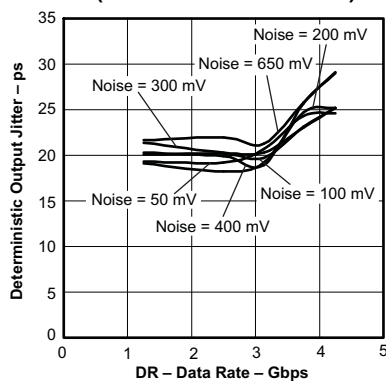


Figure 15.

**DETERMINISTIC OUTPUT JITTER  
vs  
COMMON-MODE INPUT VOLTAGE**

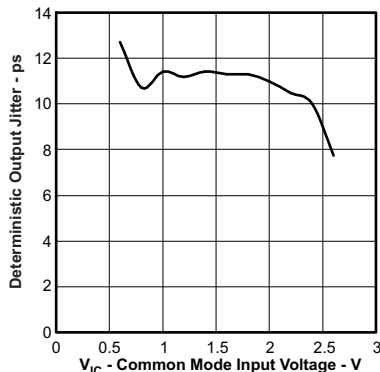
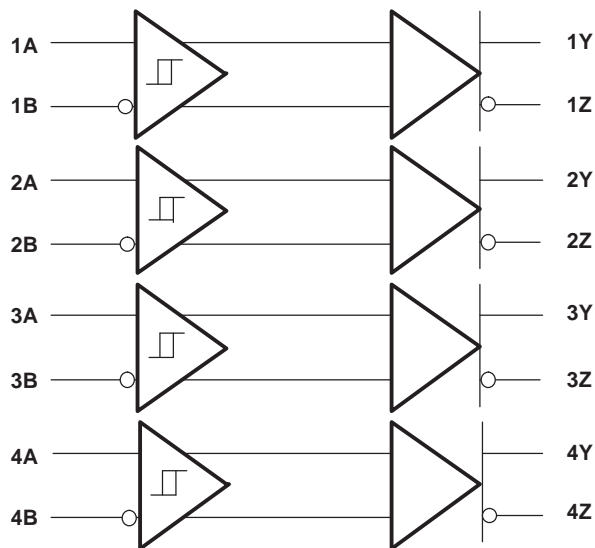


Figure 16.

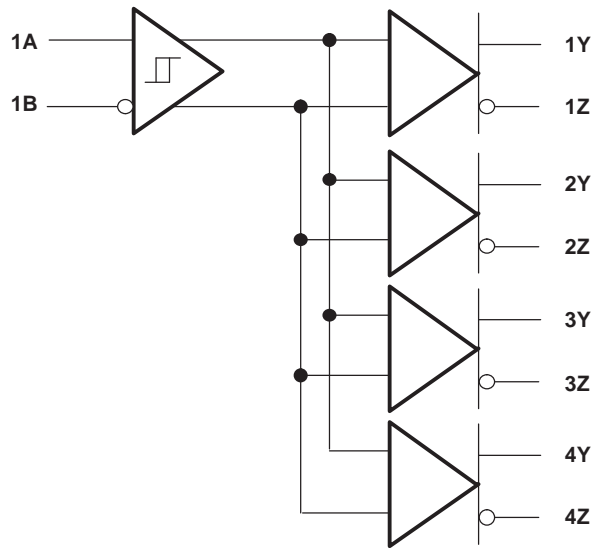
## APPLICATION INFORMATION

### CONFIGURATION EXAMPLES

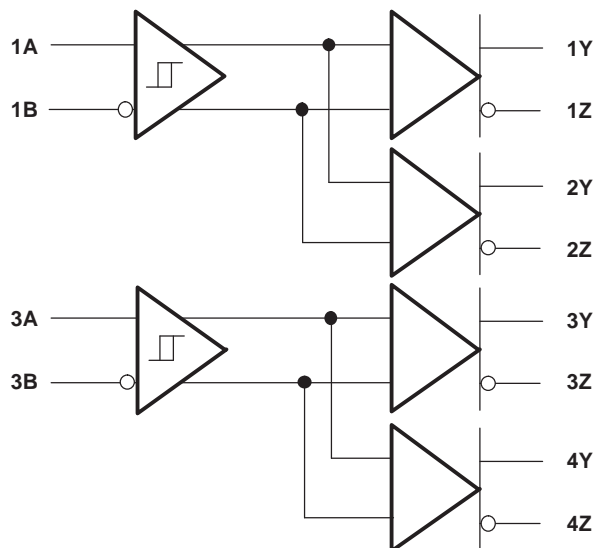
S10	S11	S20	S21
0	0	0	1
S30	S31	S40	S41
1	0	1	1



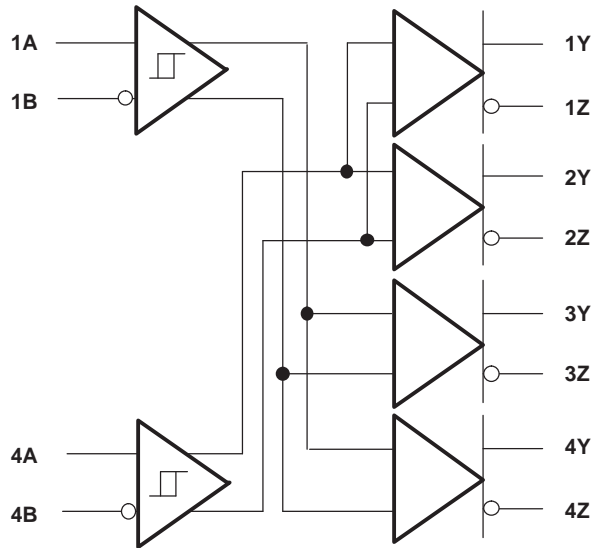
S10	S11	S20	S21
0	0	0	0
S30	S31	S40	S41
0	0	0	0



S10	S11	S20	S21
0	0	0	0
S30	S31	S40	S41
1	0	1	0



S10	S11	S20	S21
1	1	1	1
S30	S31	S40	S41
0	0	0	0



## EXPLANATION OF EQUALIZATION

Backplane designs differ widely in size, layer stackup, and connector placement. In addition, the performance is impacted by trace architecture (trace width, coupling method) and isolation from adjacent signals. Common to most commercial backplanes is the use of FR4 as board material, with its related high-frequency signal attenuation. Within a backplane, the shortest to longest trace lengths differ substantially, often ranging from 8 inches (20,3 cm) up to 40 inches (101,6 cm). Increased loss is associated with longer signal traces. In addition, the backplane connector often contributes a good amount of signal attenuation. As a result, the signal attenuation for a 300-MHz signal might range from 1 dB to 4 dB, whereas the corresponding attenuation for a 2-GHz signal might span 6 dB to 24 dB. This frequency-dependent loss causes distortion jitter on the transmitted signal. Each SN65LVCP204 receiver input incorporates an equalizer and compensates for such frequency loss. The SN65LVCP204 equalizer provides 5 dB or 12 dB of frequency gain between 375 MHz and 1.875 GHz, compensating roughly for 20 inches (50,8 cm) of FR4 material with 8-mil (0,2-mm) trace width. Distortion jitter improvement is substantial, often providing more than 30-ps jitter reduction. The 5-dB compensation is sufficient for most short backplane traces. For longer trace lengths, it is recommended to enable transmit preemphasis in addition.

## SETTING THE PREEMPHASIS LEVEL

The receive equalization compensates for ISI. This reduces jitter and opens the data eye. In order to find the best preemphasis setting for each link, calibration of every link is recommended. Assuming each link consists of a transmitter (with adjustable preemphasis, such as the SN65LVCP204) and the SN65LVCP204 receiver, the following steps are necessary:

1. Set the transmitter and receiver to 0-dB preemphasis; record the data eye on the SN65LVCP204 receiver output.
2. Increase the transmitter preemphasis until the data eye on the SN65LVCP204 receiver output looks the cleanest.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65LVCP204RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	LVCP204	<a href="#">Samples</a>
SN65LVCP204RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	LVCP204	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

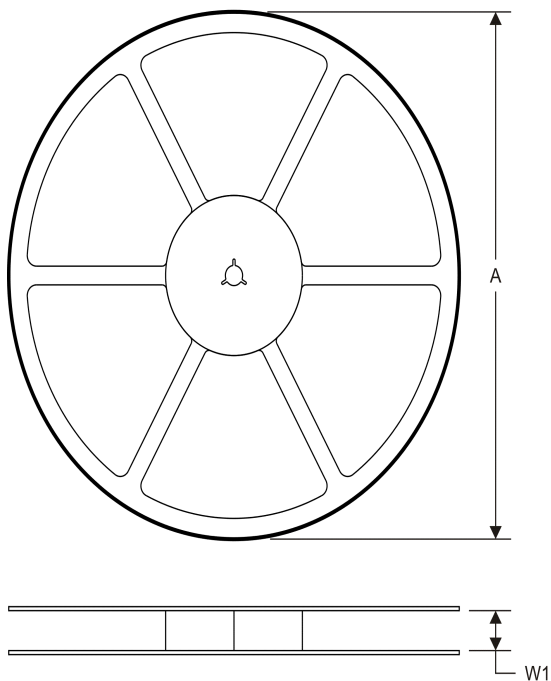
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVCP204RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
SN65LVCP204RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2



## TAPE AND REEL BOX DIMENSIONS

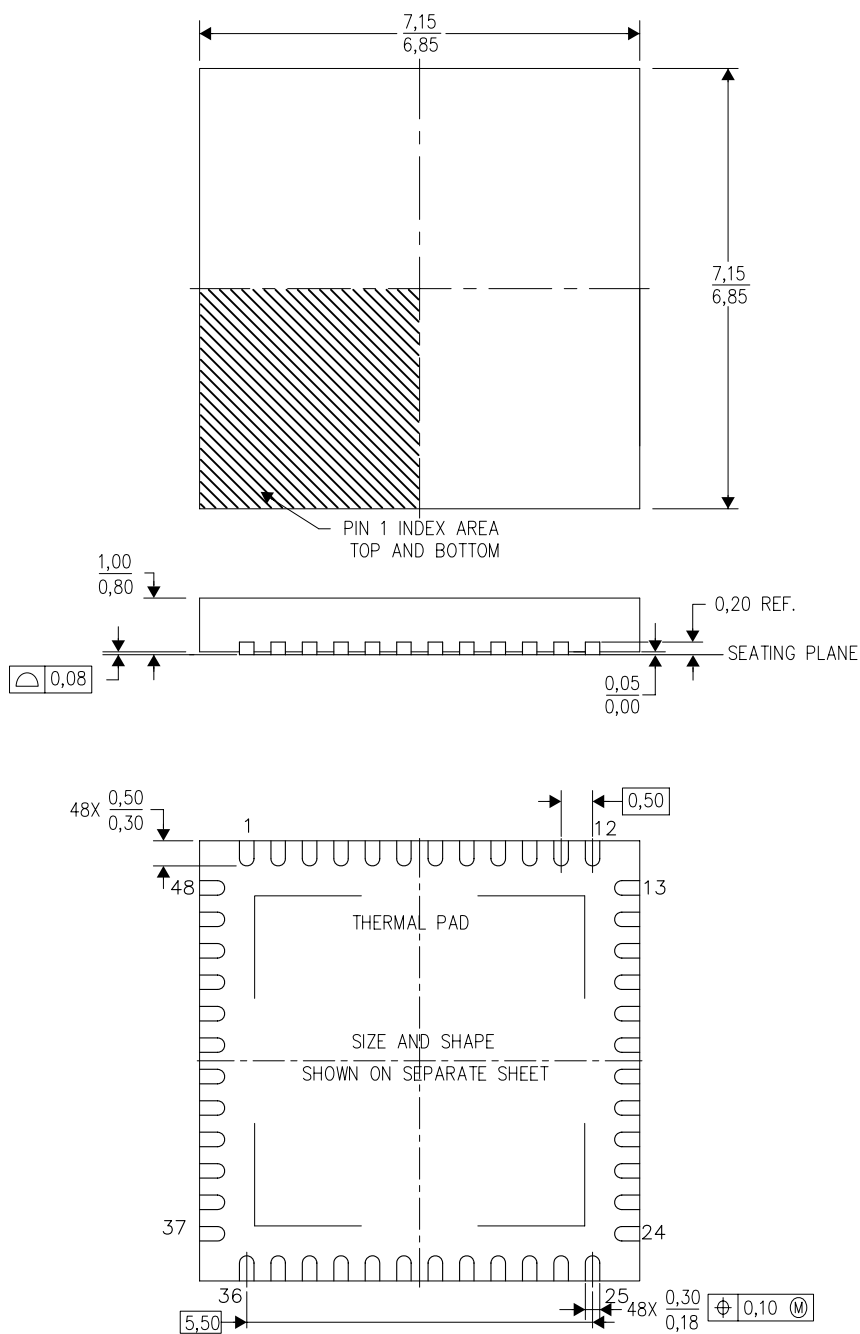


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVCP204RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
SN65LVCP204RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



4204101/F 06/11

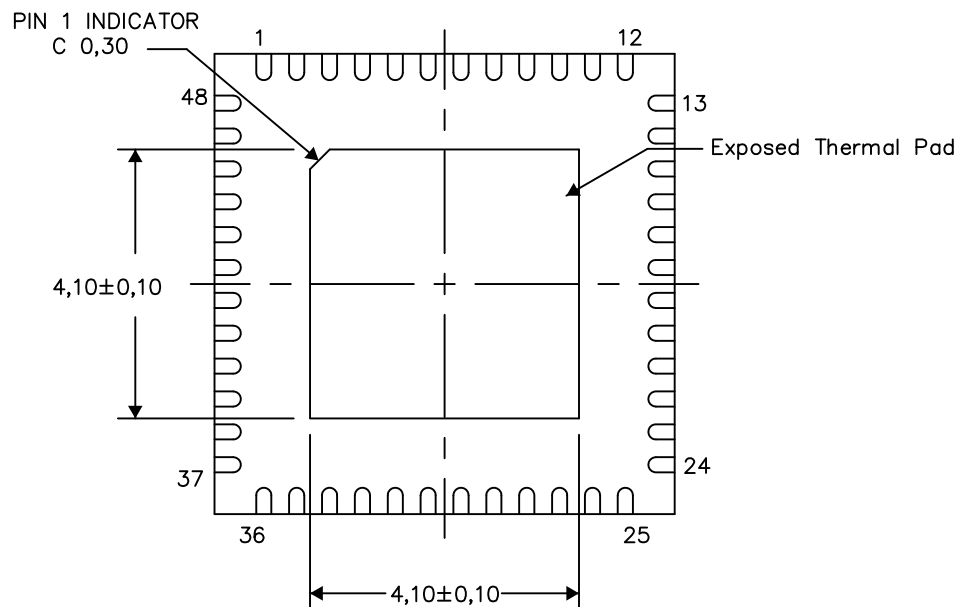
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-220.

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

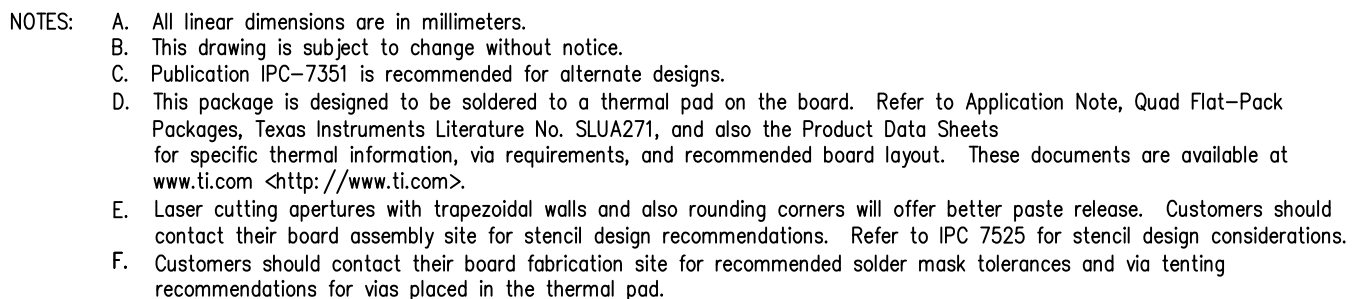


Bottom View

Exposed Thermal Pad Dimensions

4206354-3/T 03/13

NOTE: All linear dimensions are in millimeters



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