

PROGRAMMABLE 27-BIT PARALLEL-TO-SERIAL TRANSMITTER

FEATURES

- FlatLink™ 3G Serial-Interface Technology
- Compatible With FlatLink™3G Receivers Such as SN65LVDS308
- Input Supports Video Interfaces up to 24-Bit RGB Data and 3 Control Bits Received Over Two Differential Data Lines
- SubLVDS Differential Voltage Levels
- Up to 810-Mbps Data Throughput
- Three Operating Modes to Conserve Power
 - Active-Mode QVGA, 60 fps, 17.4 mW (typ)
 - Active-Mode VGA, 60 fps, 28.8 mW (typ)
 - Shutdown Mode $\approx 0.9 \mu\text{W}$ (typ)
 - Standby Mode $\approx 0.9 \mu\text{W}$ (typ)
- 1.8-V Supply Voltage
- ESD Rating > 3 kV (HBM)
- Pixel Clock Range of 4 MHz–30 MHz
- Failsafe on All CMOS Inputs
- 4-mm \times 4-mm MicroStar Junior™ $\mu\text{BGA}^{\text{®}}$ Package With 0.5-mm Ball Pitch
- Very Low EMI

APPLICATIONS

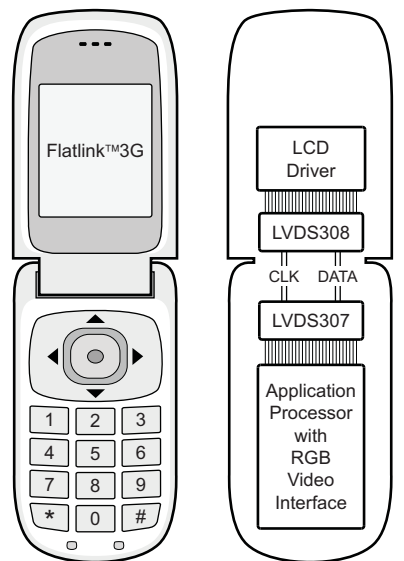
- Host-Controller to Display-Module Interface
- Mobile Phones and Smart Phones
- Portable Multimedia Players

DESCRIPTION

The SN65LVDS307 serializer device converts 27 parallel data inputs to one or two sub-low-voltage differential signaling (SubLVDS) serial outputs. It loads a shift register with 24 pixel bits and 3 control bits from the parallel CMOS input interface. In addition to the 27 data bits, the device adds a parity bit and two reserved bits into a 30-bit data word. Each word is latched into the device by the pixel clock (PCLK). The parity bit (odd parity) allows a receiver to detect single bit errors. The serial shift register is uploaded at 30 or 15 times the pixel-clock data rate, depending on the number of serial links used. A copy of the pixel clock is output on a separate differential output.

FPC cabling typically interconnects the SN65LVDS307 with the display. Compared to parallel signaling, the SN65LVDS307 outputs significantly reduce the EMI of the interconnect by over 20 dB.

The SN65LVDS307 supports three power modes (shutdown, standby, and active) to conserve power. When transmitting, the PLL locks to the incoming pixel clock, PCLK, and generates an internal high-speed clock at the line rate of the data lines. The parallel data are latched on the rising or falling edge of PCLK, as selected by the external control signal CPOL. The serialized data is presented on the serial outputs D0 and D1, together with a recreated PCLK that is generated from the internal high-speed clock and output on CLK. If PCLK stops, the device enters a standby mode to conserve power.



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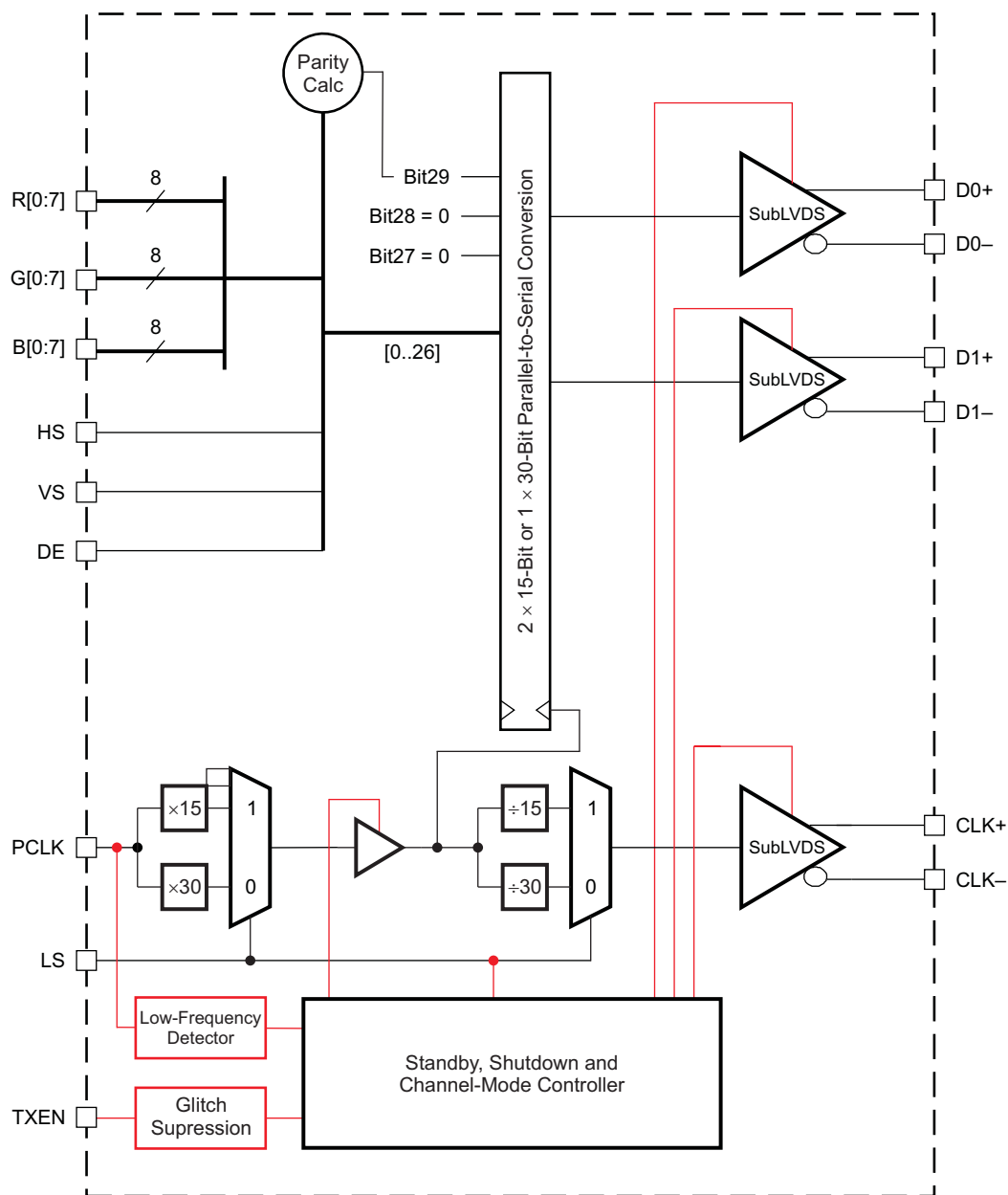
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The link select line, LS, controls whether one or two serial links are used. The TXEN input may be used to put the SN65LVDS307 in a shutdown mode. The SN65LVDS307 enters an active standby mode if the input clock, PCLK, stops. This minimizes power consumption without the need for controlling an external terminal. The SN65LVDS307 is characterized for operation over ambient air temperatures of -40°C to 85°C . All CMOS inputs offer failsafe to protect the input from damage during power up and to avoid current flow into the device inputs during power up. An input voltage of up to 2.165 V can be applied to all CMOS inputs while VDD is between 0 V and 1.65 V.

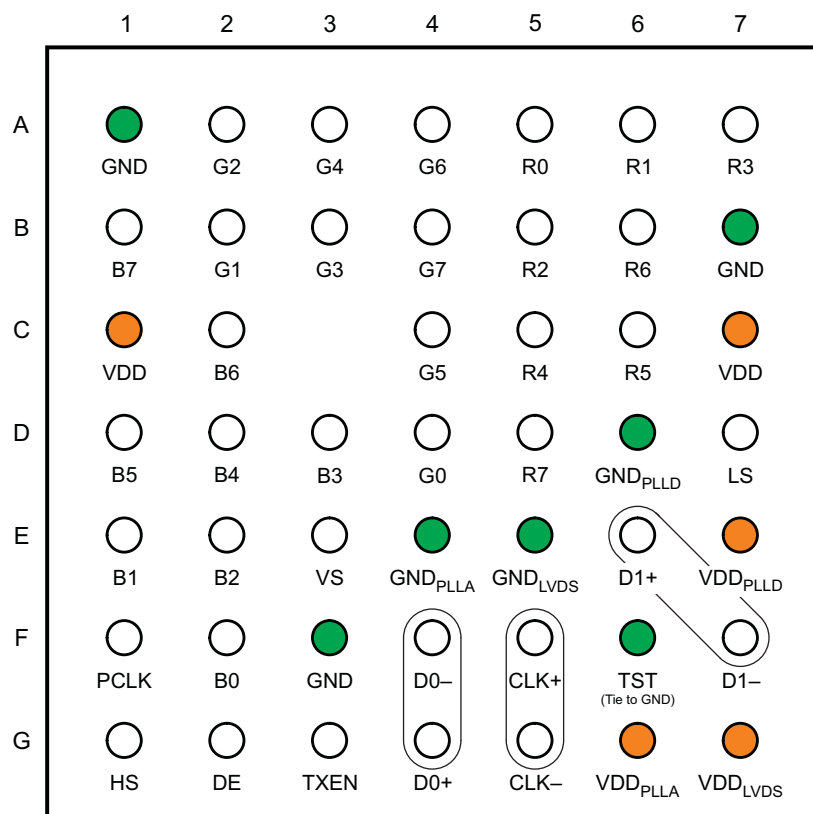


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Figure 1. Functional Block Diagram

PINOUT – TOP VIEW

ZQC PACKAGE (TOP VIEW)



P0063-01

Table 1. Numeric Terminal List

TERMINAL	SIGNAL	TERMINAL	SIGNAL	TERMINAL	SIGNAL	TERMINAL	SIGNAL
A1	GND	B7	GND	D6	GND _{PLLD}	F5	CLKP
A2	G2	C1	VDD	D7	LS	F6	TST
A3	G4	C2	B6	E1	B1	F7	D1–
A4	G6	C3	–	E2	B2	G1	HS
A5	R0	C4	G5	E3	VS	G2	DE
A6	R1	C5	R4	E4	GND _{PLLA}	G3	TXEN
A7	R3	C6	R5	E5	GND _{LVDS}	G4	D0+
B1	B7	C7	VDD	E6	D1+	G5	CLKN
B2	G1	D1	B5	E7	VDD _{PLLD}	G6	VDD _{PLLA}
B3	G3	D2	B4	F1	PCLK	G7	VDD _{LVDS}
B4	G7	D3	B3	F2	B0		
B5	R2	D4	G0	F3	GND		
B6	R6	D5	R7	F4	D0–		

Table 2. Terminal Functions

NAME	I/O	DESCRIPTION
D0+, D0–	SubLVDS out	SubLVDS data link (active during normal operation)
D1+, D1–		SubLVDS data link (active during normal operation when LS = high; high impedance if LS = low)
CLK+, CLK–		SubLVDS input pixel clock; clock polarity is fixed.
R0–R7	CMOS in	Red pixel data (8)
G0–G7		Green pixel data (8)
B0–B7		Blue pixel data (8)
HS		Horizontal sync
VS		Vertical sync
DE		Data enable
PCLK		Input pixel clock (rising clock polarity)
LS		Link select (determines active SubLVDS data links and PLL range); see Table 3 .
TXEN		Disables the CMOS drivers and turns off the PLL, putting device in shutdown mode 1 – Transmitter enabled 0 – Transmitter disabled (shutdown) Note: The TXEN input incorporates glitch-suppression logic to avoid device malfunction on short input spikes. It is necessary to pull TXEN high for longer than 10 μ s to enable the transmitter. It is necessary to pull the TXEN input low for longer than 10 μ s to disable the transmitter. At power up, the transmitter is enabled immediately if TXEN = 1 and disabled if TXEN = 0.
TST		Test (TI internal use only); tie this pin permanently to GND.
VDD	Power supply ⁽¹⁾	Supply voltage
GND		Supply ground
VDD _{LVDS}		SubLVDS I/O supply voltage
GND _{LVDS}		SubLVDS ground
VDD _{PLLA}		PLL analog supply voltage
GND _{PLLA}		PLL analog GND
VDD _{PLLD}		PLL digital supply voltage
GND _{PLLD}		PLL digital GND

(1) For a multilayer PCB, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

FUNCTIONAL DESCRIPTION

SERIALIZATION MODES

The SN65LVDS307 transmitter has two modes of operation controlled by link-select terminal LS. Table 3 shows the serializer modes of operation.

Table 3. Logic Table: Link Select Operating Modes

LS	Mode of Operation	Data-Link Status
0	1-channel mode, 1ChM (30-bit serialization rate)	D0 active; D1 high-impedance
1	2-channel mode, 2ChM (15-bit serialization rate)	D0, D1 active

1-CHANNEL MODE

While LS is held low, the SN65LVDS307 transmits payload data over a single SubLVDS data pair, D0. The PLL locks to PCLK and internally multiplies the clock by a factor of 30. The internal high-speed clock is used to serialize (shift out) the data payload on D0. Two reserved bits and the parity bit are added to the data frame. Figure 2 illustrates the timing and the mapping of the data payload into the 30-bit frame. The internal high-speed clock is divided by a factor of 30 to recreate the pixel clock, and presented on the SubLVDS CLK output. While in this mode, the PLL can lock to a clock that is in the range of 4 MHz through 15 MHz. This mode is intended for smaller video display formats (e.g. QVGA to HVGA) that do not require the full bandwidth capabilities of the SN65LVDS307.

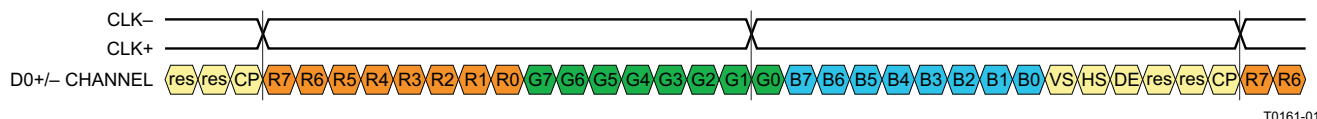


Figure 2. Data and Clock Output in 1-Channel Mode (LS = Low).

2-CHANNEL MODE

While LS is held high, the SN65LVDS307 transmits payload data over two SubLVDS data pairs, D0 and D1. The PLL locks to PCLK and internally multiplies it by a factor of 15. The internal high-speed clock is used to serialize the data payload on D0 and D1. Two reserved bits and the parity bit are added to the data frame. Figure 3 illustrates the timing and the mapping of the data payload into the 30-bit frame and how the frame becomes split into the two output channels. The internal high-speed clock is divided by 15 to recreate the pixel clock and presented on SubLVDS CLK. The PLL can lock to a clock that is in the range of 8 MHz through 30 MHz in this mode. Typical applications for using the 2-channel mode are HVGA and VGA displays.

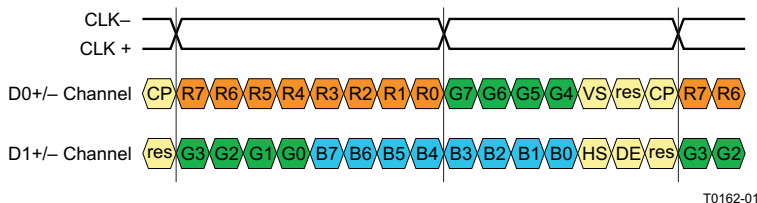


Figure 3. Data and Clock Output in 2-Channel Mode (LS = High).

POWER-DOWN MODES

The SN65LVDS307 transmitter has two power-down modes to facilitate efficient power management.

Shutdown Mode

The SN65LVDS307 enters shutdown mode when the TXEN terminal is asserted low. This turns off all transmitter circuitry, including the CMOS input, PLL, serializer, and SubLVDS transmitter output stage. All outputs are high-impedance. Current consumption in shutdown mode is nearly zero.

Standby Mode

The SN65LVDS307 enters the standby mode if TXEN is high and the PCLK input signal frequency is less than 500 kHz. All circuitry except the PCLK input monitor is shut down, and all outputs enter the high-impedance state. The current consumption in standby mode is very low. When the PCLK input signal is completely stopped, the I_{DD} current consumption is less than 10 μ A. The PCLK input must not be left floating.

NOTE:

A floating (left open) CMOS input allows leakage currents to flow from VDD to GND. To prevent large leakage current, a CMOS gate must be kept at a valid logic level, either V_{IH} or V_{IL} . This can be achieved by applying an external voltage of V_{IH} or V_{IL} to all SN65LVDS307 inputs.

ACTIVE MODES

When TXEN is high and the PCLK input clock signal is faster than 3 MHz, the SN65LVDS307 enters the active mode. Current consumption in the active mode depends on operating frequency and the number of data transitions in the data payload.

Acquire Mode (PLL Approaches Lock)

The PLL is enabled and attempts to lock to the input clock. All outputs remain in the high-impedance state. When the PLL monitor detects stable PLL operation, the device switches from the acquire mode to the transmit mode. For proper device operation, the pixel clock frequency must fall within the valid f_{PCLK} range specified under recommended operating conditions. If the pixel clock frequency is higher than 3 MHz but lower than $f_{PCLK}(\text{min})$, the SN65LVDS307 PLL is enabled. Under such conditions, it is possible for the PLL to lock temporarily to the pixel clock, causing the PLL monitor to release the device into transmit mode. If this happens, the PLL may or may not be properly locked to the pixel clock input, potentially causing data errors, frequency oscillation, and PLL deadlock (loss of VCO oscillation).

Transmit Mode

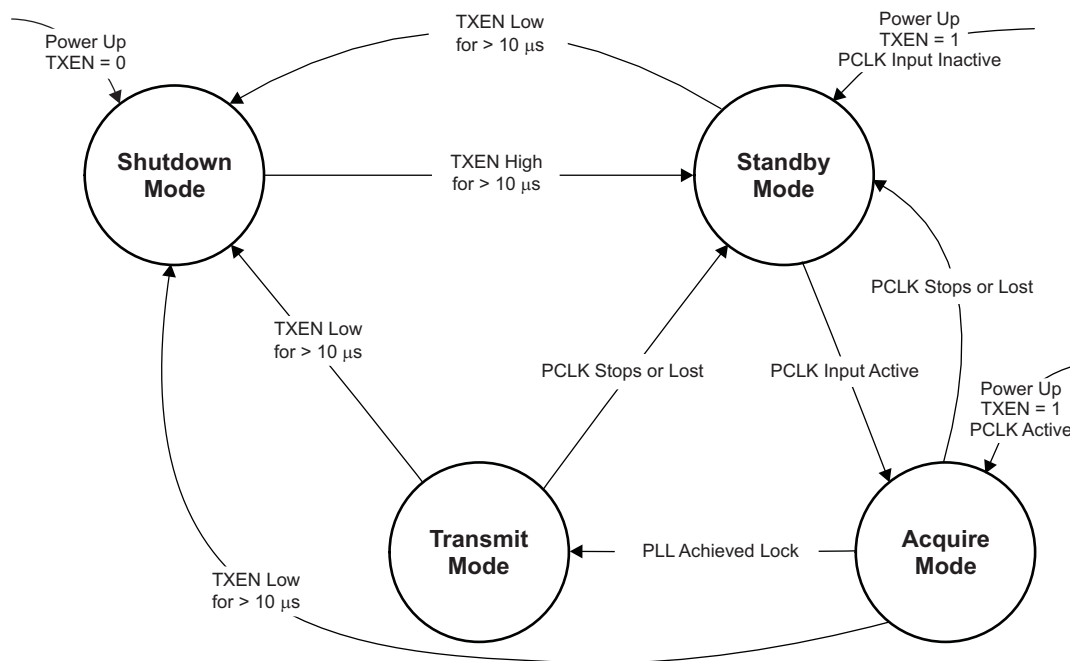
After the PLL achieves lock, the device enters the normal transmit mode. The CLK terminal outputs a copy of PCLK. Based on the selected mode of operation, the D0 and D1 outputs carry the serialized data. In 1-channel mode, the D1 outputs remain in the high-impedance state.

PARITY BIT GENERATION

The SN65LVDS307 transmitter calculates the parity of the transmit data word and sets the parity bit accordingly. The parity bit covers the 27-bit data payload consisting of 24 bits of pixel data plus VS, HS and DE. The two reserved bits are not included in the parity generation. Odd-parity bit signaling is used. The transmitter sets the parity bit if the sum of the 27 data bits results in an even number of ones. The parity bit is cleared otherwise. This allows the receiver to verify parity and detect single bit errors.

STATUS DETECT AND OPERATING MODES FLOW DIAGRAM

The SN65LVDS307 switches between the power saving and active modes in the following way:



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Figure 4. Status Detect and Operating Modes Flow Diagram

Table 4. Status Detect and Operating Modes Descriptions

Mode	Characteristics	Conditions
Shutdown mode	Least amount of power consumption (most circuitry turned off); all outputs are high-impedance.	TXEN is low for longer than 10 μ s. ⁽¹⁾⁽²⁾
Standby mode	Low power consumption (only clock activity circuit active; PLL is disabled to conserve power); all outputs are high-impedance.	TXEN is high for longer than 10 μ s; PCLK input signal is missing or inactive. ⁽²⁾
Acquire mode	PLL tries to achieve lock; all outputs are high-impedance.	TXEN is high; PCLK input monitor detected input activity.
Transmit mode	Data transfer (normal operation); transmitter serializes data and transmits data on serial output; unused outputs remain high-impedance.	TXEN is high and PLL is locked to incoming clock.

(1) In shutdown mode, all SN65LVDS307 internal switching circuits (e.g., PLL, serializer, etc.) are turned off to minimize power consumption. The input stage of any input terminal remains active.

(2) Leaving inputs unconnected can cause random noise to toggle the input stage and potentially harm the device. All CMOS inputs must be tied to a valid logic level, V_{IL} or V_{IH} , during shutdown or standby mode.

Table 5. Operating Mode Transitions

MODE TRANSITION	USE CASE	TRANSITION SPECIFICS
Shutdown → standby	Drive TXEN high to enable transmitter	<ol style="list-style-type: none"> 1. TXEN high > 10 μs 2. Transmitter enters standby mode. <ol style="list-style-type: none"> a. All outputs are high-impedance. b. Transmitter turns on clock input monitor.
Standby → acquire	Transmitter activity detected	<ol style="list-style-type: none"> 1. PCLK input monitor detects clock input activity. 2. Outputs remain high-impedance. 3. PLL circuit is enabled.
Acquire → transmit	Link is ready to transfer data	<ol style="list-style-type: none"> 1. PLL is active and approaches lock. 2. PLL achieved lock within t_{wakeup}. 3. Parallel data input latches into shift register. 4. CLK output turns on. 5. Selected data outputs turn on and send out first serial data bit.
Transmit → standby	Request transmitter to enter standby mode by stopping PCLK	<ol style="list-style-type: none"> 1. PCLK input monitor detects missing PCLK. 2. Transmitter indicates standby, putting all outputs into high-impedance. 3. PLL shuts down. 4. PCLK activity input monitor remains active.
Transmit/standby → shutdown	Turn off transmitter	<ol style="list-style-type: none"> 1. TXEN pulled low for longer than t_{pwrdn}. 2. Transmitter indicates standby, putting output CLK+ and CLK– into high-impedance state. 3. Transmitter puts all other outputs into high-impedance state. 4. Most IC circuitry is shut down for least power consumption.

ORDERING INFORMATION

PART NUMBER	Package	SHIPPING METHOD
SN65LVDS307ZQCR	ZQC	Reel

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply voltage range, VDD ⁽²⁾ , VDD _{PLLA} , VDD _{PLLD} , VDD _{LVDS}		−0.3 to 2.175	V
Voltage range at any input or output terminal	When VDD _x > 0 V	−0.5 to 2.175	V
	When VDD _x ≤ 0 V	−0.5 to VDD + 2.175	V
Electrostatic discharge	Human-body model ⁽³⁾ (all terminals)	±3	kV
	Charged-device model ⁽⁴⁾ (all terminals)	±500	V
	Machine model ⁽⁵⁾ (all terminals)	±200	
Continuous power dissipation		See <i>Dissipation Ratings</i> table	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the GND terminals.

(3) In accordance with JEDEC Standard 22, Test Method A114-A.

(4) In accordance with JEDEC Standard 22, Test Method C101.

(5) In accordance with JEDEC Standard 22, Test Method A115-A.

DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	$T_A < 25^\circ\text{C}$	DERATING FACTOR ⁽¹⁾ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
ZQC	Low-K ⁽²⁾	496 mW	6.21 mW/°C	124 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

(2) In accordance with the low-K thermal metric definitions of EIA/JESD51-2.

THERMAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS		VALUE	UNIT
P_D Device power dissipation	Typical	$V_{DD_X} = 1.8\text{ V}$, $T_A = 25^\circ\text{C}$, 2-channel mode	PCLK at 4 MHz	14.4	mW
			PCLK at 30 MHz	38.2	
	Maximum	$V_{DD_X} = 1.95\text{ V}$, $T_A = -40^\circ\text{C}$	PCLK at 4 MHz	22.3	mW
			PCLK = 30 MHz	50.2	

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			MIN	NOM	MAX	UNIT
VDD VDD _{PLLA} VDD _{PLLD} VDD _{LVDS}	Supply voltages		1.65	1.8	1.95	V
VDD _{n(PP)}	Supply voltage noise magnitude 50 MHz (all supplies)	Test setup see Figure 10 f(noise) = 1Hz to 2 GHz			100	mV
f _{PCLK}	Pixel clock frequency	1-channel transmit mode, see Figure 2	4		15	MHz
		2-channel transmit mode, see Figure 3	8		30	
		Frequency threshold, standby mode to active mode ⁽²⁾ , see Figure 14	0.5		3	
t _H × f _{PCLK}	PCLK input duty cycle		0.33		0.67	
T _A	Operating free-air temperature		−40		85	°C
t _{jit(per)PCLK}	PCLK RMS period jitter ⁽³⁾	Measured on PCLK input			5	ps-rms
t _{jit(TJ)PCLK}	PCLK total jitter				0.05/f _{PCLK}	s
t _{jit(CC)PCLK}	PCLK peak cycle-to-cycle jitter ⁽⁴⁾				0.02/f _{PCLK}	s
PCLK, R[0:7], G[0:7], B[0:7], VS, HS, DE, PCLK, LS, TXEN						
V _{IH}	High-level input voltage		0.7 VDD		VDD	V
V _{IL}	Low-level input voltage				0.3 VDD	V
t _{DS}	Data setup time prior to PCLK transition	f(PCLK) = 30 MHz; see Figure 6	2			ns
t _{DH}	Data hold time after PCLK transition		2			ns

(1) Unused single-ended inputs must be held high or low to prevent them from floating.

(2) PCLK input frequencies lower than 500 kHz force the SN65LVDS307 into standby mode. Input frequencies between 500 kHz and 3 MHz may or may not activate the SN65LVDS307. Input frequencies beyond 3 MHz activate the SN65LVDS307.

(3) Period jitter is the deviation in cycle time of a signal with respect to the ideal period over a random sample of 100,000 cycles.

(4) Cycle-to-cycle jitter is the variation in cycle time of a signal between adjacent cycles over a random sample of 1,000 adjacent cycle pairs.

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP ⁽¹⁾	MAX	UNIT
I _{DD}	1ChM	VDD = VDD _{PLLA} = VDD _{PLLD} = VDD _{LVDS} , R _{L(PCLK)} = R _{L(Dx)} = 100 Ω, V _{IH} = VDD, V _{IL} = 0 V, TXEN at VDD, alternating 1010 serial bit pattern	f _{PCLK} = 4 MHz		9	11.4	mA
			f _{PCLK} = 6 MHz		10.6	12.6	
			f _{PCLK} = 15 MHz		16	18.8	
		VDD = VDD _{PLLA} = VDD _{PLLD} = VDD _{LVDS} , R _{L(PCLK)} = R _{L(Dx)} = 100 Ω, V _{IH} = VDD, V _{IL} = 0 V, TXEN at VDD, typical power test pattern (see Table 7)	f _{PCLK} = 4 MHz		8		mA
			f _{PCLK} = 6 MHz		8.9		
			f _{PCLK} = 15 MHz		14		
	2ChM	VDD = VDD _{PLLA} = VDD _{PLLD} = VDD _{LVDS} , R _{L(PCLK)} = R _{L(Dx)} = 100 Ω, V _{IH} = VDD, V _{IL} = 0 V, TXEN at VDD, alternating 1010 serial bit pattern	f _{PCLK} = 8 MHz		13.7	15.9	mA
			f _{PCLK} = 22 MHz		18.4	22	
			f _{PCLK} = 30 MHz		21.4	25.8	
		VDD = VDD _{PLLA} = VDD _{PLLD} = VDD _{LVDS} , R _{L(PCLK)} = R _{L(Dx)} = 100 Ω, V _{IH} = VDD, V _{IL} = 0 V, TXEN at VDD, typical power test pattern (see Table 8)	f _{PCLK} = 8 MHz		11.5		mA
			f _{PCLK} = 22 MHz		16		
			f _{PCLK} = 30 MHz		19.1		
	Standby mode		VDD = VDD _{PLLA} = VDD _{PLLD} = VDD _{LVDS} , R _{L(PCLK)} = R _{L(Dx)} = 100 Ω, V _{IH} = VDD, V _{IL} = 0 V, all inputs held static high or static low		0.61	10	μA
	Shutdown mode				0.55	10	μA

(1) All typical values are at 25°C and with 1.8-V supply unless otherwise noted.

OUTPUT ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
SubLVDS Output (D0+, D0–, D1+, D1–, CLK+, and CLK–)					
V _{OC(SS)M}	Steady-state common-mode output voltage	Output load see Figure 8	0.8	0.9	1 V
V _{OCM(SS)}	Change in steady-state common-mode output voltage		–10		10 mV
V _{OCM(PP)}	Peak-to-peak common mode output voltage			75	mV
V _{Od}	Differential output voltage magnitude V _{Dx+} – V _{Dx–} , V _{CLK+} – V _{CLK–}		100	150	200 mV
$\Delta V_{Od} $	Change in differential output voltage between logic states		–10		10 mV
Z _{OD(CLK)}	Differential small-signal output impedance	TXEN at VDD		210	Ω
I _{OSD}	Differential short-circuit output current	V _{OD} = 0 V, f _{PCLK} = 28 MHz			10 mA
I _{OS}	Short circuit output current ⁽²⁾	V _O = 0 V or VDD		5	mA
I _{OZ}	High-impedance state output current	V _O = 0 V or VDD(max), TXEN at GND	–3		3 μ A

(1) All typical values are at 25°C and with 1.8-V supply, unless otherwise noted.

(2) All SN65LVDS307 outputs tolerate shorts to GND or VDD without device damage.

INPUT ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
R[0:7], G[0:7], B[0:7], VS, HS, DE, PCLK, LS, TXEN					
I _{IH}	High-level input current	V _{IN} = 0.7 \times VDD	–200		200 nA
I _{IL}	Low-level input current	V _{IN} = 0.3 \times VDD	–200		200 nA
C _{IN}	Input capacitance			1.5	pF

(1) All typical values are at 25°C and with 1.8-V supply, unless otherwise noted.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
t _r	20%-to-80% differential output signal rise time	See Figure 7 and Figure 8		250		500	ps
t _f	20%-to-80% differential output signal fall time	See Figure 7 and Figure 8		250		500	
f _{BW}	PLL bandwidth (3-dB cutoff frequency)	Tested from PCLK input to CLK output, See Figure 5 ⁽²⁾	f _{PCLK} = 22 MHz			0.082 f _{PCLK}	MHz
			f _{PCLK} = 30 MHz			0.078 f _{PCLK}	
t _{pd(L)}	Propagation delay time, input to serial output (data latency Figure 9)	TXEN at VDD, V _{IH} = VDD, V _{IL} = GND, R _L = 100 Ω	1-channel mode	0.8/f _{PCLK}	1/f _{PCLK}	1.2/f _{PCLK}	s
			2-channel mode	1/f _{PCLK}	1.21/f _{PCLK}	1.5/f _{PCLK}	
t _H × f _{CLK0}	Output CLK duty cycle		1-channel mode	0.45	0.50	0.55	
			2-channel mode	0.49	0.53	0.58	
t _{GS}	TXEN glitch suppression pulse duration ⁽³⁾	V _{IH} = VDD, V _{IL} = GND, TXEN toggles between V _{IL} and V _{IH} , see Figure 12 and Figure 13.		3.8		10	μs
t _{pwrup}	Enable time from power down (↑TXEN)	Time from TXEN pulled high to CLK and Dx outputs enabled and transmit valid data; see Figure 13			0.24	2	ms
t _{pwrdn}	Disable time from active mode (↓TXEN)	TXEN is pulled low during transmit mode; time measurement until output is disabled and PLL is shut down; see Figure 13			0.5	11	μs
t _{wakup}	Enable time from standby (↑PCLK)	TXEN at VDD; device in standby; time measurement from PCLK starts switching to CLK and Dx outputs enabled and transmit valid data; see Figure 13			0.23	2	ms
t _{sleep}	Disable time from active mode (PCLK stopping)	TXEN at VDD; device is transmitting; time measurement from PCLK input signal halt until CLK + Dx outputs are disabled and PLL is disabled; see Figure 13			0.4	100	μs

(1) All typical values are at 25°C and with 1.8-V supply unless otherwise noted.

(2) The maximum limit is based on statistical analysis of the device performance over process, voltage, and temperature ranges. This parameter is functionality tested only on automatic test equipment (ATE).

(3) The TXEN input incorporates glitch-suppression circuitry to disregard short input pulses. t_{GS} is the duration of either a high-to-low or low-to-high transition that is suppressed.

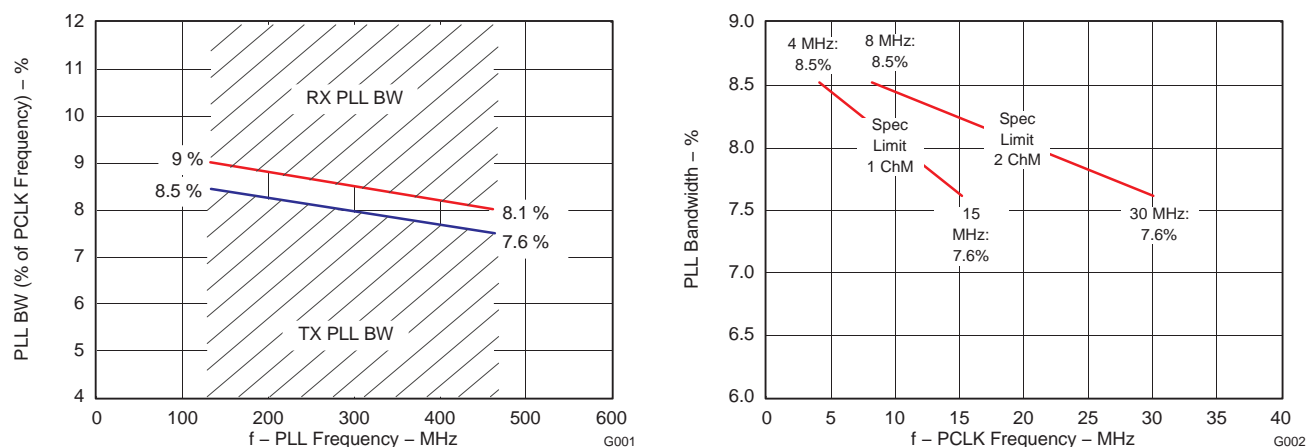


Figure 5. SN65LVDS307 PLL Bandwidth (Also Showing the SN65LVDS308 PLL Bandwidth)

TIMING CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PPOSX} Output pulse position, ↑serial data to ↑CLK; see (1)(2) and Figure 11	1ChM: x = 0..29, f _{PCLK} = 15 MHz; TXEN at VDD, V _{IH} = VDD, V _{IL} = GND, R _L = 100 Ω, test pattern as in Table 11 ⁽³⁾	$\frac{x}{30 \cdot f_{PCLK}} - 330 \text{ ps}$		$\frac{x}{30 \cdot f_{PCLK}} + 330 \text{ ps}$	ps
	1ChM: x = 0..29, f _{PCLK} = 4 MHz to 15 MHz ⁽⁴⁾	$\frac{x - 0.1845}{30 \cdot f_{PCLK}}$		$\frac{x + 0.1845}{30 \cdot f_{PCLK}}$	
	2ChM: x = 0..14, f _{PCLK} = 30 MHz TXEN at VDD, V _{IH} = VDD, V _{IL} = GND, R _L = 100 Ω, test pattern as in Table 12 ⁽³⁾	$\frac{x}{15 \cdot f_{PCLK}} - 330 \text{ ps}$		$\frac{x}{15 \cdot f_{PCLK}} + 330 \text{ ps}$	
	2ChM: x = 0..14, f _{PCLK} = 8 MHz to 30 MHz ⁽⁴⁾	$\frac{x - 0.1845}{15 \cdot f_{PCLK}}$		$\frac{x + 0.1845}{15 \cdot f_{PCLK}}$	

- (1) This number also includes the high-frequency random and deterministic PLL clock jitter that is not traceable by the SN65LVDS308 receiver PLL; t_{PPOSx} represents the total timing uncertainty of the transmitter necessary to calculate the jitter budget when combined with the SN65LVDS308 receiver.
- (2) The pulse position min/max variation is given with a bit error rate target of 10⁻¹²; the measurement estimates the random jitter contribution to the total jitter by multiplying the random RMS jitter by a factor of 14; measurements of the total jitter are taken with > 10¹² samples.
- (3) The minimum and maximum limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges. This parameter is functionality tested only on automatic test equipment (ATE).
- (4) These minimum and maximum limits are simulated only.

PARAMETER MEASUREMENT INFORMATION

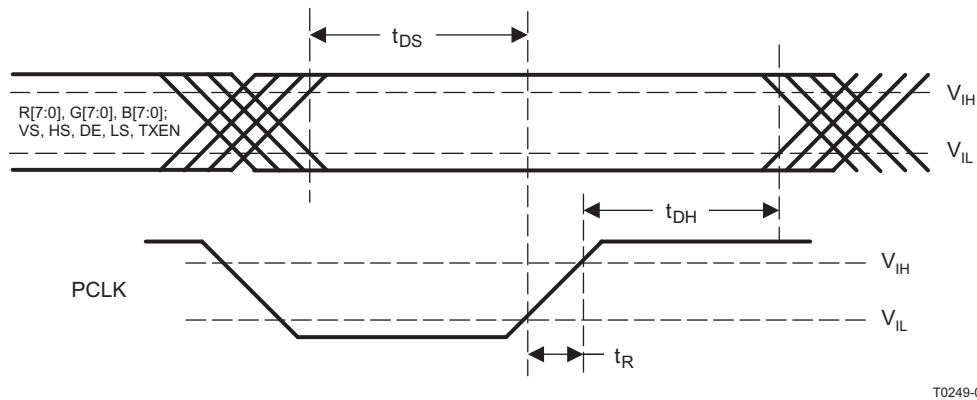


Figure 6. Setup/Hold Time

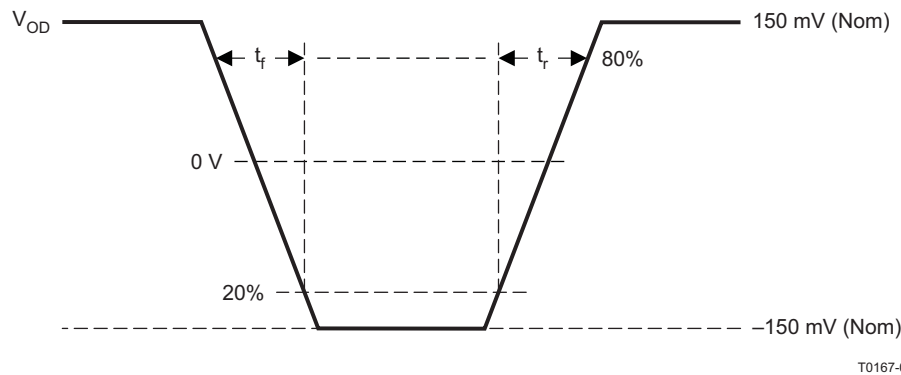
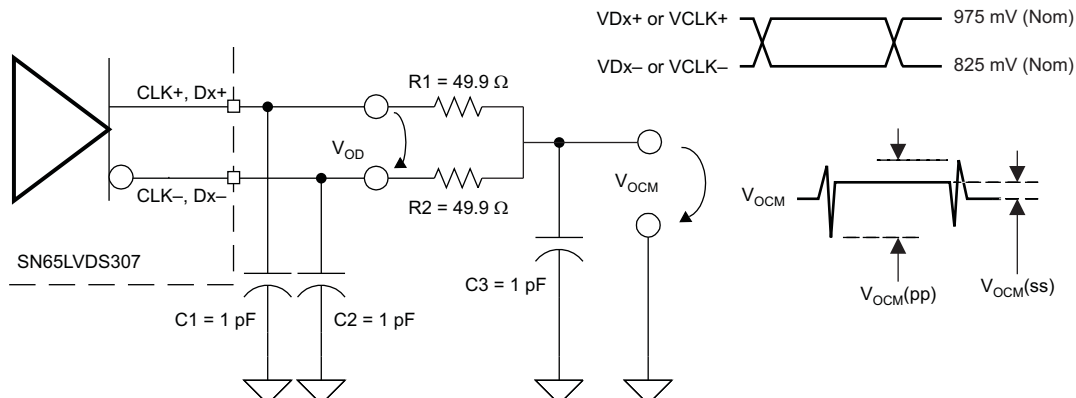


Figure 7. Rise and Fall Time Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

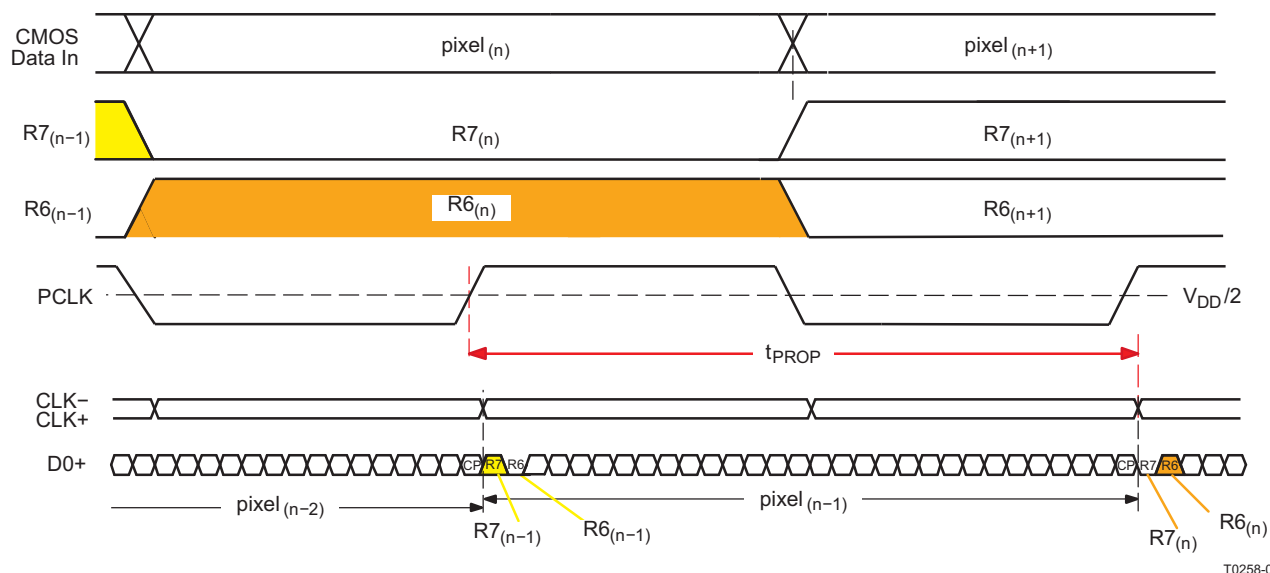


NOTES:

- 20-MHz output test pattern on all differential outputs (CLK, D0, and D1):
this is achieved by:
 - Device is set to 2-channel mode.
 - $f_{CLK} = 20 \text{ MHz}$
 - Inputs R[7:3] = B[7:3] connected to V_{DD} , all other data inputs set to GND.
- C1, C2, and C3 include instrumentation and fixture capacitance, tolerance $\pm 20\%$; C, R1, and R2 tolerance $\pm 1\%$
- The measurement of $V_{OCM(pp)}$ and $V_{OC(ss)}$ are taken with test equipment bandwidth $> 1 \text{ GHz}$.

S0263-01

Figure 8. Driver Output Voltage Test Circuit and Definitions



T0258-01

Figure 9. $t_{pd(L)}$ Propagation Delay Input to Output (LS = 0)

PARAMETER MEASUREMENT INFORMATION (continued)

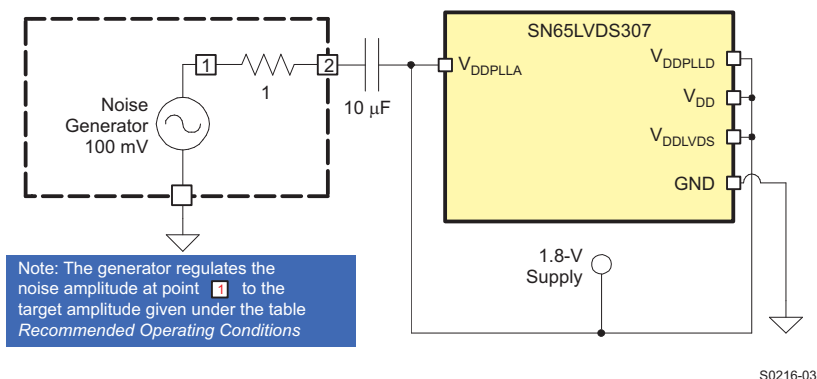


Figure 10. Power Supply Noise Test Setup

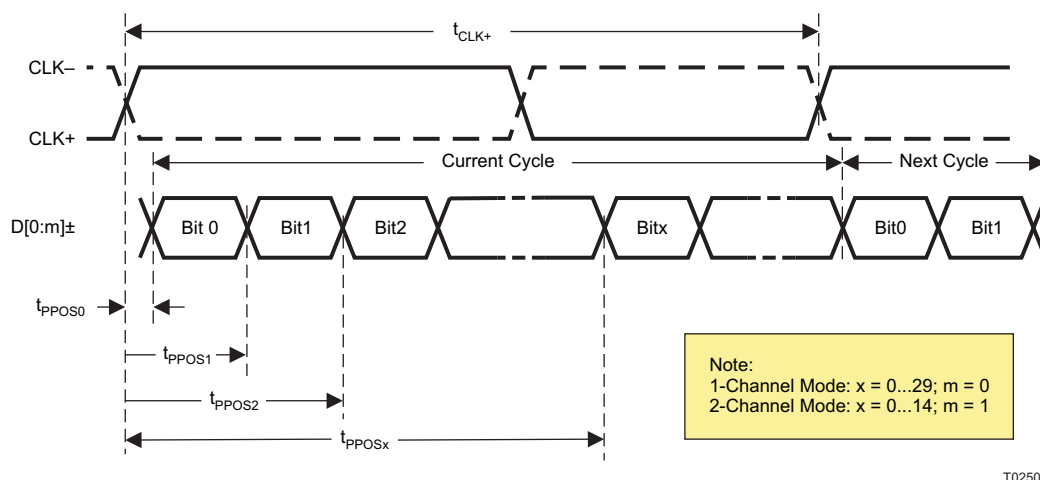


Figure 11. $t_{SK(0)}$ SubLVDS Output Pulse Position Measurement

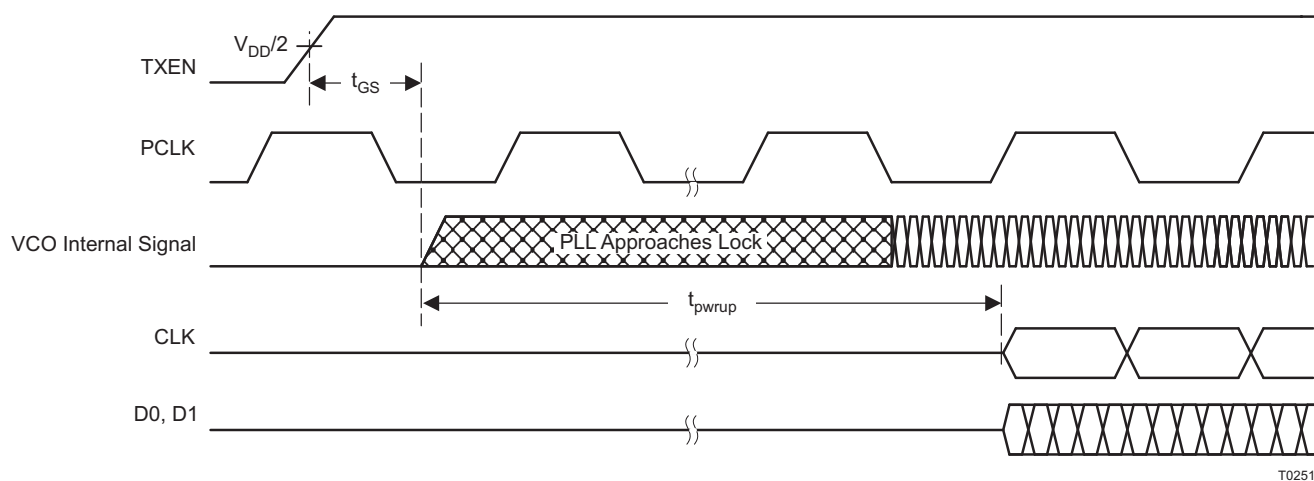
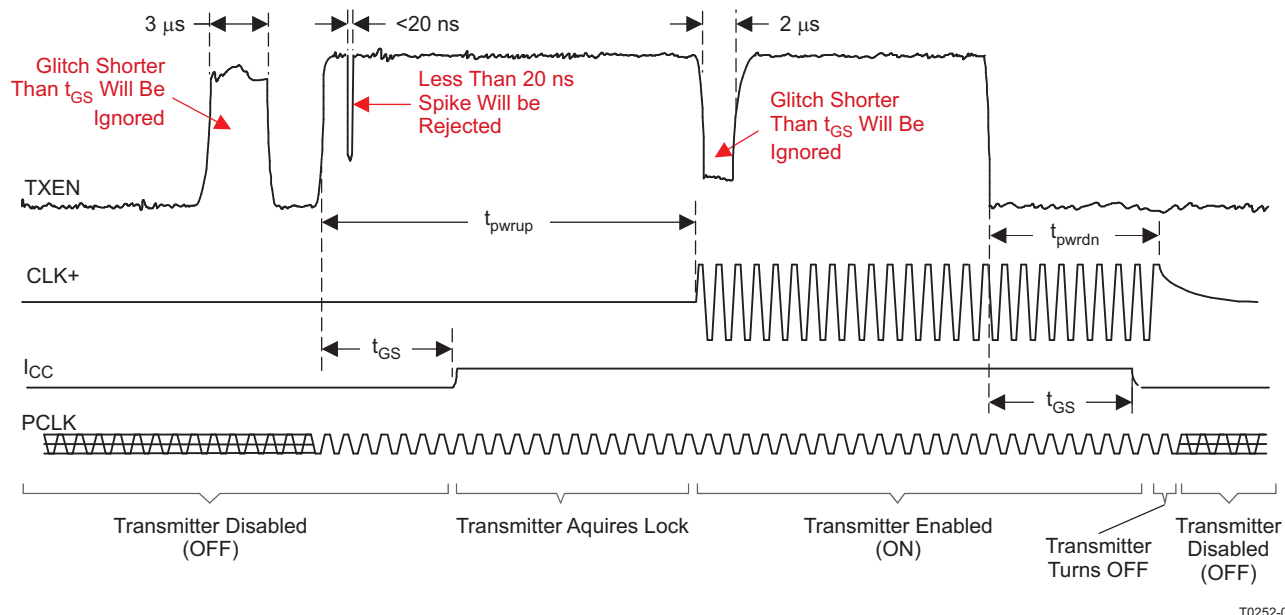


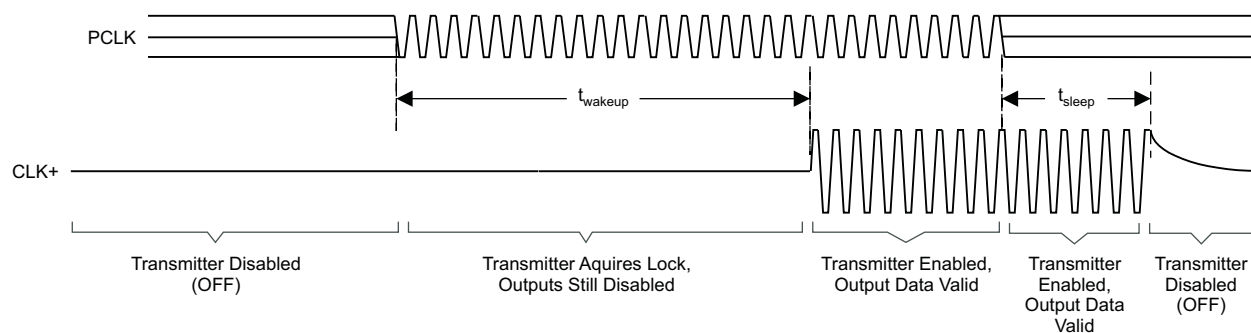
Figure 12. Transmitter Behavior While Approaching Sync

PARAMETER MEASUREMENT INFORMATION (continued)



T0252-01

Figure 13. Transmitter Enable Glitch Suppression Time



T0253-01

Figure 14. Standby Detection

Power Consumption Tests

Table 6 shows an example test pattern word.

Table 6. Example Test Pattern Word

Word	R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE
1	0x7C3E1E7

7				C				3				E				1				E				7			
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	0	VS	HS	DE
0	1	1	1	1	1	0	0	0	0	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1

Typical IC Power-Consumption Test Pattern

The typical power-consumption test pattern consists of 16 30-bit transmit words in 1-channel mode, eight 30-bit transmit words in 2-channel mode. The pattern repeats itself throughout the entire measurement. It is assumed that every possible transmit code on RGB inputs has the same probability to occur during typical device operation.

Table 7. Typical IC Power-Consumption Test Pattern, 1-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE
1	0x0000007
2	0xFFFF007
3	0x01FFF47
4	0xF0E07F7
5	0x7C3E1E7
6	0xE707C37
7	0xE1CE6C7
8	0xF1B9237
9	0x91BB347
10	0xD4CCC67
11	0xAD53377
12	0xACB2207
13	0xAAB2697
14	0x5556957
15	0xAAAAAB3
16	0xAAAAAA5

Table 8. Typical IC Power-Consumption Test Pattern, 2-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE
1	0x0000001
2	0x03F03F1
3	0xBFFBFF1
4	0x1D71D71
5	0x4C74C71
6	0xC45C451
7	0xA3AA3A5
8	0x5555553

Maximum Power Consumption Test Pattern

The maximum (or worst-case) power consumption of the SN65LVDS307 is tested using the two different test patterns shown in [Table 9](#). Test patterns consists of sixteen 30-bit transmit words in 1-channel mode, eight 30-bit transmit words in 2-channel mode. The pattern repeats itself throughout the entire measurement. It is assumed that every possible transmit code on RGB inputs has the same probability to occur during typical device operation.

Table 9. Worst-Case Power-Consumption Test Pattern 1

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE
1	0xAAAAAA5
2	0x5555555

**Table 10. Worst-Case Power-Consumption
Test Pattern 2**

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE
1	0x0000000
2	0xFFFFF7

Output Skew Pulse Position and Jitter Performance

The following test patterns are used to measure the output skew pulse position and the jitter performance of the SN65LVDS307. The jitter test patterns stress the interconnect for worst-case ISI. Each pattern is self-repeating for the duration of the test.

Table 11. Transmit Jitter Test Pattern, 1-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE
1	0x0000001
2	0x0000031
3	0x00000F1
4	0x00003F1
5	0x0000FF1
6	0x0003FF1
7	0x000FFF1
8	0x0F0F0F1
9	0x0C30C31
10	0x0842111
11	0x1C71C71
12	0x18C6311
13	0x1111111
14	0x3333331
15	0x2452413
16	0x22A2A25
17	0x5555553
18	0xDB6DB65
19	0xCCCCC1
20	0xEEEEE1
21	0xE739CE1
22	0xE38E381
23	0xF7BDEE1
24	0xF3CF3C1
25	0xF0F0F01
26	0xFFFF001
27	0xFFFFC01
28	0xFFFFF01
29	0xFFFFFC01
30	0xFFFFF01
31	0xFFFFFC1
32	0xFFFFF1

Table 12. Transmit Jitter Test Pattern, 2-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE
1	0x0000001
2	0x000FFF3
3	0x8008001
4	0x0030037
5	0xE00E001
6	0x00FF001
7	0x007E001
8	0x003C001
9	0x0018001
10	0x1C7E381
11	0x3333331
12	0x555AAA5
13	0x6DBDB61
14	0x7777771
15	0x555AAA3
16	0xAAAAAA5
17	0x5555553
18	0xAAA5555
19	0x8888881
20	0x9242491
21	0xAAA5571
22	0xCCCCC1
23	0xE3E1C71
24	0xFFE7FF1
25	0xFFC3FF1
26	0xFF81FF1
27	0xFE00FF1
28	0x1FF1FF1
29	0xFFCFFC3
30	0x7FF7FF1
31	0xFFF0007
32	0xFFFFF1

TYPICAL CHARACTERISTICS

**POWERDOWN, STANDBY SUPPLY CURRENT
vs TEMPERATURE**

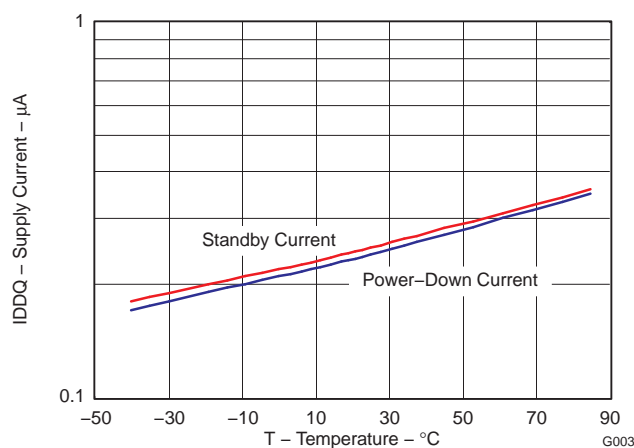


Figure 15.

SUPPLY CURRENT I_{DD} vs TEMPERATURE

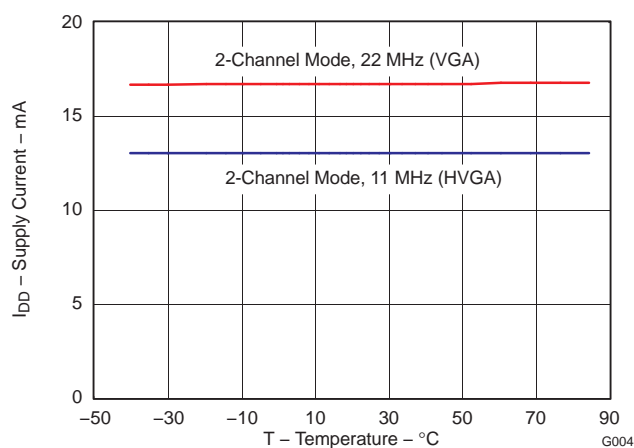


Figure 16.

SUPPLY CURRENT vs PCLK FREQUENCY

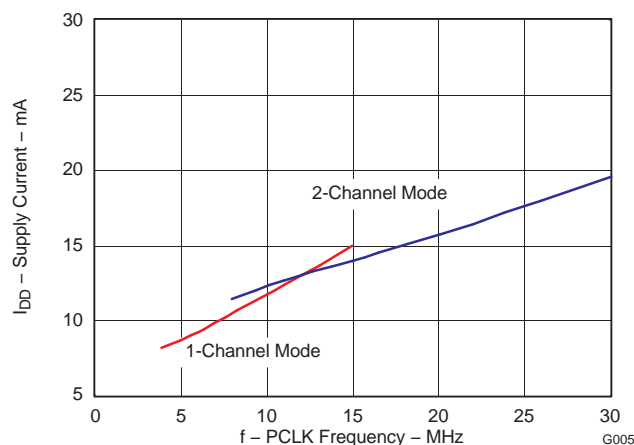


Figure 17.

DIFFERENTIAL OUTPUT SWING vs PCLK FREQUENCY

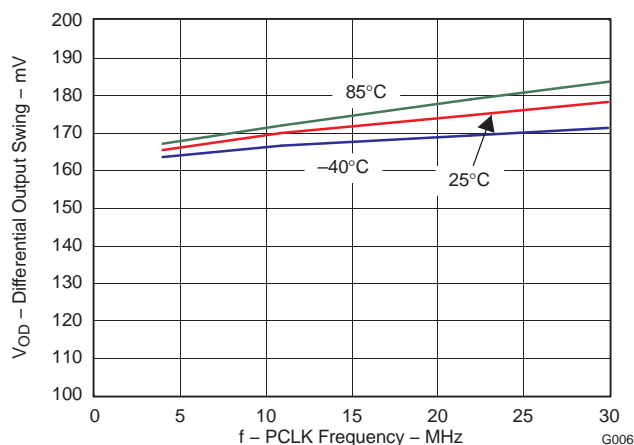


Figure 18.

PLL BANDWIDTH

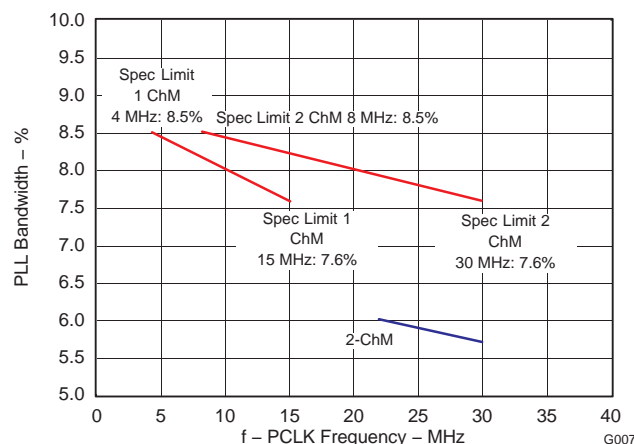


Figure 19.

**CYCLE-TO-CYCLE OUTPUT JITTER
vs PCLK FREQUENCY**

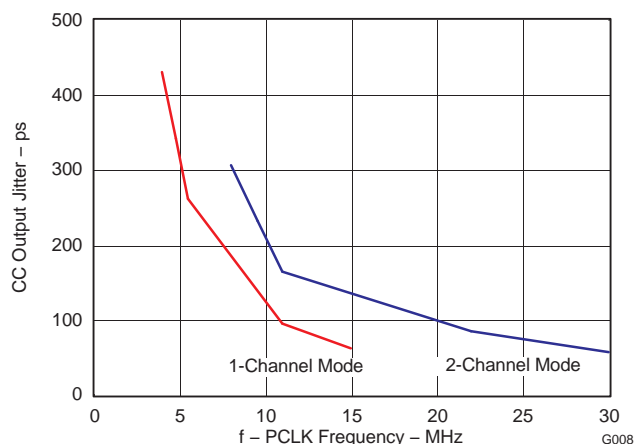
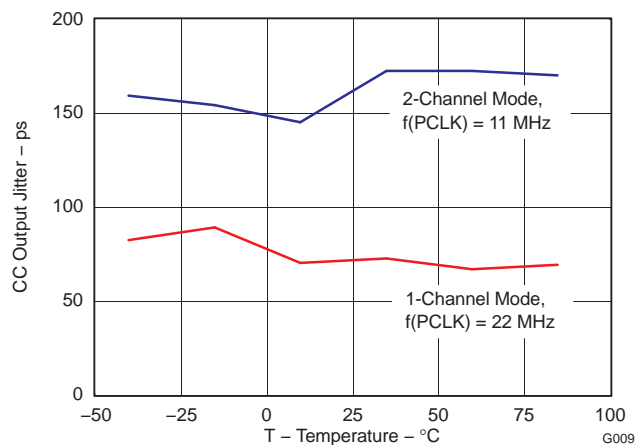
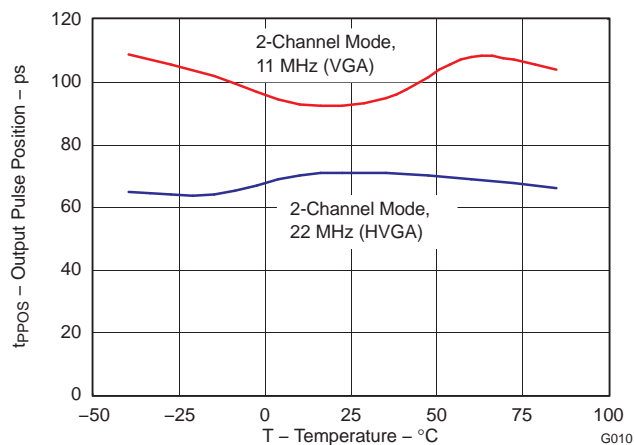
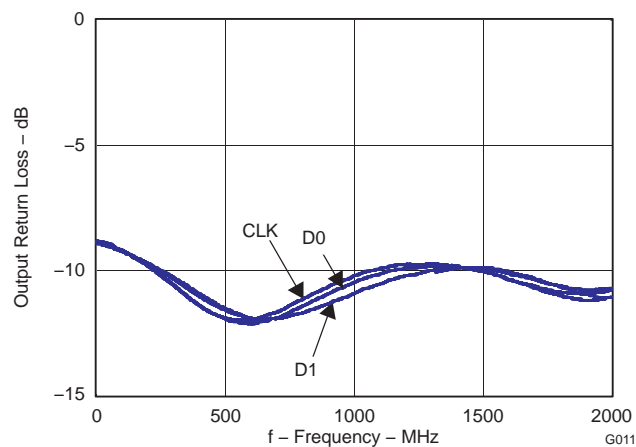
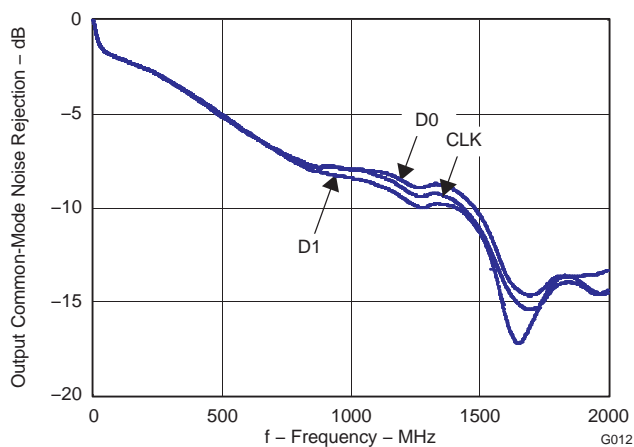
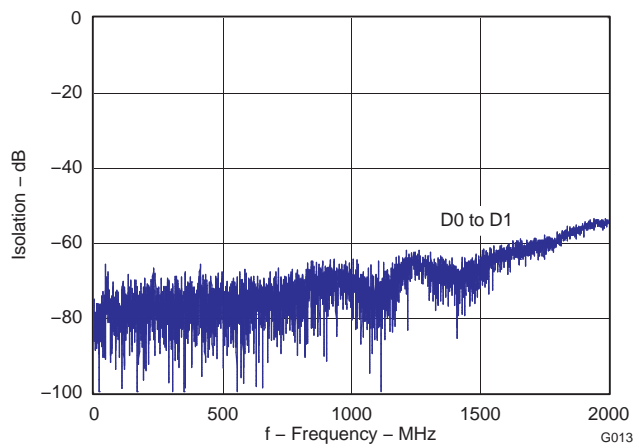


Figure 20.

TYPICAL CHARACTERISTICS (continued)**CYCLE-TO-CYCLE OUTPUT JITTER
vs TEMPERATURE****Figure 21.****OUTPUT PULSE POSITION vs TEMPERATURE****Figure 22.****OUTPUT RETURN LOSS****Figure 23.****OUTPUT COMMON MODE NOISE REJECTION****Figure 24.****CROSSTALK****Figure 25.**

APPLICATION INFORMATION

Preventing Increased Leakage Currents in Control Inputs

A floating (left open) CMOS input allows leakage currents to flow from VDD to GND. Do not leave any CMOS input unconnected or floating. Every input must be connected to a valid logic level, V_{IH} or V_{IL} , while power is supplied to VDD. This also minimizes the power consumption of standby and power-down modes.

Power Supply Design Recommendation

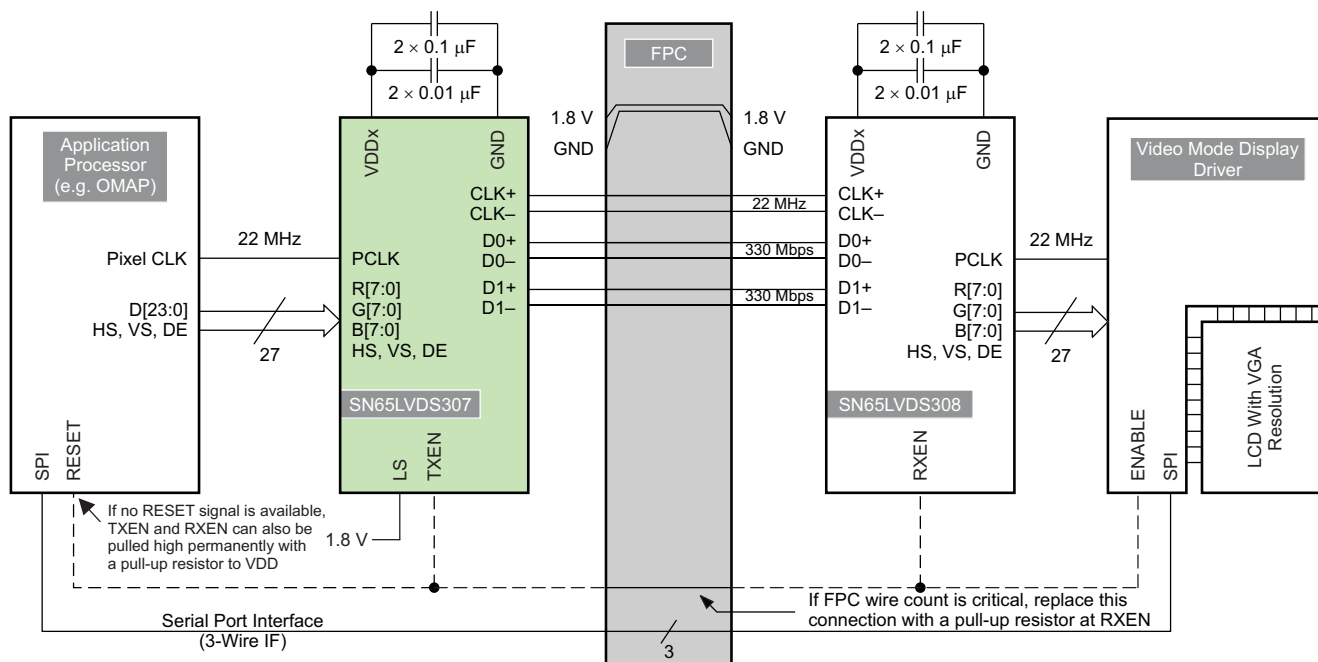
For a multilayer PCB, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

Decoupling Recommendation

The SN65LVDS307 was designed to operate reliably in a constricted environment with other digital switching ICs. In cell phone designs, the SN65LVDS307 often shares a power supply with other ICs. The SN65LVDS307 can operate with power-supply noise as specified in [Recommend Operating Conditions](#). To minimize the power-supply noise floor, provide good decoupling near the SN65LVDS307 power terminals. The use of four ceramic capacitors ($2 \times 0.01 \mu\text{F}$ and $2 \times 0.1 \mu\text{F}$) provides good performance. At the very least, it is recommended to install one $0.1\text{-}\mu\text{F}$ and one $0.01\text{-}\mu\text{F}$ capacitor near the SN65LVDS307. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and IC power inputs terminals must be minimized. Placing the capacitor underneath the SN65LVDS307 on the bottom of the PCB is often a good choice.

VGA Application

Figure 26 shows a possible implementation of a $640\text{-} \times 480\text{-}$ pixel VGA display. The SN65LVDS307 interfaces to the SN65LVDS308, which is the corresponding receiver device, to deserialize the data and drive the display driver. The pixel clock rate of 22 MHz assumes $\sim 20\%$ blanking overhead and 60-Hz display refresh rate. The application assumes 24-bit color resolution. Also shown is how the application processor provides a power-down (reset) signal for both serializer and the display driver. The signal count over the flexible printed-circuit board (FPC) could be further decreased by using the automatic standby detection feature on the SN65LVDS307 and/or SN65LVDS308 and pulling RXEN permanently high.



B0178-02

Figure 26. Typical VGA Display Application

APPLICATION INFORMATION (continued)**Typical Application Frequencies**

The SN65LVDS307 supports pixel clock frequencies from 4 MHz to 30 MHz. [Table 13](#) provides a few typical display resolution examples. The blanking overhead is assumed to be 20%. Often, blanking overhead is smaller, resulting in a lower data rate.

Table 13. Typical Application Data Rates and Serial Pair Usage

Display Screen Resolution	Visible Pixel Count	Blanking Overhead	Display Refresh Rate [Hz]	Pixel Clock Frequency [MHz]	Data Rate on	
					D0 With LS = 0	D0 and D1 With LS = 1
240 × 320 (QVGA)	76,800	20%	90	8.3	249 Mbps	124 Mbps
240 × 320 (QVGA)	76,800		60	5.5	166 Mbps	–
640 × 200	128,000			9.2	276 Mbps	138 Mbps
352 × 416 (CIF+)	146,432			10.5	316 Mbps	158 Mbps
352 × 440	154,880			11.2	335 Mbps	167 Mbps
320 × 480 (HVGA)	153,600			5.5	166 Mbps	–
320 × 480 (HVGA)	153,600		30	11.1	332 Mbps	166 Mbps
800 × 250	200,000		60	14.4	432 Mbps	216 Mbps
640 × 320	204,800			14.7	442 Mbps	221 Mbps
640 × 480 (VGA)	307,200			22.1	–	332 Mbps
640 × 480 (VGA)	307,200		30	11.1	332 Mbps	166 Mbps
1024 × 320	327,680		60	23.6	–	354 Mbps
854 × 480 (WVGA)	409,920			29.5	–	443 Mbps
800 × 600 (SVGA)	480,000		30	17.3	–	259
1024 × 768 (XGA)	786,432			28.3	–	425

Calculation Example: HVGA Display

The following calculation shows an example for a typical half-VGA display with the following parameters:

Display resolution:	480 × 320
Frame refresh rate:	58.4 Hz
Vertical visible pixels:	320 lines
Vertical front porch:	10 lines
Vertical sync:	5 lines
Vertical back porch:	3 lines
Horizontal visible pixels:	480 columns
Horizontal front porch:	20 columns
Horizontal sync:	5 columns
Horizontal back porch:	3 columns

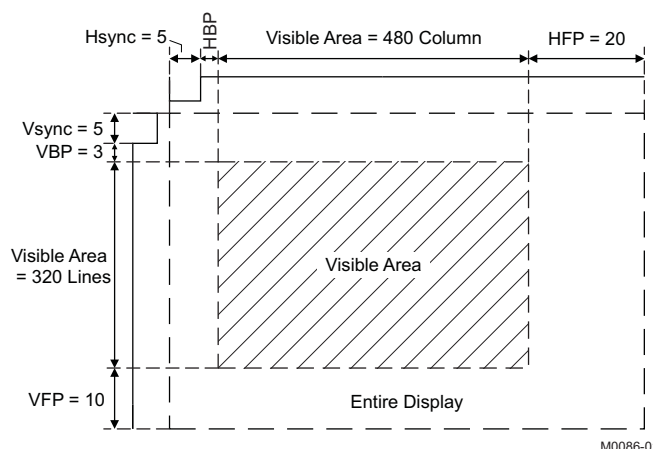


Figure 27. HVGA Display Parameters

Calculation of the total number of pixels and blanking overhead:

Visible area pixel count:	$480 \times 320 = 153,600$ pixels
Total frame pixel count:	$(480 + 20 + 5 + 3) \times (320 + 10 + 5 + 3) = 171,704$ pixels
Blanking overhead:	$(171,704 - 153,600) \div 153,600 \approx 11.8\%$

The application requires following serial-link parameters:

Pixel clock frequency:	$171,704 \times 58.4 \text{ Hz} = 10 \text{ MHz}$
Serial data rate:	1-channel mode: $10 \text{ MHz} \times 30 \text{ bits/channel} = 300 \text{ Mbps}$
	2-channel mode: $10 \text{ MHz} \times 15 \text{ bits/channel} = 150 \text{ Mbps}$

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65LVDS307ZQCR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQC	48	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
SN65LVDS307ZQCT	ACTIVE	BGA MI CROSTA R JUNI OR	ZQC	48	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS307ZQCR	BGA MICROSTAR JUNIOR	ZQC	48	2500	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q1
SN65LVDS307ZQCT	BGA MICROSTAR JUNIOR	ZQC	48	250	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

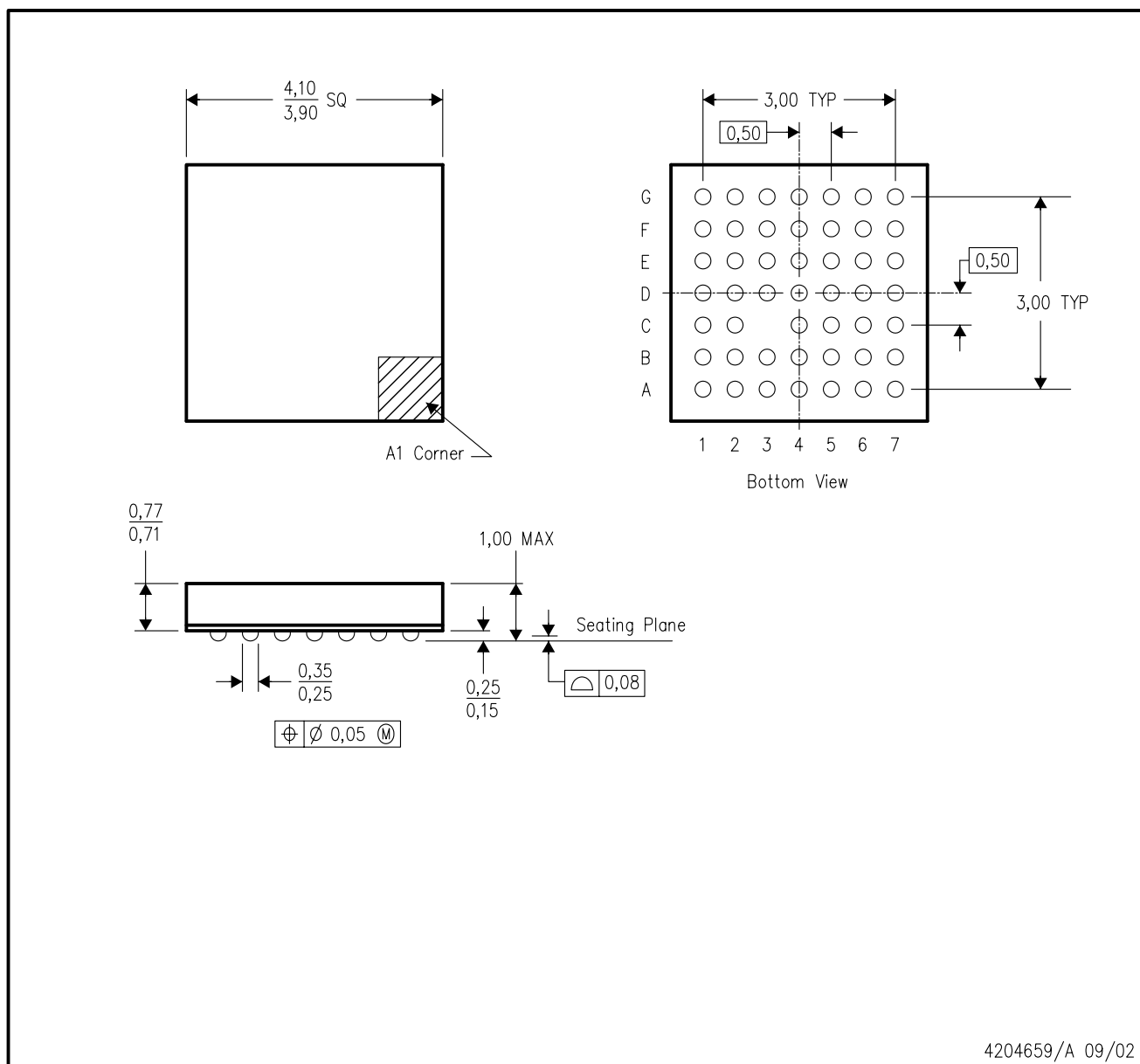


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS307ZQCR	BGA MICROSTAR JUNIOR	ZQC	48	2500	338.1	338.1	20.6
SN65LVDS307ZQCT	BGA MICROSTAR JUNIOR	ZQC	48	250	338.1	338.1	20.6

ZQC (S-PBGA-N48)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MicroStar Junior™ BGA configuration
 - D. Falls within JEDEC MO-225
 - E. This package is lead-free.

MicroStar Junior is a trademark of Texas Instruments.

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