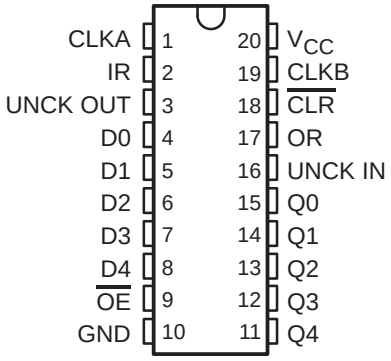
- **Independent Asychronous Inputs and Outputs**
- **16 Words by 5 Bits**
- **DC to 10-MHz Data Rate**
- **3-State Outputs**
- **Packaged in Standard Plastic 300-mil DIPs**

N PACKAGE
(TOP VIEW)



description

This 80-bit active-element memory is a monolithic Schottky-clamped transistor-transistor logic (STTL) array organized as 16 words by 5 bits. A memory system using the SN74S225 easily can be expanded in multiples of 48 words or of 10 bits as shown in Figure 3. The 3-state outputs controlled by a single output-enable ($\overline{OE}$) input make bus connection and multiplexing easy.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from dc to 10 MHz in a bit-parallel format, word by word.

Reading or writing is done independently, utilizing separate asynchronous data clocks. Data can be written into the array on the low-to-high transition of either load-clock (CLKA, CLKB) input. Data can be read out of the array on the low-to-high transition of the unload-clock (UNCK IN) input (normally high). Writing data into the FIFO can be accomplished in one of two ways:

- In applications not requiring a gated clock control, best results are achieved by applying the clock input to one of the clocks while tying the other clock input high.
- In applications needing a gated clock, the load clock (gate control) must be high for the FIFO to load on the next clock pulse.

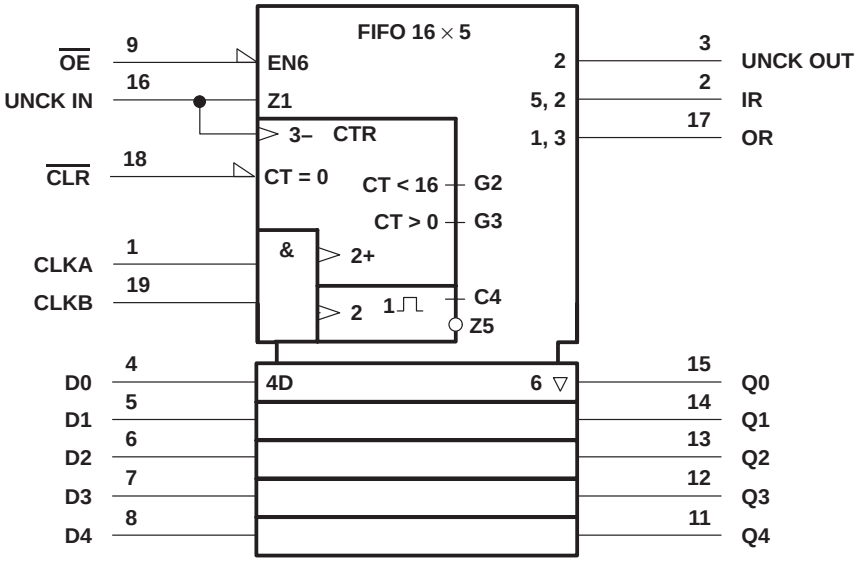
CLKA and CLKB can be used interchangeably for either clock gate control or clock input.

Status of the SN74S225 is provided by three outputs. The input-ready (IR) output monitors the status of the last word location and signifies when the memory is full. This output is high whenever the memory is available to accept any data. The unload-clock (UNCK OUT) output also monitors the last word location. This output generates a low-logic-level pulse (synchronized to the internal clock pulse) when the location is vacant. The third status output, output ready (OR), is high when the first word location contains valid data and UNCK IN is high. When UNCK IN goes low, OR will go low and stay low until new valid data is in the first word position. The first word location is defined as the location from which data is provided to the outputs.

The data outputs are noninverted with respect to the data inputs and are 3-state, with a common control input ($\overline{OE}$). When $\overline{OE}$ is low, the data outputs are enabled to function as totem-pole outputs. A high logic level forces each data output to a high-impedance state while all other inputs and outputs remain active.The clear ($\overline{CLR}$) input invalidates all data stored in the memory array by clearing the control logic and setting OR to a low logic level on the high-to-low transition of a low-active pulse.

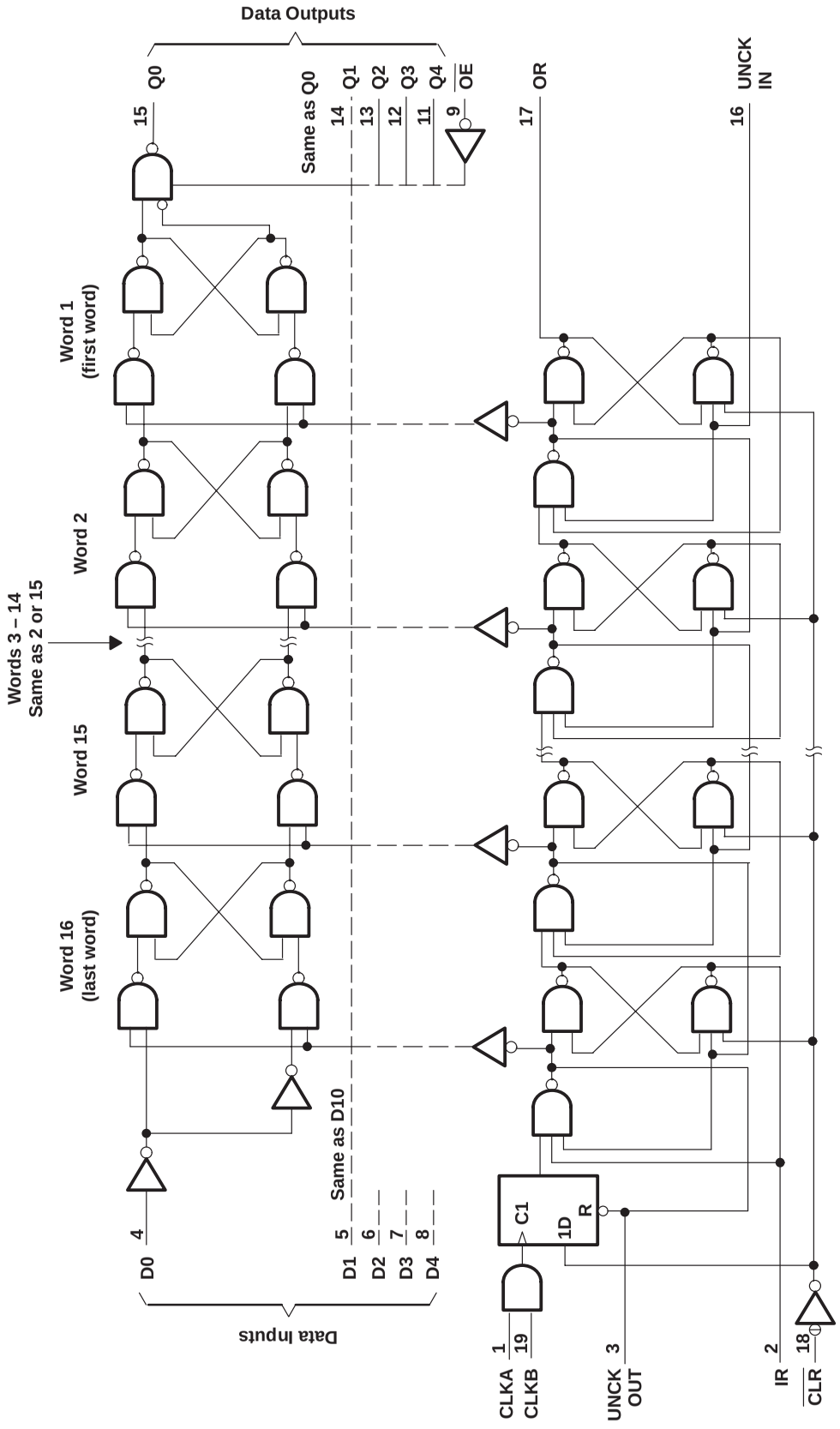
The SN74S225 is characterized for operation from 0°C to 70°C.

logic symbol†

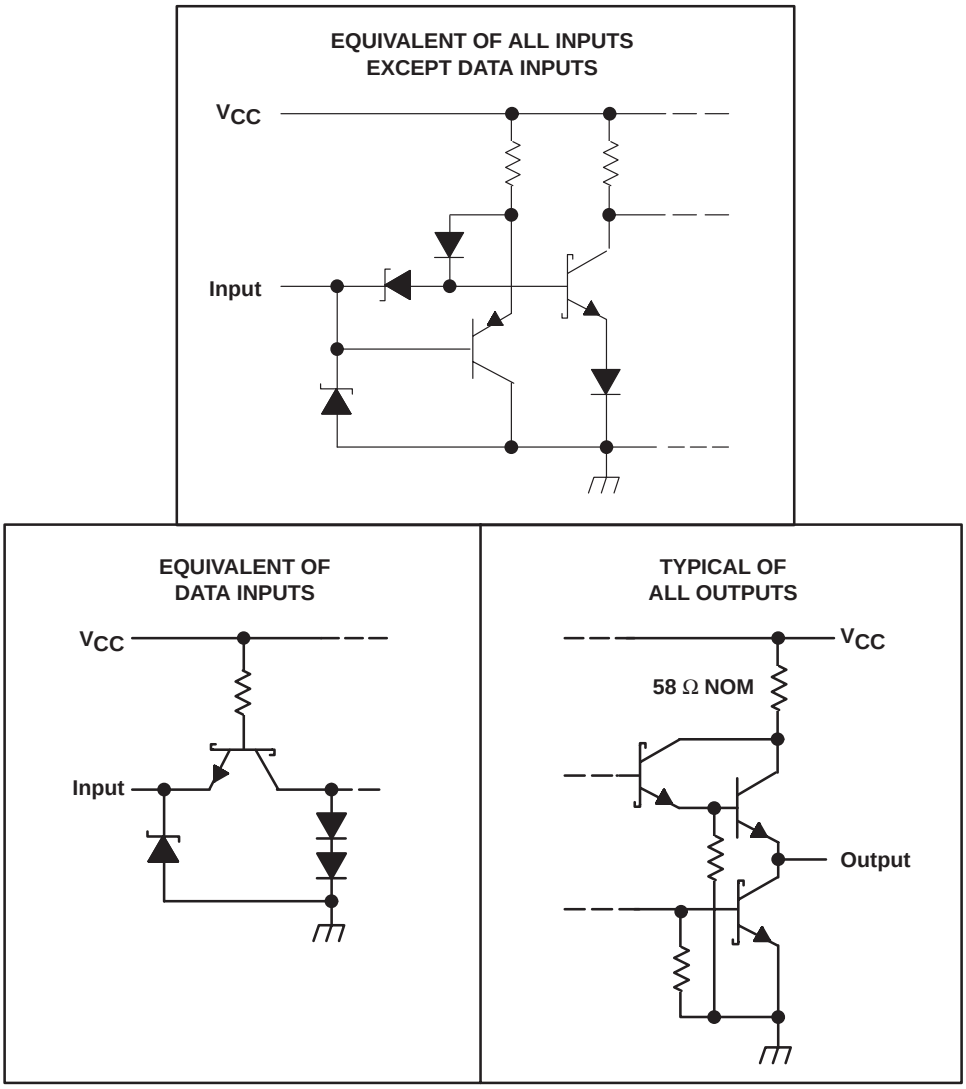


† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

functional block diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range, V_I . . . . . –0.5 V to 5.5 V
Off-state output voltage range . . . . . –0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 67°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			–6.5	mA
		All other outputs			–3.2	
I_{OL}	Low-level output current	Q outputs			16	mA
		All other outputs			8	
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA			–1.2	V
V_{OH}	Q outputs	V_{CC} = 4.75 V,	I_{OL} = –6.5 mA	2.4	2.9		V
	All others	V_{CC} = 4.75 V,	I_{OL} = –3.2 mA	2.4	2.9		
V_{OL}	Q outputs	V_{CC} = 4.75 V,	I_{OL} = 16 mA		0.35	0.5	V
	All others	V_{CC} = 4.75 V,	I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.25 V,	V_O = 2.4 V			50	µA
I_{OZL}		V_{CC} = 5.25 V,	V_O = 0.5 V			–50	µA
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			1	mA
I_{IH}	Data	V_{CC} = 5.25 V,	V_I = 2.7 V			40	µA
	All others					25	
I_{IL}	Data	V_{CC} = 5.25 V,	V_I = 0.5 V			–1	mA
	All others					–0.25	
I_{OS}‡		V_{CC} = 5.25 V,	V_O = 0	–30		–100	mA
I_{CC}§		V_{CC} = 5.25 V			80	120	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Duration of the short circuit should not exceed one second.
§ I_{CC} is measured with all inputs grounded and the outputs open.

timing requirements over recommended operating conditions (unless otherwise noted) (see Figure 1)

			MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency				10	MHz
t_w	Pulse duration	CLKA or CLKB high	25			ns
		UNCK IN low	7			
		$\overline{CLR}$ low	40			
t_{su}	Setup time before CLKA↑ or CLKB↑	Data (see Note 3)	–20			ns
		$\overline{CLR}$ inactive	25			
t_h	Hold time after CLKA↑ or CLKB↑		70			ns

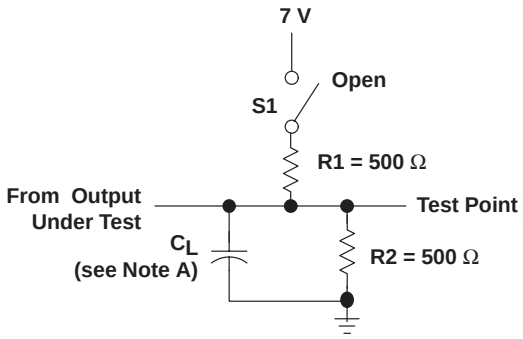
NOTE 3: Data must be set up within 20 ns after the load-clock positive transition.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}	CLKA		C_L = 30 pF	10	20		MHz
	CLKB			10	20		
	UNCK IN			10	20		
t_w	UNCK OUT		C_L = 30 pF	7	14		ns
t_{dis}	OE	Any Q	C_L = 5 pF		10	25	ns
t_{en}	OE	Any Q	C_L = 30 pF		25	40	ns
t_{PLH}	UNCK IN	Any Q	C_L = 30 pF		50	75	ns
t_{PHL}					50	75	
t_{PLH}	CLKA or CLKB	OR	C_L = 30 pF		190	300	ns
t_{PLH}	UNCK IN	OR	C_L = 30 pF		40	60	ns
t_{PHL}					30	45	
t_{PHL}	CLR	OR	C_L = 30 pF		35	60	ns
	CLKA or CLKB	UNCK OUT			25	45	
	UNCK IN				270	400	
	CLKA or CLKB	IR			55	75	
t_{PLH}	UNCK IN	IR	C_L = 30 pF		255	400	ns
	$\overline{CLR}$				16	35	
	OR↑	Any Q			10	20	

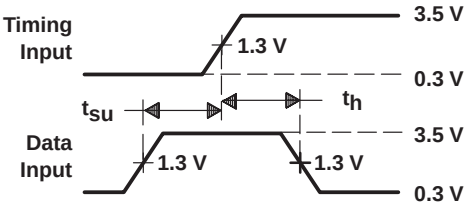
† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

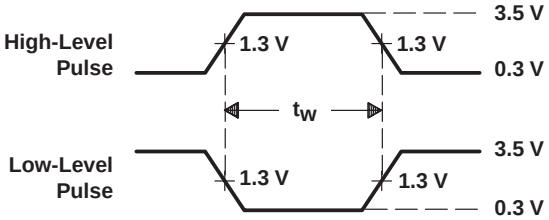


LOAD CIRCUIT FOR 3-STATE OUTPUTS

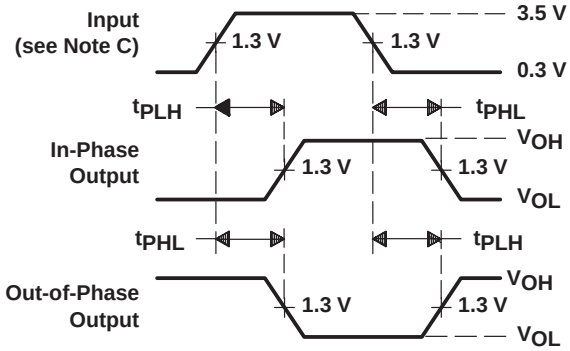
PARAMETER		S1
t_{en}	t_{PZH}	Open
	t_{PZL}	Closed
t_{dis}	t_{PHZ}	Open
	t_{PLZ}	Closed
t_{pd}	t_{PLH}	Open
	t_{PHL}	Open



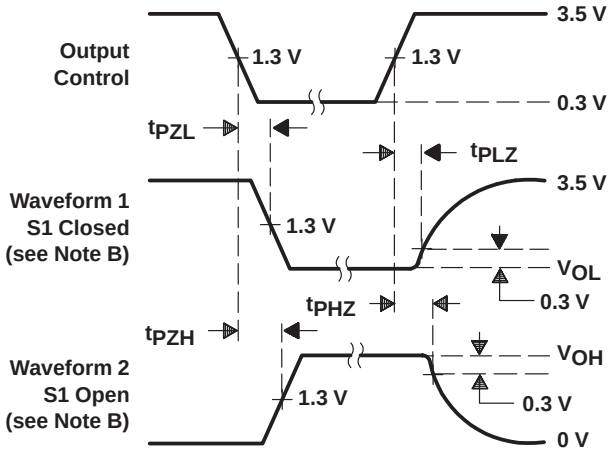
VOLTAGE WAVEFORMS
SET UP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

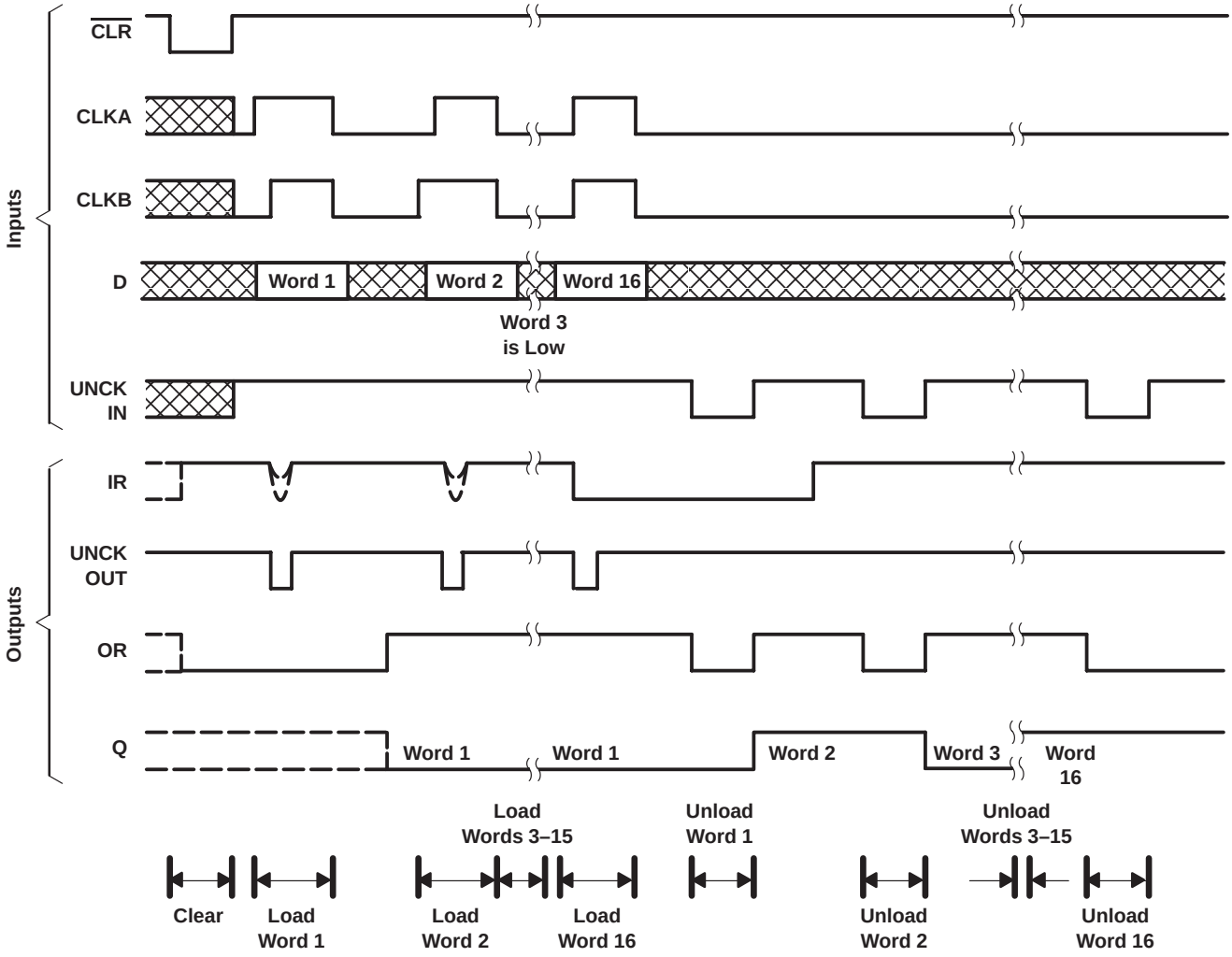


Figure 2. Typical Waveforms for a 16-Word FIFO

APPLICATION INFORMATION

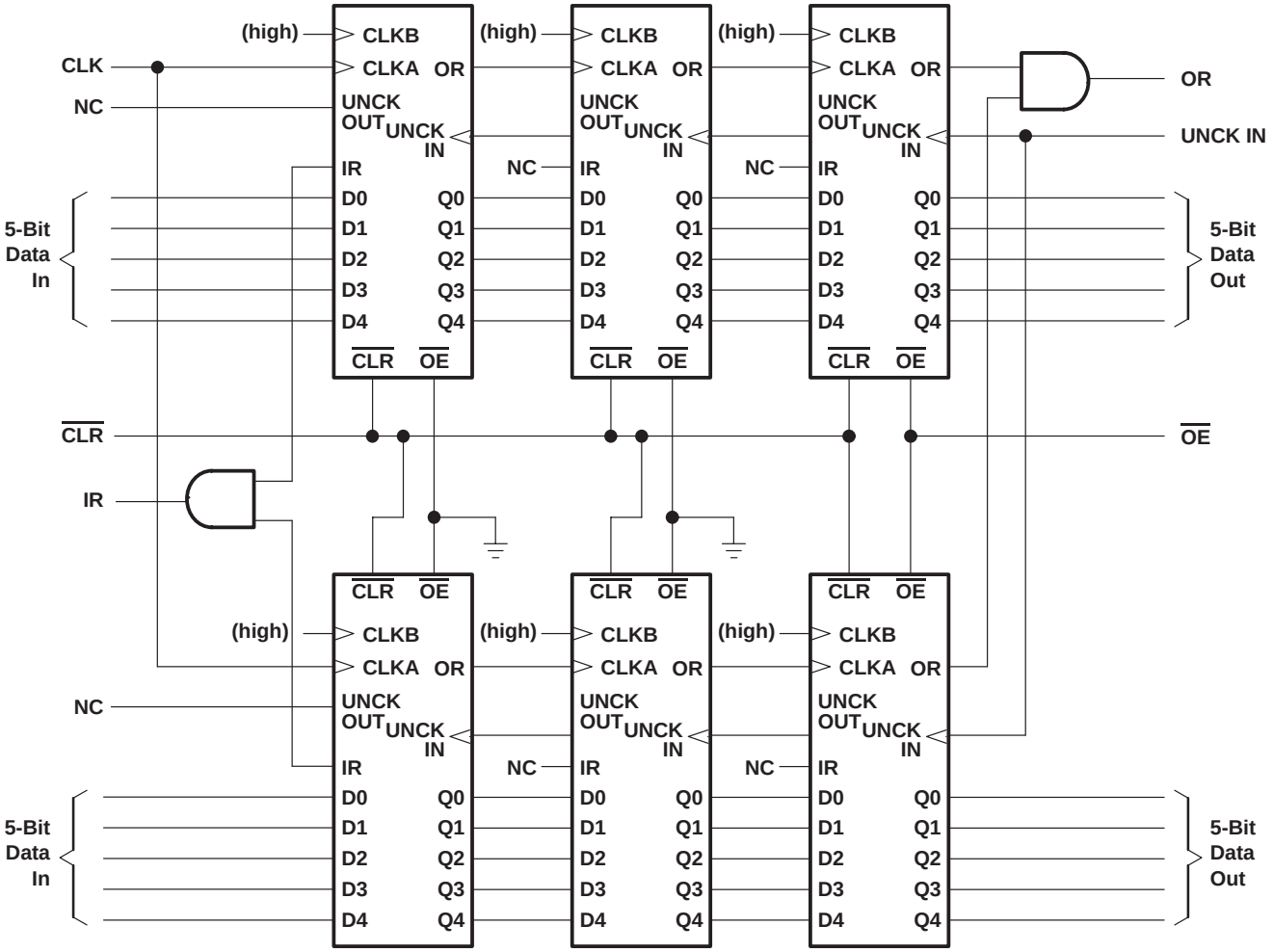


Figure 3. Word-Width Expansion: 48 × 10 Bits

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.