Flip Flops, Series 54/74

DM5473 / DM7473 (SN5473/SN7473)
DM5476 / DM7476 (SN5476/SN7476)
DM54107 / DM74107 (SN54107/SN74107)
dual JK master/slave flip flops

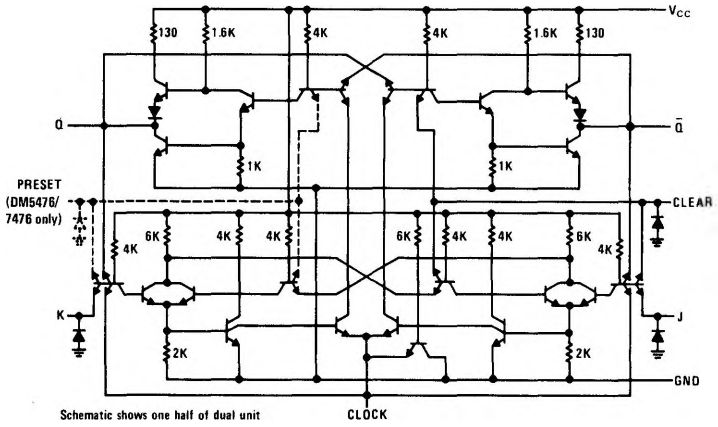
general description

The flip flops described herein are TTL (Transistor-Transistor Logic) dual JK Master/Slave flip flops. Asynchronous CLEAR inputs are provided on the DM5473/DM7473 and DM54107/DM74107 flip flops; and PRESET and CLEAR inputs are available on each of the DM5476/DM7476 flip flops. The latter devices are supplied in a 16 pin package. The devices are totally monolithic and designed for use in high speed control and counting applications, where economy is required, and multiple data inputs are not required. These devices meet all of the electrical and mechanical requirements of the equivalent Series 54/74 devices. They feature:

- High Speed of Operation — 25 MHz toggling
- Optimum Power Dissipation — 45 mW/ff
- High Noise Immunity — 1V
- Guaranteed Clock Skew — 15 ns

The devices also feature a special clock line clamp to reduce ringing and prevent false clocking. In addition, the usual speed-power efficiency and high output drive-capability normally gained with TTL circuits are retained.

schematic and connection diagrams

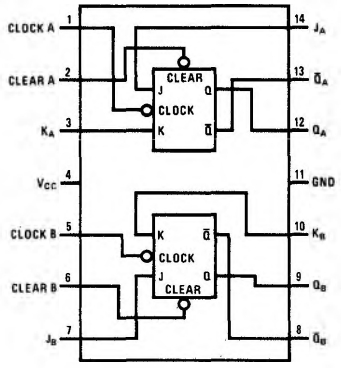


Schematic shows one half of dual unit

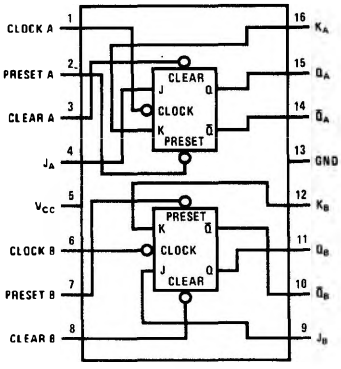
truth table

(Each Flip Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

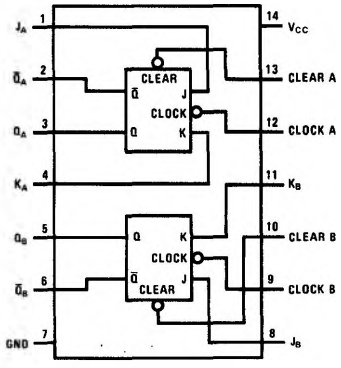
t_n = bit time before clock pulse.
t_{n+1} = bit time after clock pulse.



DM5473/DM7473



DM5476/DM7476



DM54107/DM74107

absolute maximum ratings

Supply Voltage	+7V
Input Voltage	5.5V
Fan Out	10
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
DM5473/DM5476/DM54107	−55°C to +125°C
DM7473/DM7476/DM74107	0°C to +70°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER		CONDITION		MIN.	TYP.	MAX.	UNITS
Clock Line Clamp Voltage	DM5473/DM5476/DM54107	V_{CC} = 5.5V	I_{CLOCK} = −10 mA		−.3	−0.5	V
	DM7473/DM7476/DM74107	V_{CC} = 5.25V					
Input Diode Clamp (J, K, Preset, Clear)		V_{CC} = 5.0V	T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	DM5473/DM5476/DM54107	V_{CC} = 4.5V		2.0			V
	DM7473/DM7476/DM74107	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM5473/DM5476/DM54107	V_{CC} = 4.5V				0.80	V
	DM7473/DM7476/DM74107	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM5473/DM5476/DM54107	V_{CC} = 4.5V	I_{OUT} = −400 μA	2.4	3.3		V
	DM7473/DM7476/DM74107	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM5473/DM5476/DM54107	V_{CC} = 4.5V	I_{OUT} = 16.0 mA		0.20	0.40	V
	DM7473/DM7476/DM74107	V_{CC} = 4.75V					
Logical "0" Input Current	DM5473/DM5476/DM54107	V_{CC} = 5.5V	V_{IN} = 0.40V, J or K		−1.0	−1.6	mA
	DM7473/DM7476/DM74107	V_{CC} = 5.25V	Clear, Preset or Clock		−2.0	−3.2	
Logical "1" Input Current	DM5473/DM5476/DM54107	V_{CC} = 5.5V	V_{IN} = 2.4V, J or K		10	40	μA
	DM7473/DM7476/DM74107	V_{CC} = 5.25V	Clear, Preset		20	80	
			Clock		<0	80	
Logical "1" Input Current	DM5473/DM5476/DM54107	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM7473/DM7476/DM74107	V_{CC} = 5.25V					
Output Short Current (Note 2)	DM5473/DM5476/DM54107	V_{CC} = 5.5V	V_{OUT} = 0V	−20		−55	mA
	DM7473/DM7476/DM74107	V_{CC} = 5.25V		−18			
Power Supply Current (each flip-flop)	DM5473/DM5476/DM54107	V_{CC} = 5.5V	V_{IN} = 5.0V		9	17	mA
	DM7473/DM7476/DM74107	V_{CC} = 5.25V					
Minimum Allowable Clock Pulse Width (Note 3)		V_{CC} = 5.0V, T_A = 25°C				20	ns
Toggle Frequency		V_{CC} = 5.0V, T_A = 25°C		15	25		MHz
Propagation Delay Time to a Logical "0" from Clock, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C		15	26	45	ns
Propagation Delay Time to a Logical "1" from Clock, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C		10	17	30	ns
Propagation Delay Time to a Logical "0" from Clear, or Preset		V_{CC} = 5.0V, T_A = 25°C		12	23	40	ns
Propagation Delay Time to a Logical "1" from Clear, or Preset		V_{CC} = 5.0V, T_A = 25°C		7	14	25	ns
Time after Negative going Clock Transition that J or K information must be held, t_{hold}		V_{CC} = 5.0V, T_A = 25°C				−5	ns
Clock Skew ($t_{pd\ min} - t_{hold\ max}$)		V_{CC} = 5.0V, T_A = 25°C		15			ns

Note 1: Min/max limits apply across the guaranteed operating temperature range of −55°C to +125°C for the DM5473/DM5476/DM54107 and 0°C to 70°C for the DM7473/DM7476/DM74107 unless specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2: Only one output may be shorted at a time.

Note 3: The flip flop will always recognize a 20 ns pulse, never recognize a 5 ns pulse.

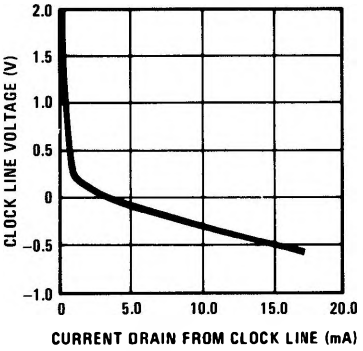
Note 4: No maximum rise and fall times are imposed upon clock or J and K waveforms. However, very slow transitions which allow an input to remain in the threshold region can cause noise problems.

Note 5: See explanation given under "Device Operation."

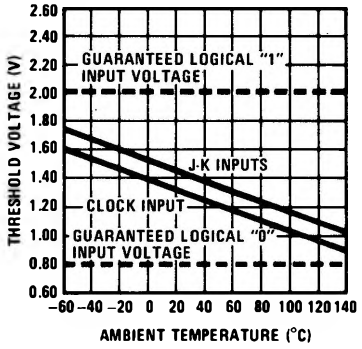
Note 6: J and K information will register properly even though the information is removed 5 ns before the clock pulse voltage falls. However when this occurs it must be assured that the Logical "1" clock pulse level and the desired J and K information occur simultaneously for at least 20 ns.

typical performance characteristics

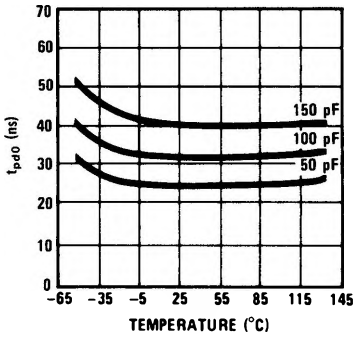
Typical Clock Line Voltage vs Clock Line Current



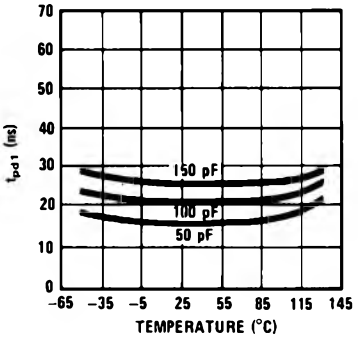
Typical Threshold Voltage vs Temperature



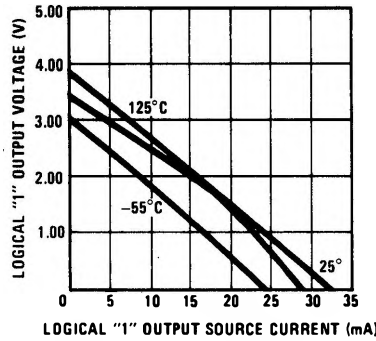
Transition Time to Logical "0" (t_{pd0}) vs Temperature



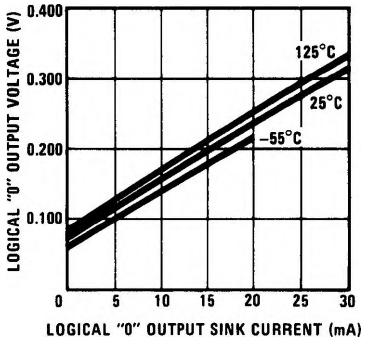
Transition Time to Logical "1" (t_{pd1}) vs Temperature



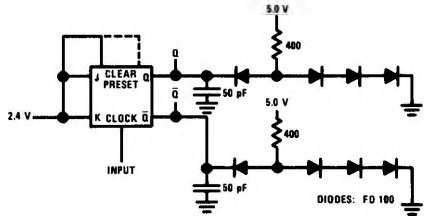
Logical "1" Output Voltage vs Source (Output) Current

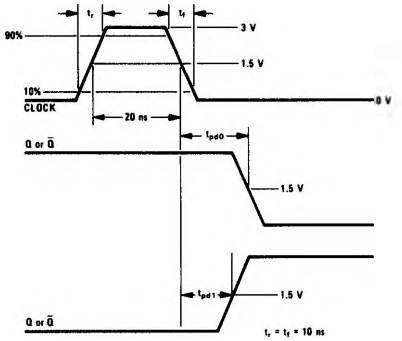


Logical "0" Output Voltage vs Sink Current



ac test circuit





switching time waveforms (Notes 4, 5)