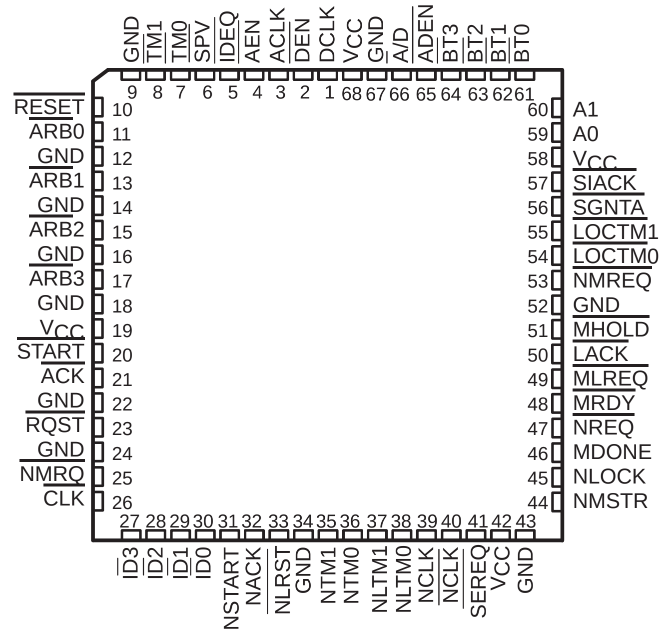
SCHS010 – D3158, OCTOBER 1988 – REVISED JANUARY 1991

- **Designed for NuBus™ Interface Applications**
- **Supports Master, Slave, and Master/Slave Applications**
- **Conforms to ANSI/IEEE Std 1196-1987**
- **Designed to Operate With SN74BCT2420 NuBus™ Data/Address Interface Devices**
- **Supports NuBus™ 1987 Block Transfers With the Addition of the SN74ALS2442**
- **EPIC™ (Enhanced Performance Implanted CMOS) 1-µm Process**
- **Fully TTL-Compatible**
- **Dependable Texas Instruments Quality and Reliability**

FN PACKAGE
(TOP VIEW)



description

The SN74ACT2440 NuBus™ Controller handles NuBus™ signaling protocol in compliance with ANSI/IEEE Std 1196-1987. The device allows a simple connection to the NuBus™; typical configurations include master-only, slave-only, and master/slave. Additionally, it provides extra status and control lines to facilitate more sophisticated approaches. With the addition of the SN74ALS2442, slave block transfers can be supported by this device. For additional details on block transfers, consult the SN74ALS2442 data sheet and the application note titled *Supporting NuBus™ Block Slave Transfers Using Texas Instruments SN74ACT2440, SN74BCT2420, and SN74ALS2442*.

Figure 1 shows a typical NuBus™ interface using the 'ACT2440. Data and address buffering is handled via two SN74BCT2420s. The SN74BCT2420s are BiCMOS buffers designed specifically for supporting NuBus™ interfacing. The 'ACT2440 provides the buffer control signals needed to directly drive the SN74BCT2420s; however, in simpler applications, standard SSI and MSI buffers may be used in place of the 'BCT2420s.

The 'ACT2440 is comprised of five major signal groups: byte decode signals, data/address interface-control signals, master/slave input signals, NuBus™ card-slot signals, and NuBus™ status signals. Byte decode determines which type of NuBus™ cycle is being performed. Data/address interface control provides the buffering signals required to multiplex and de-multiplex the NuBus™ data/address lines. The master/slave inputs control the master- and slave-state machines. The NuBus™ card-slot signals interface with the NuBus™. The NuBus™ status signals indicate the status of the master/slave-state machines and provide buffered NuBus™ signals. Refer to Table 1 for additional details.

The SN74ACT2440 is characterized for operation from 0°C to 70°C.

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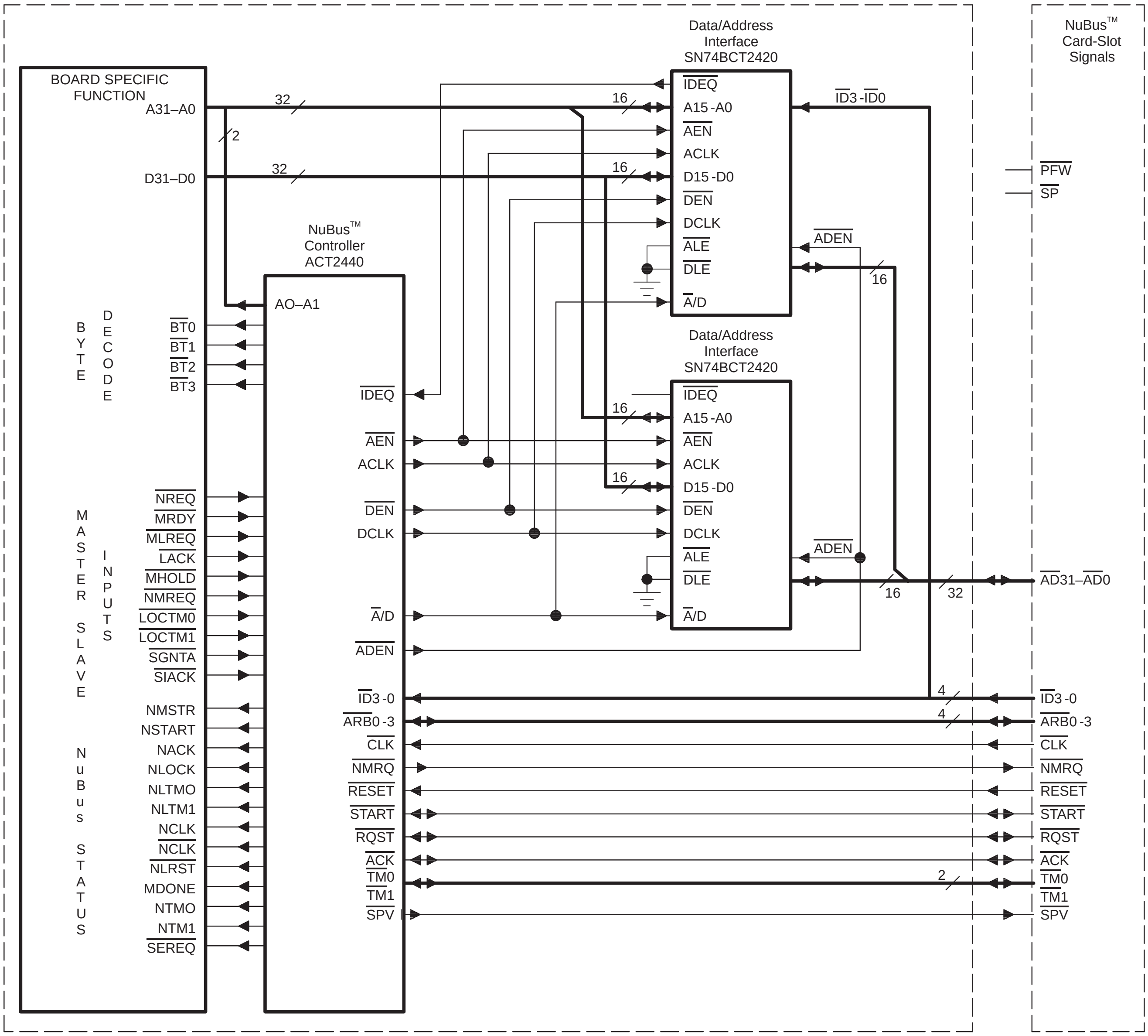

Figure 1. Typical ’ACT2440 NuBus™ Interface

Terminal Functions

As previously explained, the input and output signals on the ’ACT2440 can be functionally organized into five groups. The following tables briefly describe the controller signals in each group.

DATA/ADDRESS INTERFACE CONTROL SIGNALS

PIN NAME	PIN NO.	DESCRIPTION
ACLK	3	Address clock. This output loads NuBus™ address information onto the local board. During both master and slave start cycles, this output changes on the sample edge (high-to-low) of the NuBus™ clock signal (CLK).
A/D	66	Output select. This normally high output controls the multiplexing function of the address and data information onto theNuBus™. When low, address information is indicated. When high, data information is indicated. When the local boardis the NuBus master, A/D goes low on the driving edge (low-to-high) of start and remains low for one NuBus™ clock period.
ADEN	65	Output enable. This active-low output enables data or address information onto the NuBus™. ADEN is asserted on the driving edge (low-to-highof the NuBus™ clock signal (CLK) under any of the following conditions: – The local board is the NuBus™ master performing a write cycle and continuing until an acknowledge (ACK) is received from the NuBus™. – The local board is the NuBus™ master performing a read cycle and continuing for one NuBus™ clock cycle. – The local board is the selected NuBus™ slave during an acknowledge cycle and the current cycle is a read.
AEN	4	Address enable. This active-low output signal enables address information onto the local board. When selected as a NuBus™ slave, AEN goes low on the first sample edge after slave grant access (SGNTA) is asserted. AEN returns inactive on the first sample edge after (SGNTA) returns inactive. If SGNTA is active (low) before the first sample edge after START, then address information is placed onto the local board on the first sample edge after START.
DCLK	1	Data clock. This output loads NuBus™ data onto the local board. This output changes on the sample edge (high-to-low) of the NuBus™ clock signal (CLK) under any of the following sets of comditions: – The local board is the NuBus™ master, the current cycle is a read, and an acknowledge (ACK) or interim acknowledge (TM0 during block transfers) has been received. – The local board is a NuBus™ slave, the current cycle is a write, and slave grant access (SGNTA) is asserted. – The local board is a NuBus™ slave, the current cycle is a block write. The first rising edge of DCLK will occur on the first sample edge after SGNTA is taken active (low) and will remain high for two clock cycles. If SGNTA is active (low) during the start cycle, DCLK will go active (high) on the first sample edge after START. The SIACK iinput controls the remaining DCLK cycles with the exception of the last DCLK cycle. When the SIACK input is taken active (low), DCLK will go active on the following sample edge. DCLK will remain high for one clock cycle and return low, regardless of the SIACK input. The final DCLK cycle is controlled by the Local Acknowledge Input (LACK), as on normal write cycles.
DEN	2	Data Enable. The active-low output enables data to be placed onto the local board. DEN is asserted under either of the following conditions: – The local board is the NuBus™ master performing a read cycle. (DEN goes low on the sample edge (high-to-low) of the acknowledge cycle and remains low until the first sample edge after MHOLD returns inactive.) The local board is the selected NuBus™ slave performing a write cycle. (DEN goes low on the first sample edge after slave grant access (SGNTA) is asserted and remains low until the first sample edge after SGNTA returns inactive.)

Terminal functions (continued)

MASTER/SLAVE INPUT SIGNALS

PIN NAME	PIN NO.	DESCRIPTION
IDEQ	5	ID equal. This active-low input signal is used by the slave-state machine to detect if the current NuBus™ cycle is addressing the local board. This input is interrogated on the sample edge (high-to-low) of the NuBus™ clock in the cycle following the start cycle. This input is asserted if slot and/or super-slot addresses are broadcast on the previous start cycle
LACK	50	Local acknowledge. This active-low input signal controls the NuBus™ acknowledge signal (ACK) during slave cycles. When the local board is ready to respond to a NuBus™ transfer request, this input signal is driven low. The ACK output will go active (low) on the next driving edge after LACK is sampled.
LOCTM0 LOCTM1	54 55	Local transfer-mode control. These input signals determine the sense of the NuBus™ transfer-mode signals, TM0 and TM1, during master start and slave acknowledge cycles. The controller latches these signals upon detecting the NuBus™. Request signal (NREQ). During a NuBus™ slave acknowledge cycle, the NuBus™ TM lines reflect the current state of these inputs.
MHOLD	51	Master hold. This active-low input signal is used by the buffer control logic to hold data on the local board after the NuBus™ cycle terminates. If this signal is true when the acknowledge cycle is received (for a NuBus™ cycle initiated by this controller) and the current cycle is a NuBus™ read, then the data enable signal (DEN) remains true until MHOLD is unasserted. Additionally, the latched TM status lines (NLTMO, NLTM1) continue to reflect the TM information presented on the NuBus™ during the acknowledge cycle (this applies to both reads and writes). While the holding function is active, the controller inhibits the local master from issuing another NuBus™ start cycle when NREQ is not taken inactive after the acknowledge. In other words, MHOLD allows only one start cycle to occur.
MLREQ	49	Master lock request. This active-low input signal, in conjunction with NREQ, causes the controller to lock the NuBus™ by issuing an attention lock resource cycle after winning arbitration. When MLREQ is taken inactive, the controller automatically issues a NuBus™ attention null cycle (regardless of the state of NREQ). The attention null cycle signals the end of the locked resource tenture.
MRDY	48	Master ready. This active-low input signal indicates to the controller that the local board is ready to perform a NuBus™ master start cycle. The current state of the master-state machine determines this signal’s effect. If the master-state machine enters the arbitration process (with no lock request) and wins mastership of the bus, this signal can delay issuing a start cycle for up to 16 NuBus™ clocks periods. After this period, the master–state machine automatically issues a NuBus™ attention null cycle, returns to the idle state, and re-enters the arbitration process with lock request asserted, it issues an attention lock cycle immediately upon acquiring mastership of the bus. The master-state machine then waits for MRDY to be asserted before issuing a NuBus™ start cycle. There is no timer in the lock mode. If the master-state machine is parked on the bus, this signal is simply ANDed with the NuBus™ request signal (NREQ) to generate the start cycle.
NMREQ	53	NonMaster request. This nonsynchronous active-low input asserts the NuBus™ NonMaster request signal (NMRQ)
NREQ	47	NuBus™ request. This active-low input signal indicates to the controller that the local board wants access to the NuBus™. It initiates arbitration if the local board is not already the bus master.
SGNTA	56	Slave grant access. This active-low input signal indicates to the slave-state machine that the local board resources are available. When this signal is asserted and an external request is pending, the slave-state machine issues the proper enable signals (AEN and DEN). These enable signals remain active until SGNTA is unasserted.
SIACK	57	Slave interim acknowledge. This active-low signal indicates to the slave-state machine that an interim acknowledge (required for block transfers) should be issued on the NuBus™. The controller responds by asserting TM0 during block transfers.

Terminal Functions (continued)

NUBUS™ CARD-SLOT SIGNALS

PIN NAME	PIN NO.	DESCRIPTION
$\overline{ACK}$	21	Transfer acknowledge. This bidirectional I/O pin signals the end of a transaction. It also signals attention cycles.
$\overline{ARB0}$ $\overline{ARB1}$ $\overline{ARB2}$ $\overline{ARB3}$	11 13 15 17	Arbitration signals. These four I/O lines are bused and binary encoded in the same manner as the $\overline{ID3}$–$\overline{ID0}$ lines. During an arbitration contest, contending modules compare these lines with the binary value of their own $\overline{ID3}$–$\overline{ID0}$ lines. Each module drives the $\overline{ARB3}$–$\overline{ARB0}$ lines according to the rules of the distributed arbitration logic. The net effect of the arbitration contest is that the $\overline{ARB3}$–$\overline{ARB0}$ lines carry the binary-encoded number of the next NuBusT™ owner.
$\overline{CLK}$	26	Clock. The NuBus™ Clock signal is tied directly to the controller. Bus arbitration and data transfers are synchronized to this signal.
$\overline{ID0}$ $\overline{ID1}$ $\overline{ID2}$ $\overline{ID3}$	30 29 28 27	Card-slot identification. These four input lines are not bused but are binary encoded at each card-slot position to specify the module's position on the backplane. The controller uses these inputs when requesting access to the NuBus™.
NMRQ	25	NonMaster request. This asynchronous output on the 'ACT2440 is controlled by the NMRQ input on the 'ACT2440 and can be used in applications where the local board is not capable becoming a bus master but wishes to issue an interrupt. In systems that use the $\overline{NMRQ}$ line as a bused signal (all $\overline{NMRQ}$ signals tied common), the $\overline{NMRQ}$ output on the 'ACT2440 must first be buffered through an open-collector driver. In systems that use the $\overline{NMRQ}$ signal as an individual interrupt line, the $\overline{NMRQ}$ output on the 'ACT2440 does not have to be buffered with an open-collector driver.
$\overline{RESET}$	10	Reset. This asynchronous input monitors the NuBus™ $\overline{RESET}$ line. When taken active (low), it intializes the NuBus™ controller.
$\overline{RQST}$	23	Bus request. This bidirectional I/O pin is asserted by the controller when the local board wants ownership of the bus.
$\overline{SPV}$	6	System parity valid. System parity valid signals as the NuBus™ when parity has been generated for the $\overline{AD31}$–$\overline{AD0}$ lines.The controller drives this line inactive during master and slave cycles to indicate that no parity has been generated.
$\overline{START}$	20	Start. This bidirectional I/O pin is asserted at the start of a NuBus™ transaction and also initiates an arbitration contest. When asserted in conjuction with the $\overline{ACK}$ line, it denotes special nontransaction cycles called attention cycles.
$\overline{TM0}$ $\overline{TM1}$	7 8	Transfer mode. At the beginning of a transaction, these two lines indicate the type of transaction being initiated. Later in the transaction, the responding module uses them to indicate success or failure of the requested transaction.

BYTE DECODE SIGNALS

PIN NAME	PIN NO.	DESCRIPTION
A0 A1	59 60	Inverted NuBus™ address inputs. These two controller inputs require inverted versions of the NuBus™ Address signals $\overline{AD0}$ and $\overline{AD1}$ (as provided from the 'BCT2420 data/address interface device.) These signals, in conjuction with the NuBus™ transfer-mode signals ($\overline{TM0}$,$\overline{TM1}$), define the type of transfer cycle (i.e., byte, halfword, or block).
$\overline{BT0}$ $\overline{BT1}$ $\overline{BT2}$ $\overline{BT3}$	61 62 63 64	Byte control outputs. These active-low outputs are decoded from the A0, A1, and $\overline{TM0}$ controller inputs. The NuBus™ signal $\overline{TM1}$ defines whether the current cycle is a read or write. Refer to Table 1, for additional details

Terminal Functions (continued)

NUBUS™ STATUS SIGNALS

PIN NAME	PIN NO.	DESCRIPTION
MDONE	46	Master done. This active-high output signal is asserted when the local board is the NuBus™ master and the responding slave acknowledge (ACK) has been received. Once asserted, it remains asserted until MHOLD is unasserted.
NACK	32	NuBus™ acknowledge. This output is an inverted buffer version of the acknowledge signal (ACK).
NCLK	39	Inverted NuBus™ clock. This output signal is an inverted buffered version of the NuBus™ clock signal (CLK).
NCLK	40	Buffered Nubus clock. This output signal is a buffered version of the NuBus™ clock signal (CLK).
NLOCK	45	NuBus™ locked. This active-high output signal indicates to the local board that another master has generated an attention lock cycle and the local board is the requested slave. This output is asserted one clock after the NuBus™ start cycle on the sample edge (high-low) of the NuBus™ clock signal (CLK). NLOCK is active only during slave cycles. NLOCK is not active during master cycles.
NLRST	33	NuBus™ latched reset. This active-low output is a sychronized (2-level) version of the asynchronous NuBus™ reset signal (RESET).
NLTM0 NLTN1	38 37	NuBus™ latched transfered mode. These status signals are latched inverted versions of the NuBus™ TMx signals. They are doubled-latched to allow the local board to continue using TMx information. During NuBus™ master cycles, the transfer code is latched on the sample edge of the start cycle. The transfer code remains latched until a slave responds with an acknowledge cycle. The transfer status is latched on the sample edge of the acknowledge cycle. The transfer status remains latched as long as MHOLD is held active (low). After MHOLD returns inactive, the transfer status remains latched until the next NuBus™ start cycle. During slave cycles, the transfer code is latched on the sample edge of the cycle. The transfer code remains latched as long as SGNTA is held active (low). After SGNTA returns inactive, the transfer code remains latched until the next NuBus™ start cycle.
NMSTR	44	NuBus™ master. This active-high output indicates to the local voaed that the local board has won arbitration and is now the NuBus™ master. It is on the sample edge (high-to-low) of the NuBus™ clock signal (CLK) after winning arbitration. NMSTR remains asserted until the board loses mastership.
NTM1 NTM1	36 35	NuBus™ buffered transfer mode. These outputs are inverted buffered versions of the NuBus™ TMx lines (TM0, TM1).
SEREQ	41	Slave external request. This active-low output indicates that the local board is being requested on the NuBus™. The local board responds by driving slave grant access (SGNTA) active (low) when it is ready to service the request. In higher performance slave-only applications, SGNTA may be low going into the NuBus™ cycle.
NSTART	31	NuBus™ start. This output is an inverted buffered version of the NuBus™ start signal (START).

Table 1. Byte Decode Function Table

TM0	A1	A0	BT0	BT1	BT2	BT3	TYPE OF CYCLE
L	L	L	L	H	H	H	Byte 0
L	L	H	H	L	H	H	Byte 1
L	H	L	H	H	L	H	Byte 2
L	H	H	H	H	H	L	Byte 3
H	L	L	L	L	L	L	Full Word
H	L	H	L	L	H	H	1/2 Word 0
H	H	L	L	L	L	L	Block
H	H	H	H	H	L	L	1/2 Word 1

NOTE: TM1 = L indicates a write cycle. TM1 = H indicates a read cycle.

cycle descriptions

master read cycles

When the local board wants to read data from another board connected to the NuBus™, it first must win mastership of the bus. The timing diagram in Figure 2 shows the simplest form of operation for a typical master read cycle with master ready (MRDY) and master hold tied common with NREQ. The process begins when the local board takes NuBus™ Request (NREQ) active (low) which causes the local board to begin arbitrating for the bus by forcing RQST low.

On the first sample edge after NREQ is taken active (low), the local transfer-mode input lines (LOCTMx) are latched into the controller. Depending on the number of other masters competing for the bus, the requesting process can take a few clock cycles. Under the rules of fair arbitration, each requesting master is guaranteed to win ownership of the bus before a previous winner is allowed to re-arbitrate for the bus.

When the local board wins control of the bus, the controller signals the local board by taking NuBus™ master (NMSTR) active (high). The controller immediately issues a start cycle (if MRDY is active) on the next driving edge by taking START low and placing the read address on the bus.

The accessed slave responds to the read request by placing the read data on the bus and driving NuBus™ acknowledge (ACK) low. The controller signals the local board that the transfer is complete by driving master done (MDONE) active (high). The local board responds to the MDONE signal by driving NREQ, MRDY, and MHOLD inactive (high) when it finishes using the read data. If no other masters are requesting the NuBus™, the controller parks on the bus, which is indicated by NMSTR remaining high (see Figure 2). The local board can issue another start cycle by simply taking NREQ low; it does not have to perform arbitration when the controller is parked on the bus. The controller remains parked on the bus until another master begins arbitrating for the bus. Refer to the section on NuBus™ cycles from the parked position for additional details.

master write cycles

When the local board wants to write data to another board connected to the NuBus™, it first must win mastership of the bus. Figure 3 shows the timing diagram of a typical master write cycle. The local board follows the same arbitration process as described in the master read cycle.

When the local board wins mastership of the bus, the controller signals the local board by driving NMSTR high. The controller immediately issues a start cycle (if MRDY) is active) on the next driving edge by taking START low and placing the write address on the bus. At the end of the start cycle, the controller places the write data on the bus. The addressed slave responds to the write request by driving ACK low.

The controller signals the local board that the transfer is complete by driving master done (MDONE) active (high). The cycle is completed on the local board after NREQ, MRDY, and MHOLD return inactive. The same rules apply for parking on the bus as described in the master read cycle.

high-speed master read/write cycles

Figure 4 demonstrates a high-speed master read or master write cycle. The major difference between these cycles and the ones previously described is that MHOLD does not hold the controller after one master cycle. This feature allows the local board to generate additional start cycles quickly. This capability assumes that no other master has won ownership of the bus and the next transfer cycle (read or write) has not changed. If the transfer cycle has changed, the new transfer code must be latched into the ’ACT2440 by taking NREQ high for one clock cycle immediately after MDONE has been received.

If NREQ or MRDY are taken inactive (high) before the first sample clock edge after MDONE has been received, a new start cycle is not automatically generated. Likewise, if MHOLD is taken active (low) before the first sample clock edge after ACK has been received, a new start cycle is not automatically generated. The simplest form of interface ties MHOLD and MRDY in common with NREQ, which guarantees that only one transfer cycle is generated every NREQ cycle. However, higher performance is achievable by using the above method.

When MHOLD is tied in common with NREQ and MRDY, only one master cycle is generated. To generate another cycle, NREQ, MRDY, and MHOLD must be regenerated, which takes additional clock cycles. In the high-speed mode, the next start cycle is automatically generated. The advantage of this mode is that it produces faster read/write cycles. The disadvantage is that it shortens the time allowed for the local board to respond to read data and prepare for the next cycle.

master lock cycles

The ’ACT2440 is designed to support resource locking on the NuBus™. If the master lock request input (MLREQ) is taken active (low) when the NuBus™ request input (NREQ) is sampled, the controller issues an attention lock cycle after winning arbitration. An attention lock cycle warns all other modules connected to the bus that their local resources should be locked for the following transactions. The end of the locked sequence is signaled by an attention null cycle. The timing diagram in Figure 5 illustrates a typical locked sequence.

After the attention lock cycle is issued, normal NuBus™ master cycles can be performed. If the transfer type must be changed during a locked sequence, the new transfer code must be latched into the ’ACT2440 by taking NREQ high for one clock cycle, with MLREQ held low. The MLREQ input remains asserted for the entire lock tenure. The RQST output remains low for the entire lock cycle. When MLREQ is unasserted, the controller issues an attention null cycle. If no other masters are arbitrating for the bus, the controller parks on the NuBus™.

local resource conflict timing

In applications where the local circuitry can be both a master and a slave, conflicts for local resources may develop. For example, if the local circuitry starts the arbitration process as a master and loses to another master that in turn accesses the local circuit’s slave resources, then the local circuitry must respond to the NuBus™ as a slave and immediately be ready to accomplish a master cycle.

The master ready input (MRDY) provides a throttle mechanism to handle such situations. If this signal is inactive (high) when the master-state machine wins arbitration, the master-state machine freezes in the current state, maintaining all arbitration signals until MRDY is asserted low. The timing diagram in Figure 6 shows a situation where the local board has started arbitration as a master but loses to another master that is attempting to read or write data from the local resource.

The slave external request status output (SEREQ) signals the local board that another master is accessing the local board. When the local board is ready to respond, it drives slave grant access (SGNTA) active (low), which enables data and/or address information to be placed onto the local board. When the local board is ready to respond, the local acknowledge input (LACK) is driven active (low). This action causes the controller to issue an acknowledge cycle on the next driving clock edge. For additional details, refer to the section covering typical slave cycles.

When the local board finally wins the arbitration process, the NuBus™ master status signal (NMSTR) goes active (high). The local board responds by taking master ready (MRDY) low, which causes the controller to execute a normal master read or master write cycle. In applications where the local board is only a master, MRDY can be tied in common with NREQ for simpler operation.

master timeout cycle

When master ready (MRDY) is used to throttle the controller, a 16-state counter sets a maximum length of time that the controller will stay in the frozen state after winning arbitration. With NREQ low and MRDY high, this counter is enabled when the arbitration contest is won. When this timer reaches its maximum count (16), it forces the controller to issue a NuBus™ attention null cycle, which in turn signals all other masters on the bus to re-initiate arbitration. Figure 7 shows the timing diagram for the master timeout cycle.

On rare occasions, the local circuitry may give up on a NuBus™ request while still in the arbitration process. The controller detects this situation and issues a NuBus™ attention null cycle once it has won arbitration.

slave read/write cycles

The 'ACT2440 provides all the handshake signals required to facilitate a simple NuBus™ slave interface. In slave applications, the local board is either written to or read from. When a NuBus™ master wishes to access the local board as a slave, it places the slave's address on the bus during the start cycle. This action requires a compare function to identify when the NuBus™ address matches the 4-bit ID code associated with the local board. This function is provided in the 'BCT2420 or can be built using standard MSI comparator functions. The controller receives this input through the ID equal input (IDEQ).

Figure 8 shows the timing diagram of a typical slave read cycle. Figure 9 shows the timing diagram for a typical slave write cycle. The slave external request status output (SEREQ) signals that the local board is being accessed by another master. When the local board is ready to receive data and/or address information, it drives slave grant access (SGNTA) active (low). When the local board is ready to respond to a read or write request, it drives local acknowledge (LACK) low. The controller then issues an acknowledge on the bus, which completes the transaction. Data and/or address information is enabled onto the local board as long as SGNTA is held low. SEREQ does not go inactive until the first sample edge after SGNTA goes inactive. Data and/or address information is disabled on the first sample edge after SGNTA returns inactive (high).

All slave external requests must be responded to with a local acknowledge. Allowing the NuBus™ to timeout does not reset the slave state machine.

higher performance slave cycles

Slave grant access (SGNTA) and local acknowledge (LACK) control the duration of slave cycles on the 'ACT2440. The simplest implementation, as previously explained, uses SEREQ, SGNTA, and LACK to form a simple handshake. Faster slave cycles are possible by taking SGNTA low before the first sample edge after START as shown in Figure 10. This mode of operation enables address and data information onto the local board on the first sample edge after START. (Note: In slave-only applications, address information can be enabled onto the local board sooner by tying AEN low on the 'BCT2440s.) As previously described, LACK controls the completion of the slave cycle. Address and data information remains enabled onto the local board until SGNTA returns inactive.

If the local acknowledge (LACK) and slave grant access (SGNTA) inputs are taken low before the first sample edge after START, the acknowledge output (ACK) is generated on the next driving clock edge. This mode of operation offers the highest performance but places the greatest demand on local circuitry.

slave lock detection

NuBus™ locked (NLOCK) is a special output provided on the 'ACT2440 that signals when the local board is being accessed by another master and an attention lock cycle has occurred. NLOCK informs the local board not to modify any of its local resources until an attention null cycle is received. Figure 11 shows the timing diagram for a slave lock-detection cycle. As shown in Figure 11, NLOCK goes active (high) when an attention lock cycle occurs on the bus and the local board is being requested by another master. NLOCK will remain high until the attention null cycle is received.

master block-transfer cycles

NuBus™ 1987 master block transfers are supported by the 'ACT2440. Figure 12 shows the timing diagram for a typical master block read. Figure 13 shows the timing diagram for a typical master block write.

A master block transfer consists of a start cycle, multiple data cycles to or from sequential address locations, and an acknowledge cycle. The master controls the number of data words transferred and communicates this information to the slave during the start cycle via address lines AD5–AD2. Table 2 shows the input code for master block-transfer cycles.

During master block transfers, the slave acknowledges intermediate data cycles via the TM0 line. The 'ACT2440 detects these intermediate data cycles and generates the proper buffer control signals. The final data cycle from the responding slave is a standard acknowledge cycle.

Table 2. Master Block-Transfer Function Table

A5	A4	A3	A2	A1	A0	$\overline{LOCTM1}$	$\overline{LOCTM0}$	BLOCK SIZE	TYPE OF CYCLE
X	X	X	L	H	L	L	H	2	Write
X	X	L	H	H	L	L	H	4	Write
X	L	H	H	H	L	L	H	8	Write
L	H	H	H	H	L	L	H	16	Write
X	X	X	L	H	L	H	H	2	Read
X	X	L	H	H	L	H	H	4	Read
X	L	H	H	H	L	H	H	8	Read
L	H	H	H	H	L	H	H	16	Read

slave block-transfer cycles

The ’ACT2440 can support slave block-transfer cycles with the addition of the ’ALS2442. The first responsibility of a slave during block transfers is to determine the type and size of the block transfer. This information is provided by the requesting master and must be decoded from the TMx lines and the A5–A0 address lines (as provided by the ’ACT2420s). See Table 3 for additional details.

The slave interim acknowledge input ($\overline{SIACK}$) generates the interim acknowledge cycles via $\overline{TM0}$. The slave external request output ($\overline{SEREQ}$) signals the local board when an interim acknowledge has occurred on the bus.

Figure 14 shows the timing diagram of a typical slave block read. Figure 15 shows the timing diagram of a typical slave block write. The beginning of these cycles looks like any other slave cycle; $\overline{SEREQ}$ goes active (low), signaling the local board that another master is requesting the local board. On the first sample edge after $\overline{SGNTA}$ is taken active (low), the $\overline{AEN}$ buffer signal is driven low, enabling the NuBus™ addresses onto the local board. The A0, A1, and TMx lines must be decoded as provided on the ’ALS2442 in order to generate a block-transfer signal (represented on the timing diagrams as BLOCK). When this signal goes active (high), it signals the local board that a block transfer has been requested. Decoding A5-A2 determines the number of words to be transferred. The final acknowledge cycle is generated by driving $\overline{LACK}$ low.

Table 3. Slave Block-Transfer Decode Table

A5	A4	A3	A2	A1	A0	NTM1	NTM0	BLOCK SIZE	TYPE OF CYCLE
X	X	X	L	H	L	H	L	2	Write
X	X	L	H	H	L	H	L	4	Write
X	L	H	H	H	L	H	L	8	Write
L	H	H	H	H	L	H	L	16	Write
X	X	X	L	H	L	L	L	2	Read
X	X	L	H	H	L	L	L	4	Read
X	L	H	H	H	L	L	L	8	Read
L	H	H	H	H	L	L	L	16	Read

maximum block-transfer performance

As a master, the ’ACT2440 is capable of supporting the maximum block transfer rate of 37.6M-bytes/second (one start cycle followed by 16 consecutive 100-ns data cycles). Figure 12 shows a more typical situation where the slave controls the block transfer rate via the intermediate acknowledge signal (TM0). Note that the ’ACT2440 generates a data clock (DCLK) every clock cycle that TM0 is low. The final data cycle is a normal acknowledge cycle.

In slave block transfer mode, the ’ACT2440 has been designed to provide a simple handshake between the slave interim acknowledge (SIACK) input and the slave external request (SEREQ) output as shown in Figure 15. Note that each data clock (DCLK) cycle goes high for 100 ns as a result of the simple handshake between SIACK and SEREQ. In this simpler mode of operation, the maximum intermediate data transfer rate when using the ’ACT2441 is 200 ns, which equates to approximately 20M-bytes/second.

NuBus™ cycles from the parked position

As long as RQST remains unasserted, the bus owner is considered to be parked on the bus and may continue to use the bus without the necessity of going through an arbitration contest in which it is the only contender. The ANSI/IEEE 1196-1987 specification requires that as soon as another module drives the RQST line asserted, an arbitration contest is started and the present bus owner (currently parked on the bus) must not begin another transaction. The concept of bus parking reduces the average time needed to acquire the bus in systems with a small number of active contenders.

When using the ’ACT2440 NuBus™ controller from a parked position, the local board does not know if it remains the NuBus™ master and begins another transaction until the START signal has been generated. In other words, just because the local board has taken MRDY and NREQ active (low), does not mean the ’ACT2440 continues to own the bus and has generated a START cycle.

When the ’ACT2440 is in the parked position (NMSTR high) and no other masters are requesting the bus, a start cycle is generated on the driving edge after NREQ and MRDY are taken active (low).

Figure 16 shows a situation where an old NuBus™ master is initially parked on the bus and is attempting to issue another START cycle (by taking MRDY low); but loses to a new master who is attempting to access data from resources that are available on the old master’s board. In other words, the new master wins the bus and is trying to use the old master as a slave. This situation is similar to the local resource conflict timing diagram shown in Figure 6.

In Figure 16, the old master learns that it has lost the bus by detecting that NMSTR has gone inactive (low) during the start cycle. The new master, which has just won the bus and has generated a start cycle, is attempting to access data from the old master. The slave external request (SEREQ) output on the old master detects this access request by going active (low) on the first sample edge after the start cycle. At this time, the old master may want to take MRDY back to the inactive level (as shown in Figure 16) so that it has control of the START signal after winning back the bus. If MRDY is not taken back to the inactive level (high) after losing the bus, then the ’ACT2440 immediately issues a start cycle after the acknowledge cycle has been generated.

If the new master was directing the access cycle at a different slave, then the SEREQ output on the old master would remain inactive (high) and the MRDY input on the old master can be kept low in order to generate a start cycle as soon as the old master wins back the bus.

Notice from the timing diagram that if the old master takes MRDY low at the same time or in the following cycle, then the old master loses to the new master.

If the old master takes MRDY low on the cycle before the new master takes RQST low, then the old master retains the bus and completes its cycle.

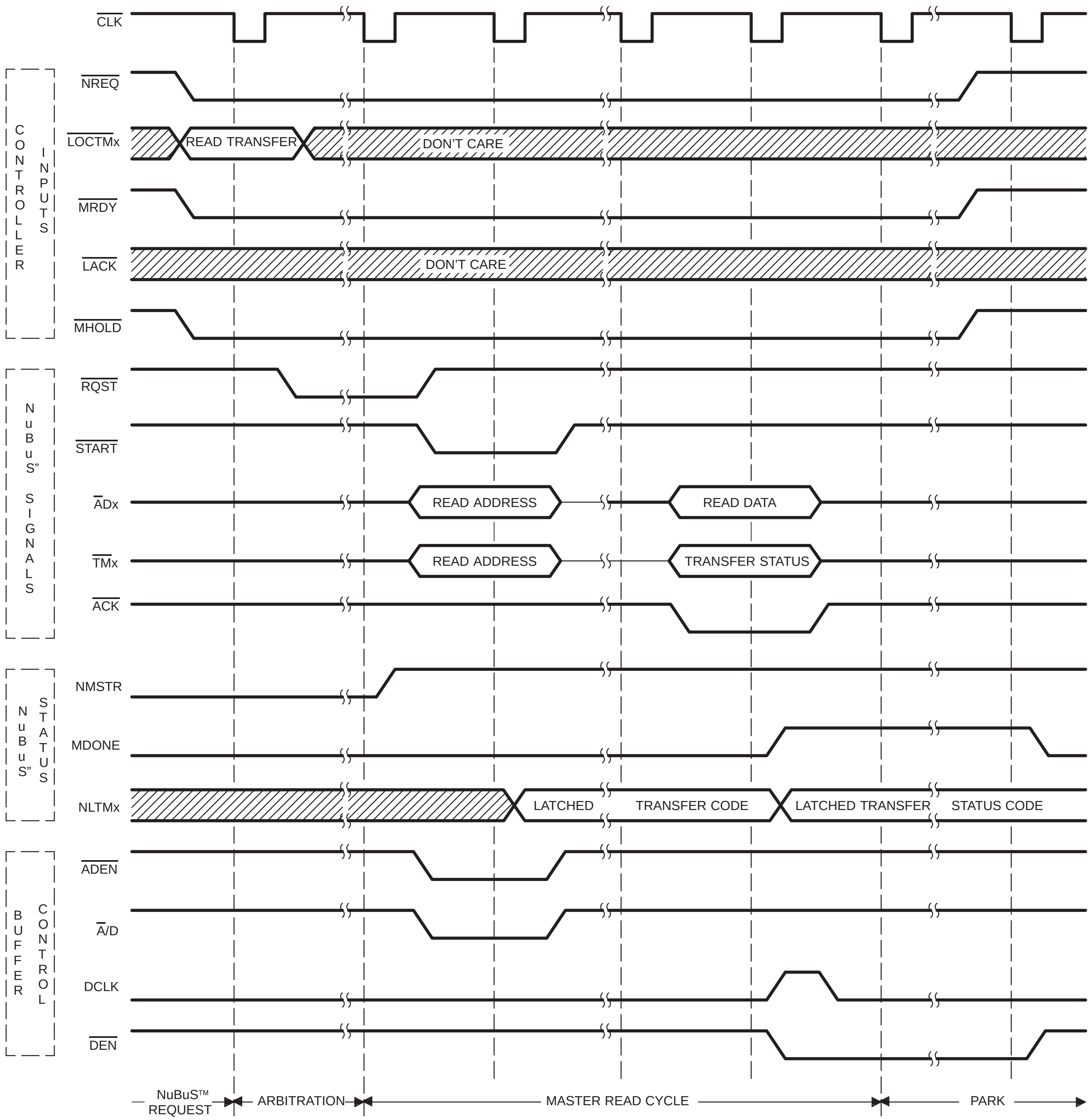

Figure 2. Typical Master Read Cycle

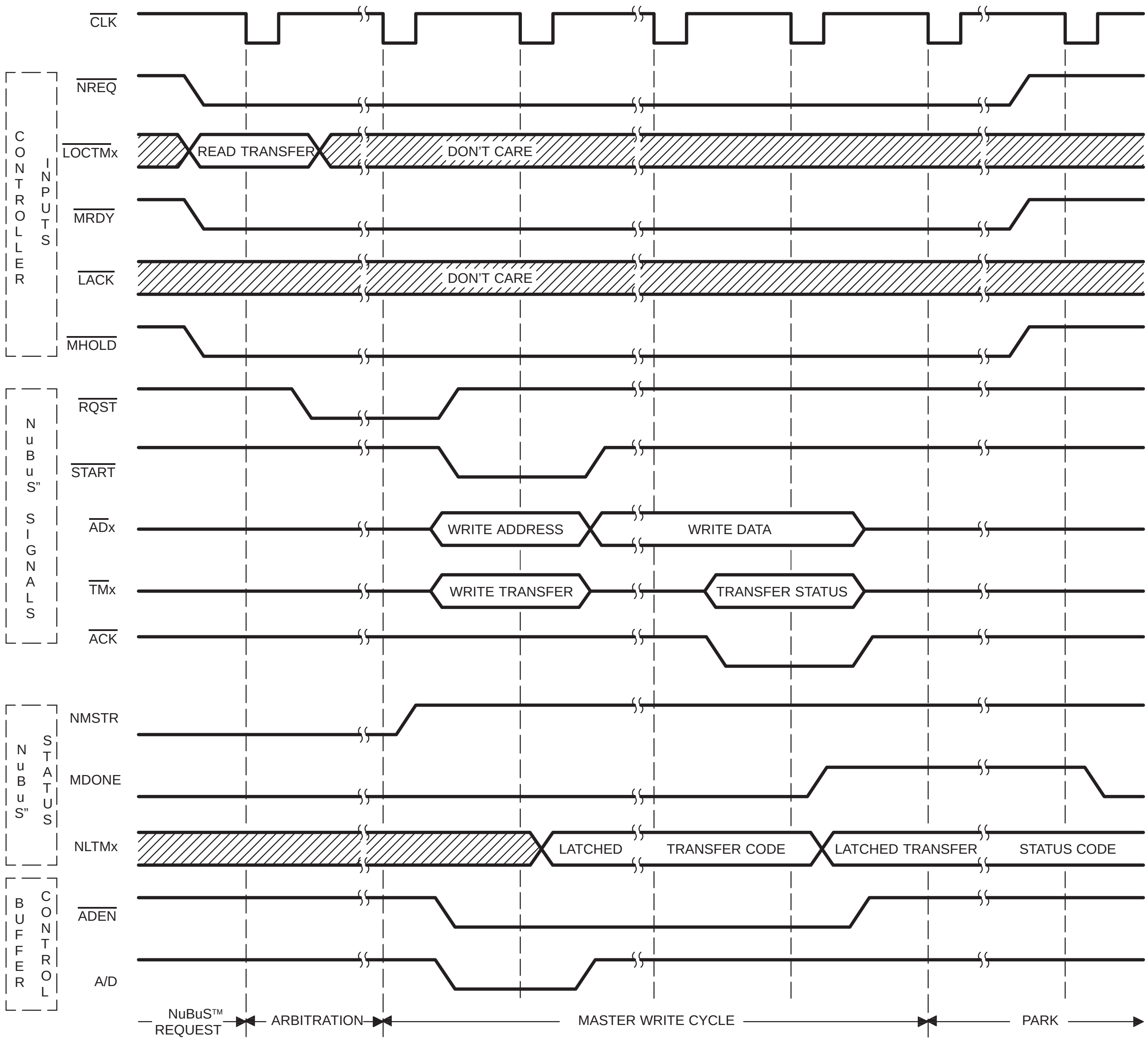

Figure 3. Typical Master Write Cycle

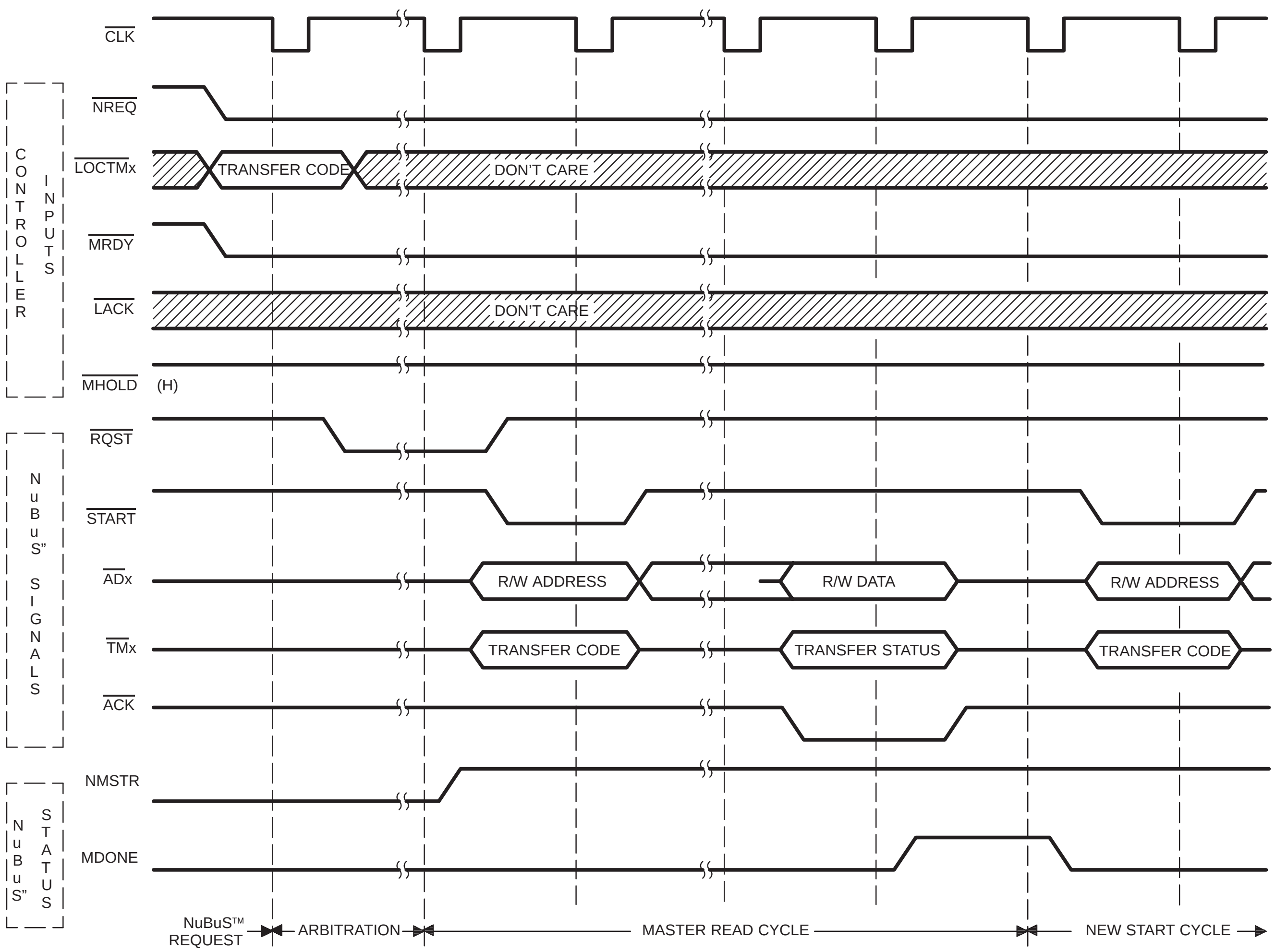

Figure 4. High-Speed Master Read/Write Cycles (MHOLD Logic Not Used)

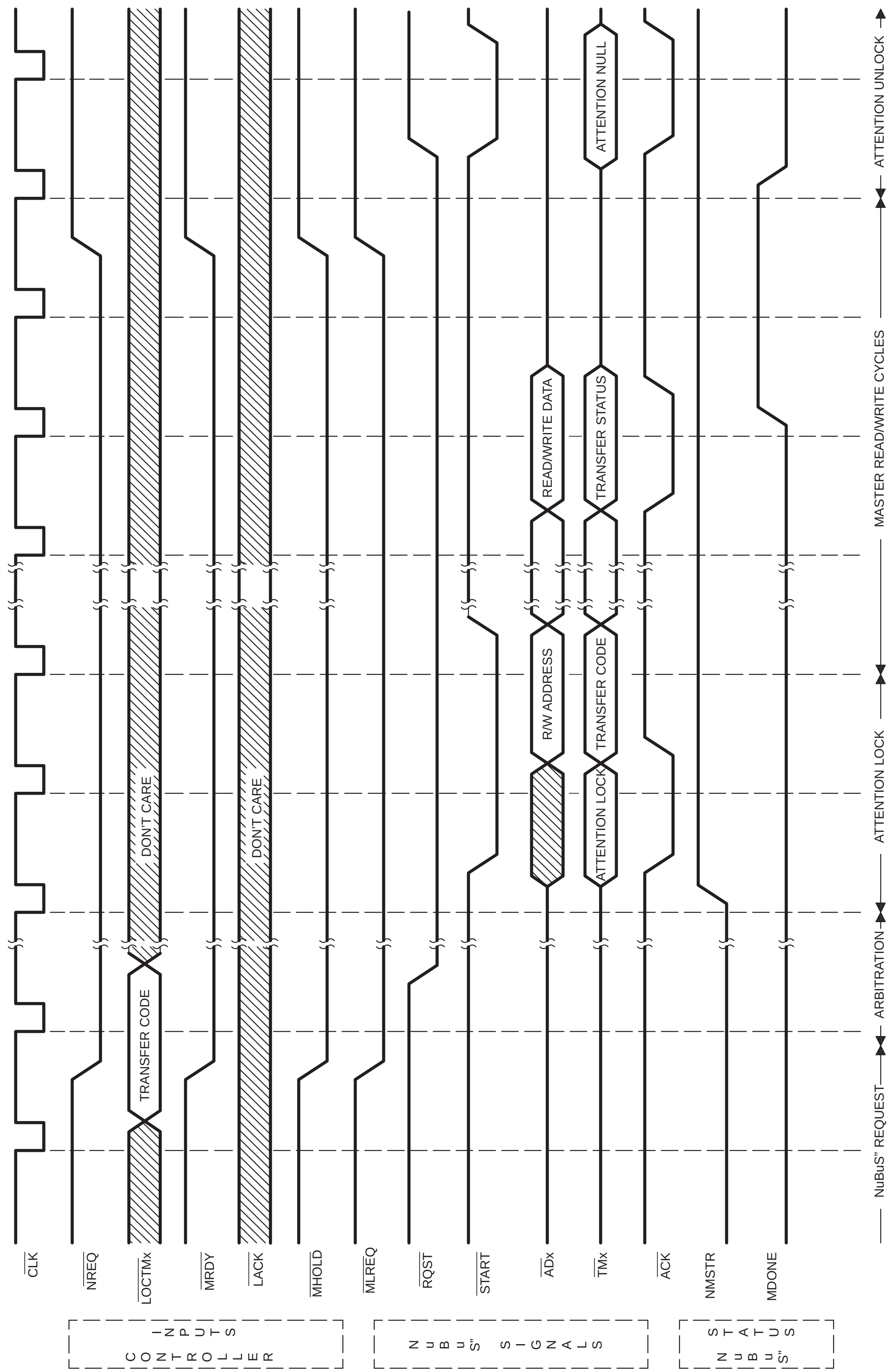

Figure 5. Master Lock Cycle

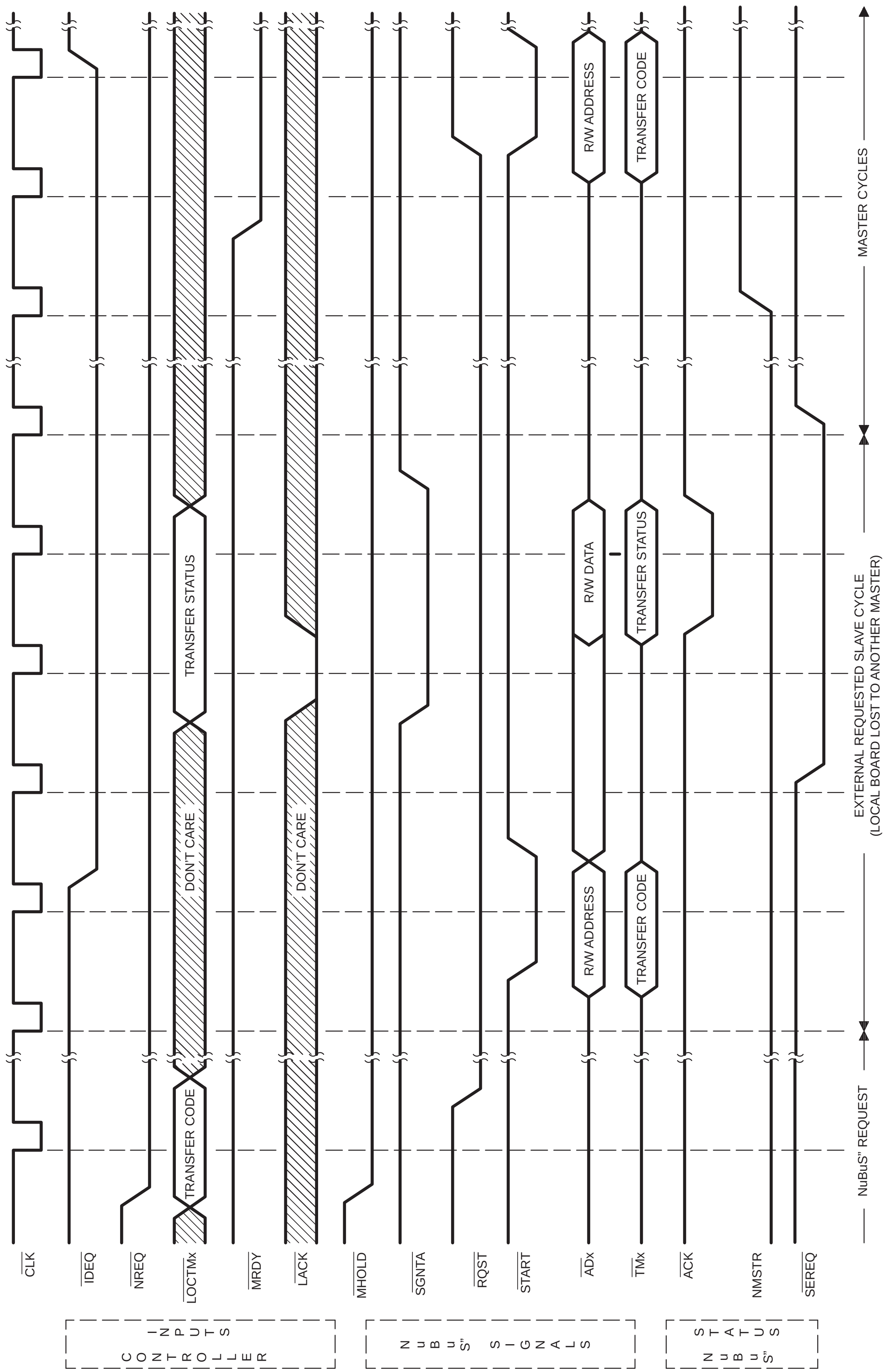

Figure 6. Local Resource Conflict Timing

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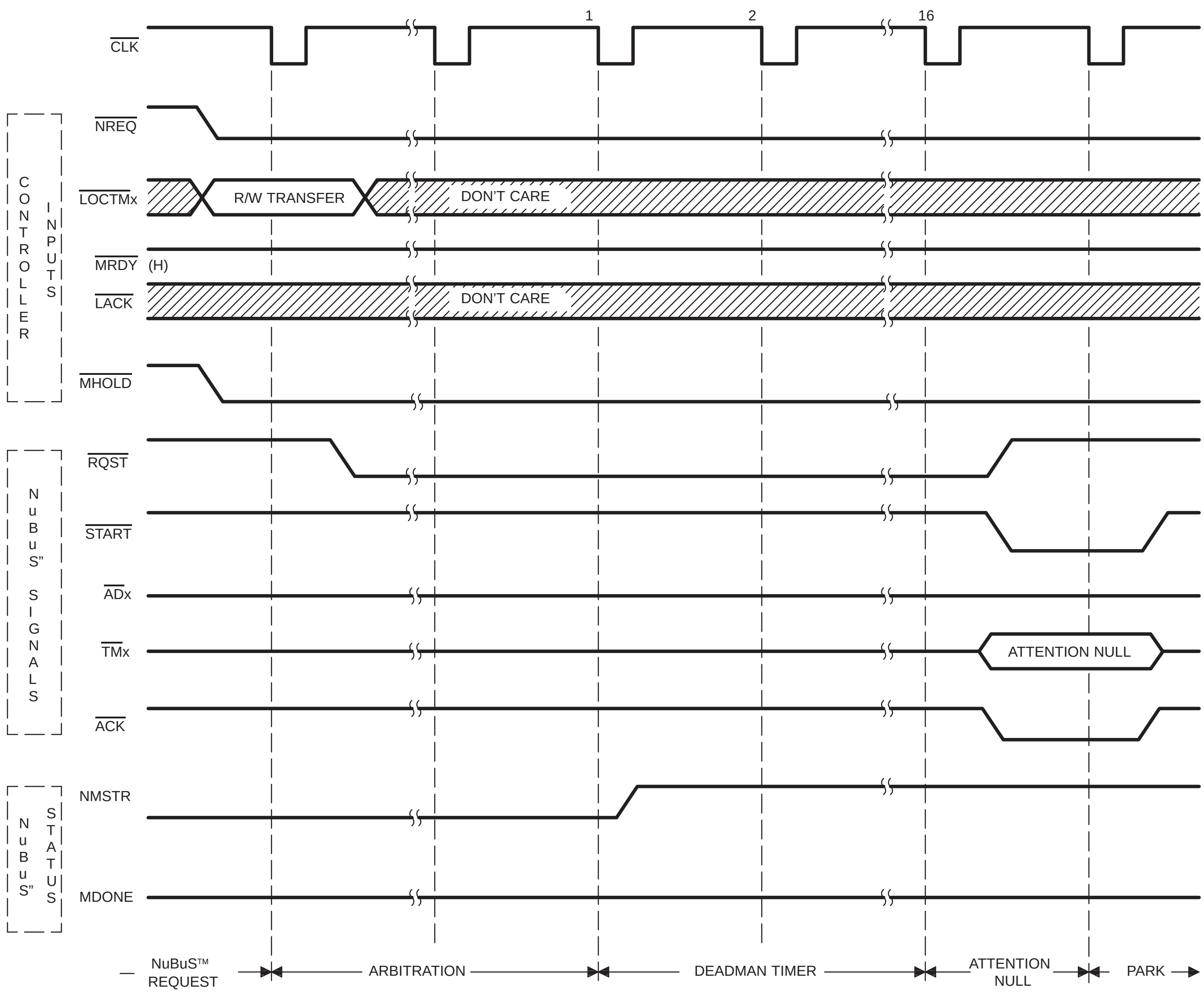


Figure 7. Master Timeout Cycle

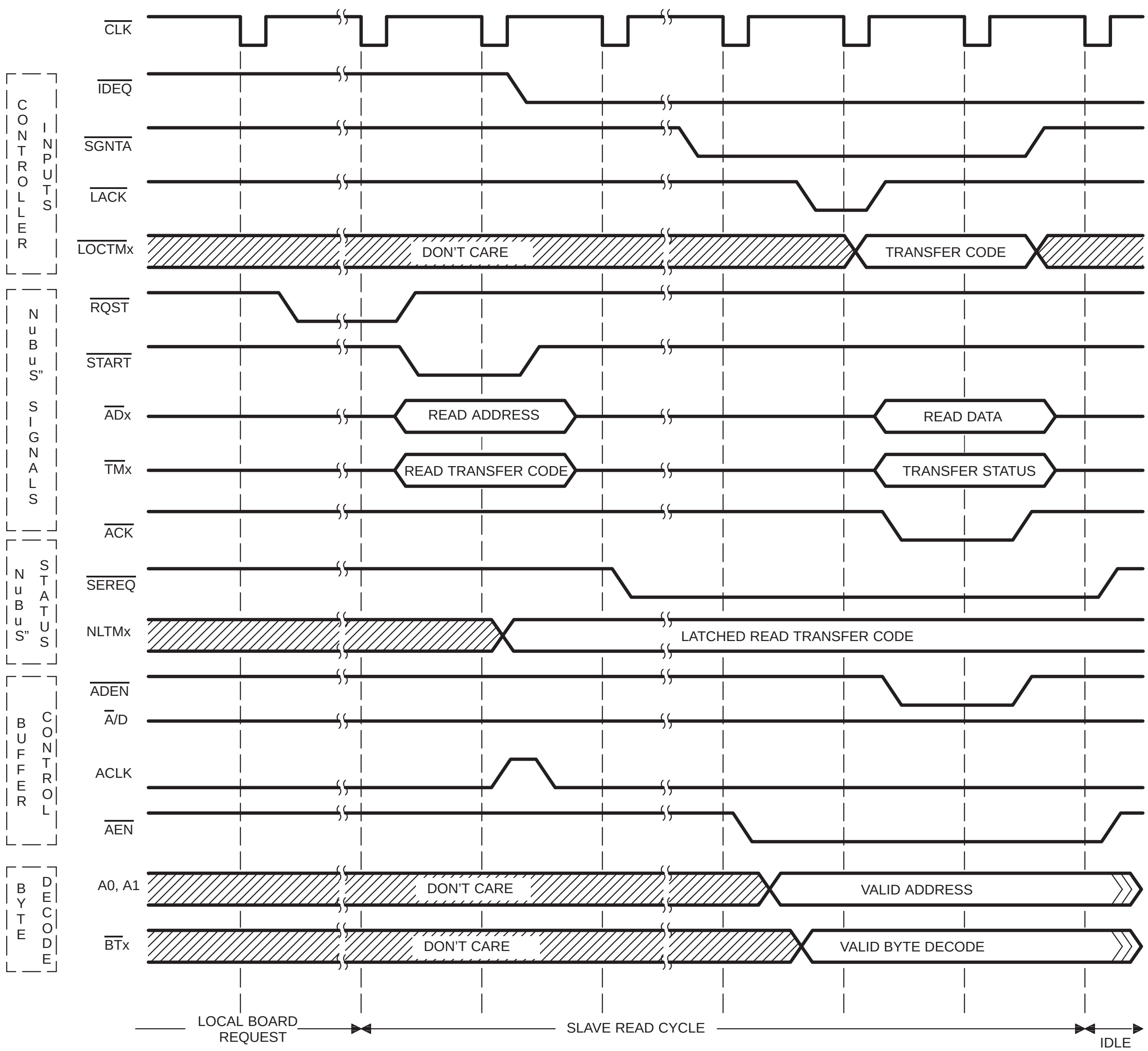


Figure 8. Typical Slave Read Cycle

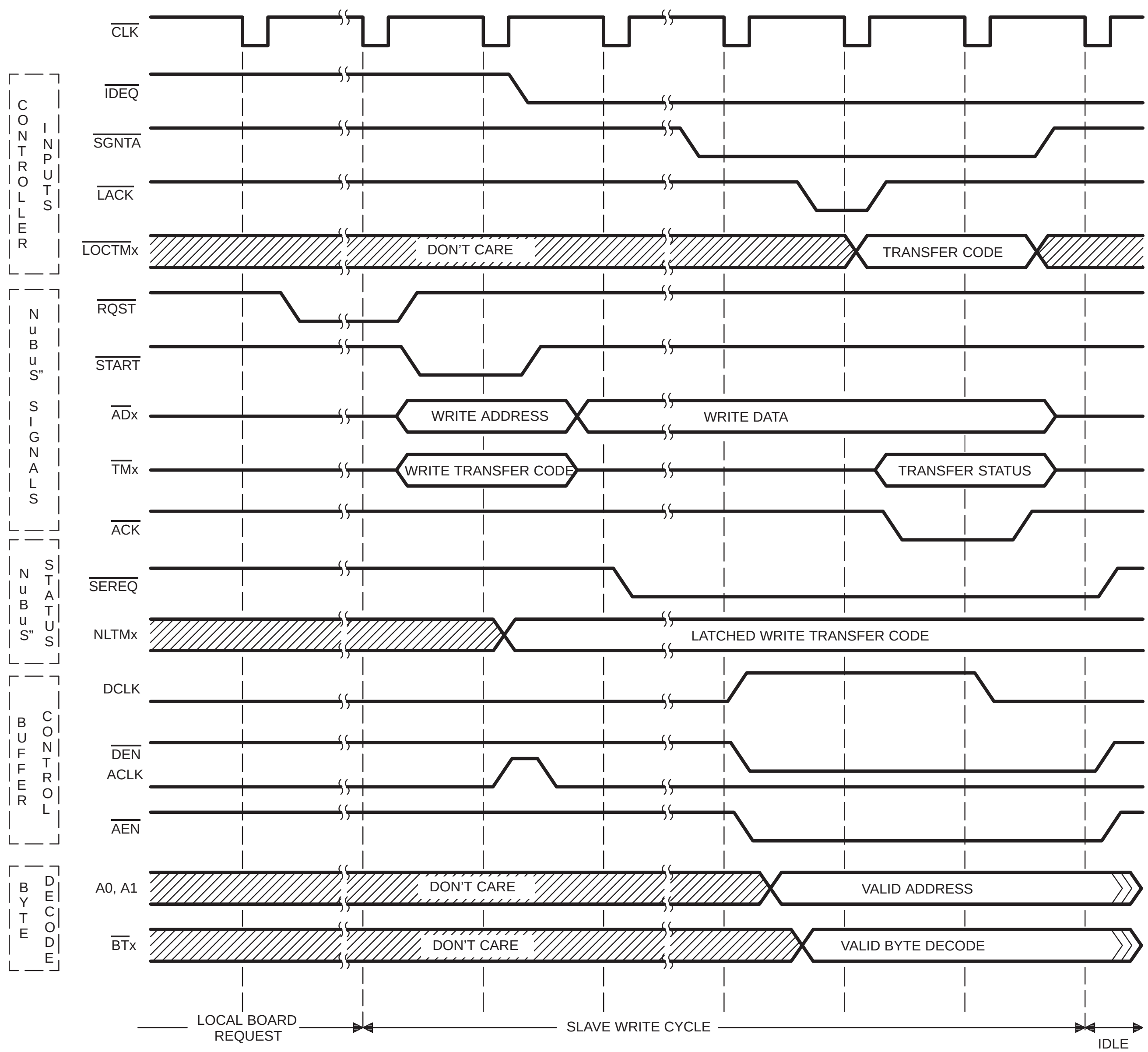


Figure 9. Typical Slave Write Cycle

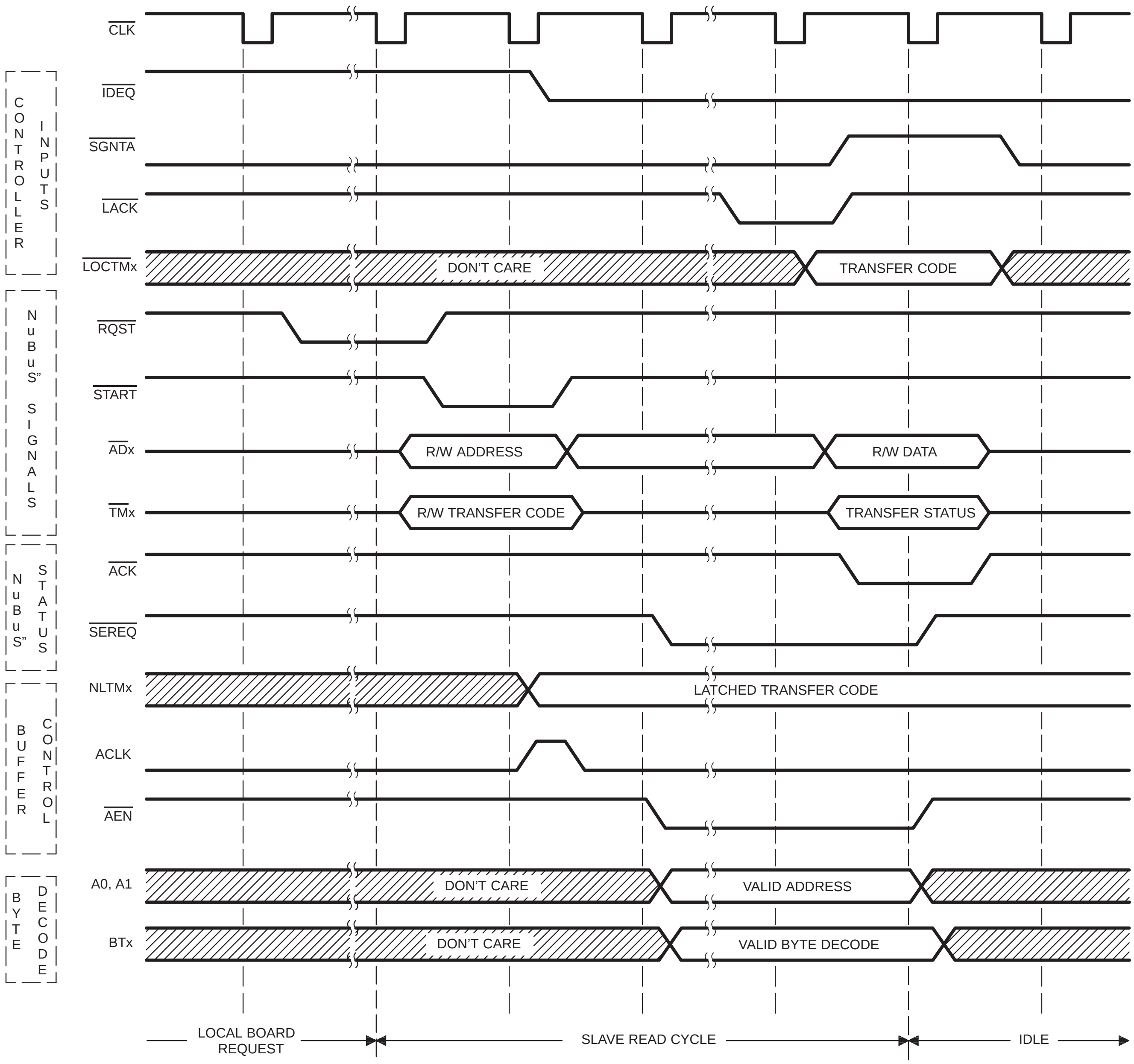


Figure 10. Higher-Performance Slave Cycles

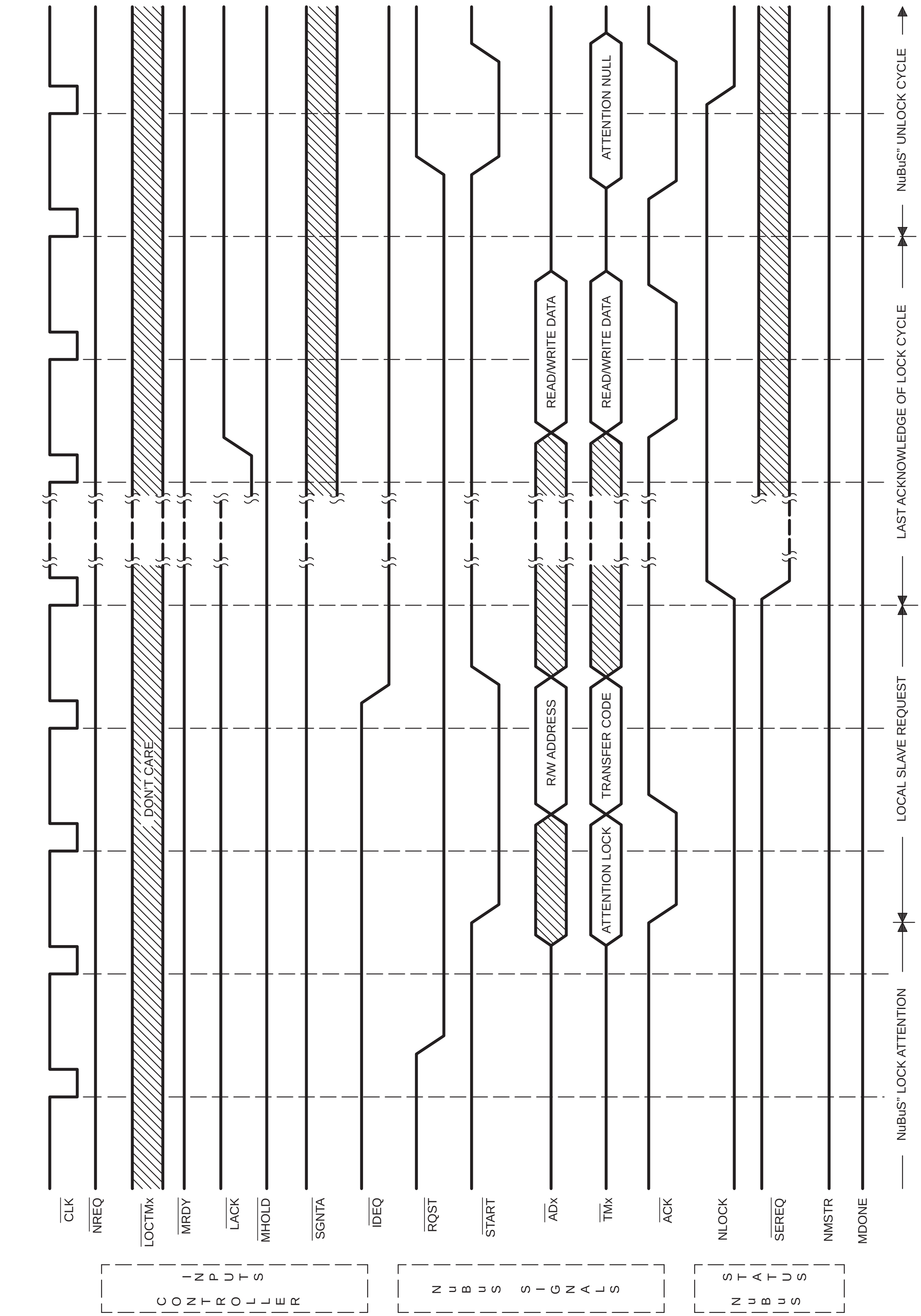


Figure 11. Slave Lock-Detection Cycle

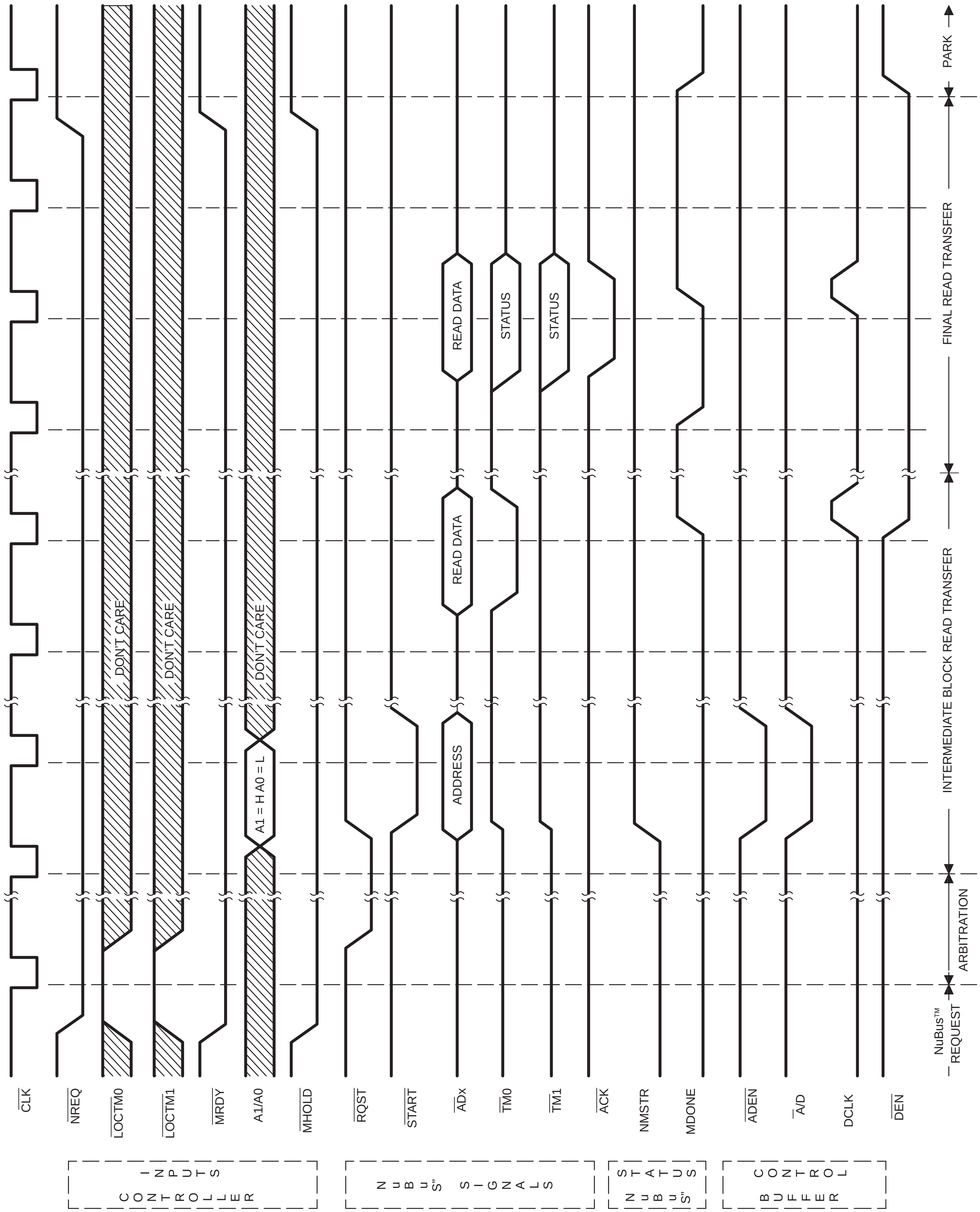


Figure 12. Master Block-Read Transfer Cycle

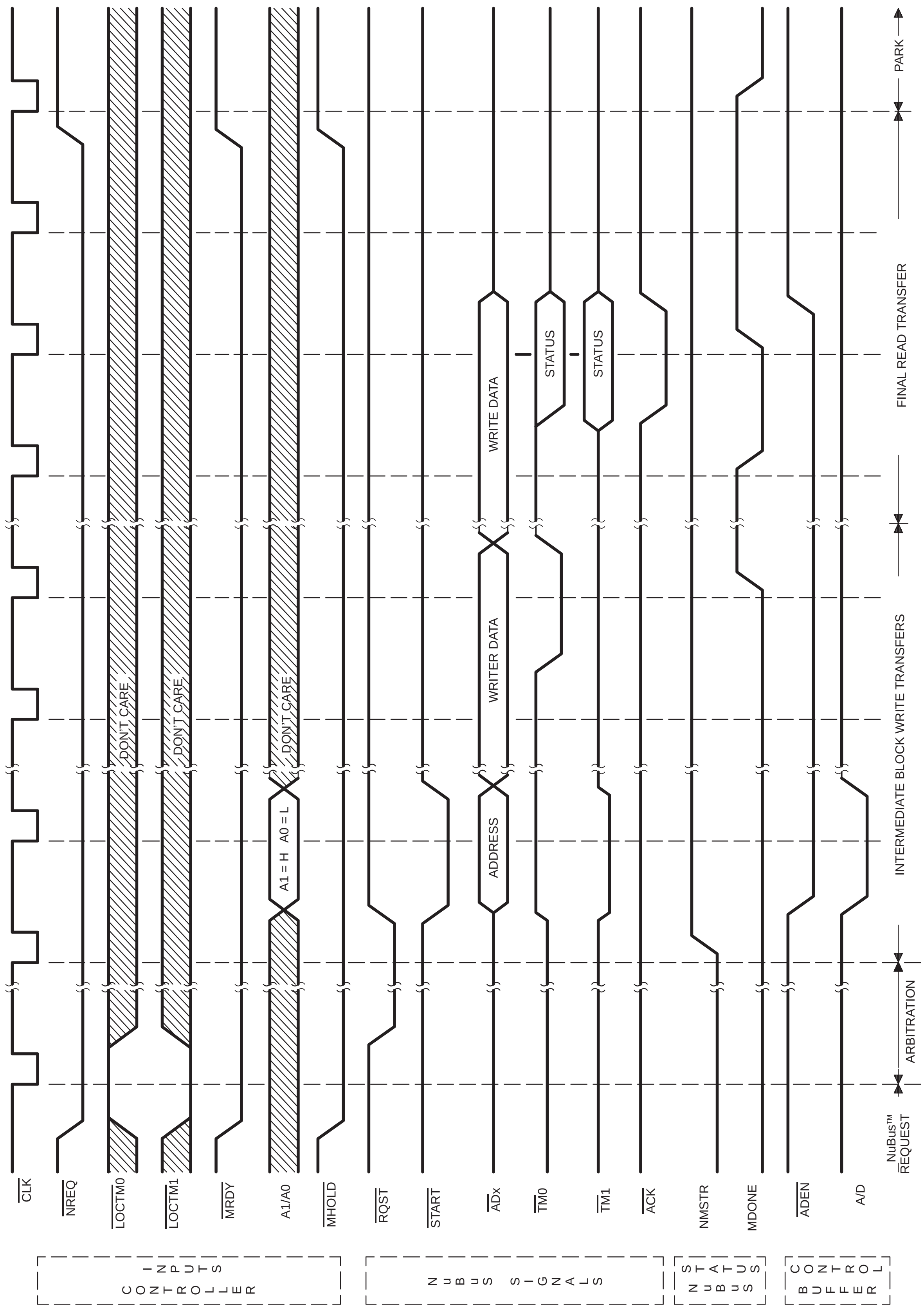
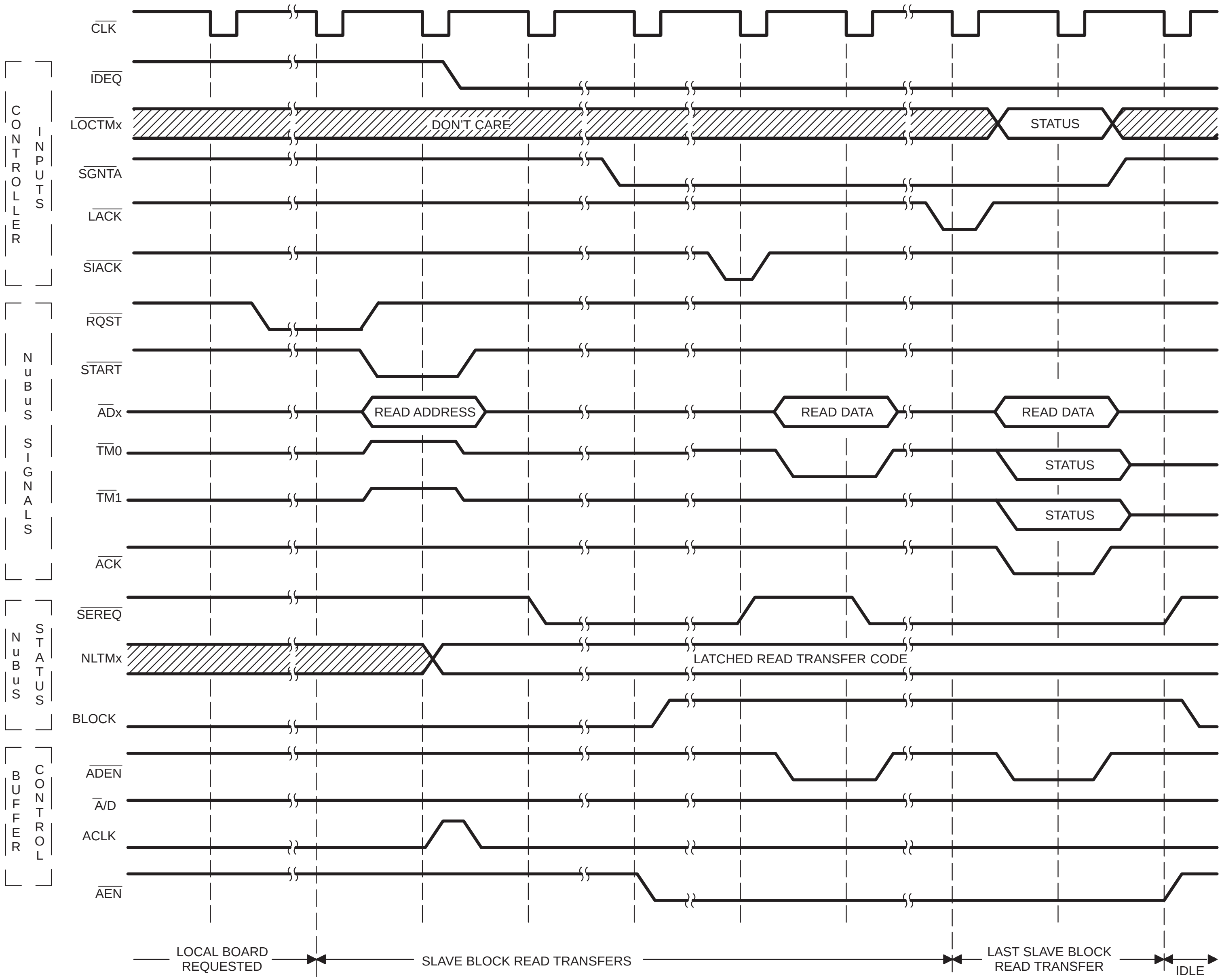
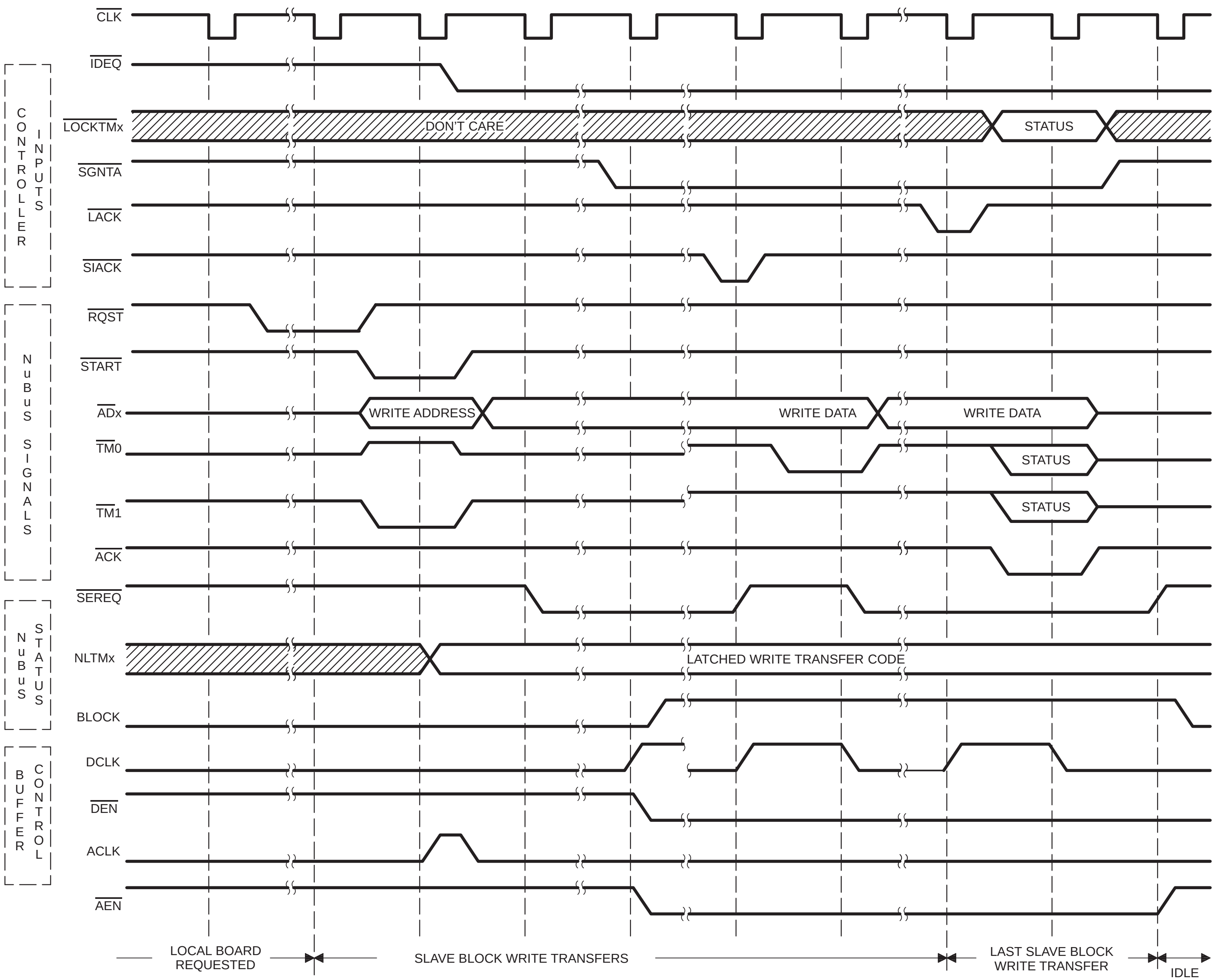


Figure 13. Master Block-Write Cycle



† The BLOCK signal must be supplied by external logic, such as from TI's SN74ALS2442.

Figure 14. Slave Block-Read Transfer Cycle



† The BLOCK signal must be supplied by external logic, such as from TI's SN74ALS2442.

Figure 15. Slave Block-Write Transfer Cycle

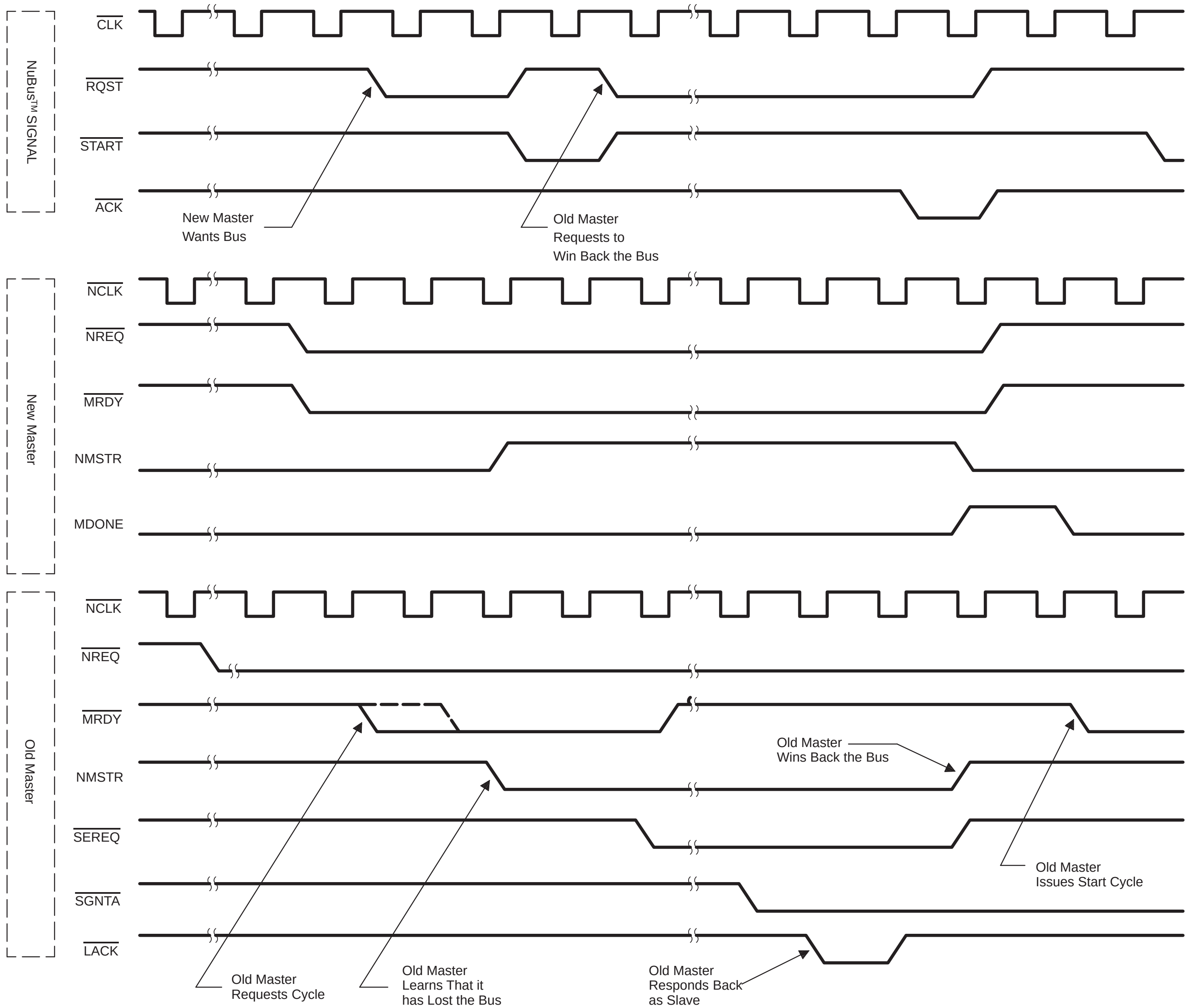


Figure 16. NuBus™ Cycles From the Parked Position

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 7 V
Input voltage range, any input	–0.5 V to 7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Status, buffer, and byte decode			–2	mA
		NuBus™ 3-state outputs			–1.6	
I_{OL}	Low-level output current	Status, buffer, and byte decode			6	mA
		NuBus™ 3-state outputs			24	
		NuBus™ open-collector outputs			80	
f_{clock}	Clock frequency		0		10	MHz
t_w	Pulse duration	$\overline{CLK}$ low	23			ns
		$\overline{CLK}$ high	73			
t_{su}	Setup time before $\overline{CLK}$↓	$\overline{NREQ}$	15			ns
		$\overline{LOCTMx}$ valid	15			
		$\overline{LACK}$	15			
		$\overline{MLREQ}$ and $\overline{NREQ}$ low	15			
		$\overline{MRDY}$ low	15			
		$\overline{SGNTA}$ low	15			
		$\overline{IDEQ}$ low	15			
		$\overline{SIACK}$ low	15			
t_h	Hold time after $\overline{CLK}$↓	$\overline{NREQ}$ low	10			ns
		$\overline{LOCTMx}$ valid	10			
		$\overline{SIACK}$ low	10			
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	Status, buffer, and byte decode	I_{OH} = 2 mA,	V_{CC} = 4.5 V	3	3.7		V
		NuuBus™ 3-state outputs	I_{OH} = 1.6 mA,	V_{CC} = 4.5 V	3	3.7		
V_{OL}	Low-level output voltage	Status, buffer, and byte decode	I_{OL} = 6 mA,	V_{CC} = 4.5 V		0.3	0.4	V
		NuuBus™ 3-state outputs	I_{OL} = 24 mA,	V_{CC} = 4.5 V		0.35	0.5	
		NuuBus™ open drain	I_{OL} = 80 mA,	V_{CC} = 4.5 V		0.35	0.5	
I_{OZH}	High-impedance state output current		V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}	High-impedance state output current		V_{CC} = 5.5 V,	V_O = 0.4 V			20	µA
I_{IH}	High-level input current		V_{CC} = 5.5 V,	V_I = 5.5 V			20	µA
I_{IL}	Low-level input current	ID0–ID3	V_{CC} = 5.5 V,	V_I = 0			–750	µA
		All other inputs					–10	
I_{OS}	Short-circuit output current‡		V_O = 0,	V_{CC} = 5.5 V	–15		–225	mA
I_1	Active supply current		V_{CC} = 5.5 V, f_{clock} = 10 MHz	All inputs active,		6	15	mA
I_2	Average standby current		V_{CC} = 5.5 V, All inputs at V_{IL} or V_{IH}, f_{clock} = 10 MHz			2	5	mA
C_i	Input capacitance		V_I = 0 V,	f = 1 0 MHz		5		pF
C_o	Output capacitance		V_O = 0 V,	f = 1 MHz		10		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ No more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
f_{max}	Clock frequency, $\overline{CLK}$	10			MHz

NuBus™ card-slot signals, C_L = 300 pF†

PARAMETER		LOAD	MIN	TYP‡	MAX	UNIT
t_{pd}	Propagation delay time, $\overline{CLK}$↑ to $\overline{START}$	R1 = 270 Ω, R2 = 470 Ω		20	32	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↑ to $\overline{ACK}$	R1 = 270 Ω, R2 = 470 Ω		20	32	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↑ to $\overline{TM}$x	R1 = 270 Ω, R2 = 470 Ω		20	32	ns
t_{pd}	Enable time, $\overline{NMREQ}$ to $\overline{NMRQ}$	R1 = 270 Ω, R2 = 470 Ω		20	32	ns
t_{en}	Enable time, $\overline{CLK}$↑ to $\overline{RQST}$	R1 = 91 Ω, R2 = 220 Ω		18	32	ns
t_{en}	Enable time, $\overline{CLK}$↑ to $\overline{START}$	R1 = 270 Ω, R2 = 470 Ω		18	32	ns
t_{en}	Enable time, $\overline{CLK}$↑ to $\overline{ACK}$	R1 = 270 Ω, R2 = 470 Ω		18	32	ns
t_{en}	Enable time, $\overline{CLK}$↑ to $\overline{TM}$x	R1 = 270 Ω, R2 = 470 Ω		18	32	ns
t_{en}	Enable time, $\overline{CLK}$↓ to $\overline{ARB}$x	R1 = 91 Ω, R2 = 220 Ω		20	35	ns
t_{en}	Enable time, $\overline{CLK}$↑ to $\overline{SPV}$	R1 = 270 Ω, R2 = 470 Ω		23	45	ns

NuBus™ card-slot signals, C_L = 50 pF†

PARAMETER		LOAD	MIN	TYP‡	MAX	UNIT
t_{dis}	Disable time, $\overline{CLK}$↑ to $\overline{RQST}$	R1 = 91 Ω, R2 = 220 Ω		13	20	ns
t_{dis}	Disable time, $\overline{CLK}$↑ to $\overline{START}$	R1 = 270 Ω, R2 = 470 Ω		12	22	ns
t_{dis}	Disable time, $\overline{CLK}$↑ to $\overline{ACK}$	R1 = 270 Ω, R2 = 470 Ω		10	18	ns
t_{dis}	Disable time, $\overline{CLK}$↑ to $\overline{TM}$x	R1 = 270 Ω, R2 = 470 Ω		10	18	ns
t_{dis}	Disable time, $\overline{CLK}$↑ to $\overline{ARB}$x	R1 = 91 Ω, R2 = 220 Ω		13	24	ns
t_{dis}	Disable time, $\overline{CLK}$↑ to $\overline{SPV}$	R1 = 270 Ω, R2 = 470 Ω		10	18	ns

† See Parameter Measurement Information for load circuit and voltage waveforms.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

NuBus™ card-slot signals, C_L = 50 pF†

PARAMETER		LOAD	MIN	TYP‡	MAX	UNIT
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to NMSTR	RL= 500 Ω		12	21	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to MDONE	RL= 500 Ω		13	21	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to $\overline{SEREQ}$	RL= 500 Ω		13	21	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to NLTMx	R_L= 500 Ω		16	25	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to $\overline{NLRST}$	R_L= 500 Ω		11	21	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to NLOCK	R_L= 500 Ω		11	21	ns
t_{pd}	Propagation delay time, $\overline{CLK}$ to NLCK	R_L= 500 Ω		9	16	ns
t_{pd}	Propagation delay time, $\overline{CLK}$ to $\overline{NLCK}$	R_L= 500 Ω		10	18	ns
t_{pd}	Propagation delay time, $\overline{START}$ to NSTART	R_L= 500 Ω		8	14	ns
t_{pd}	Propagation delay time, $\overline{ACK}$ to NACK	R_L= 500 Ω		8	14	ns
t_{pd}	Propagation delay time, $\overline{TMx}$ to NTMx	R_L= 500 Ω		8	14	ns

NuBus™ buffer, C_L = 50 pF†

PARAMETER		LOAD	MIN	TYP‡	MAX	UNIT
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to ACLK high	R_L= 500 Ω		12	20	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↑ to ACLK low	R_L= 500 Ω		13	20	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to $\overline{AEN}$	R_L= 500 Ω		13	20	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to DCLK high	R_L= 500 Ω		12	20	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↑ to DCLK low	R_L= 500 Ω		14	22	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↓ to DEN	R_L= 500 Ω		14	22	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↑ to $\overline{ADEN}$	R_L= 500 Ω		9	14	ns
t_{pd}	Propagation delay time, $\overline{CLK}$↑ to $\overline{A}$/D	R_L= 500 Ω		9	14	ns

byte decode signals, C_L = 50 pF†

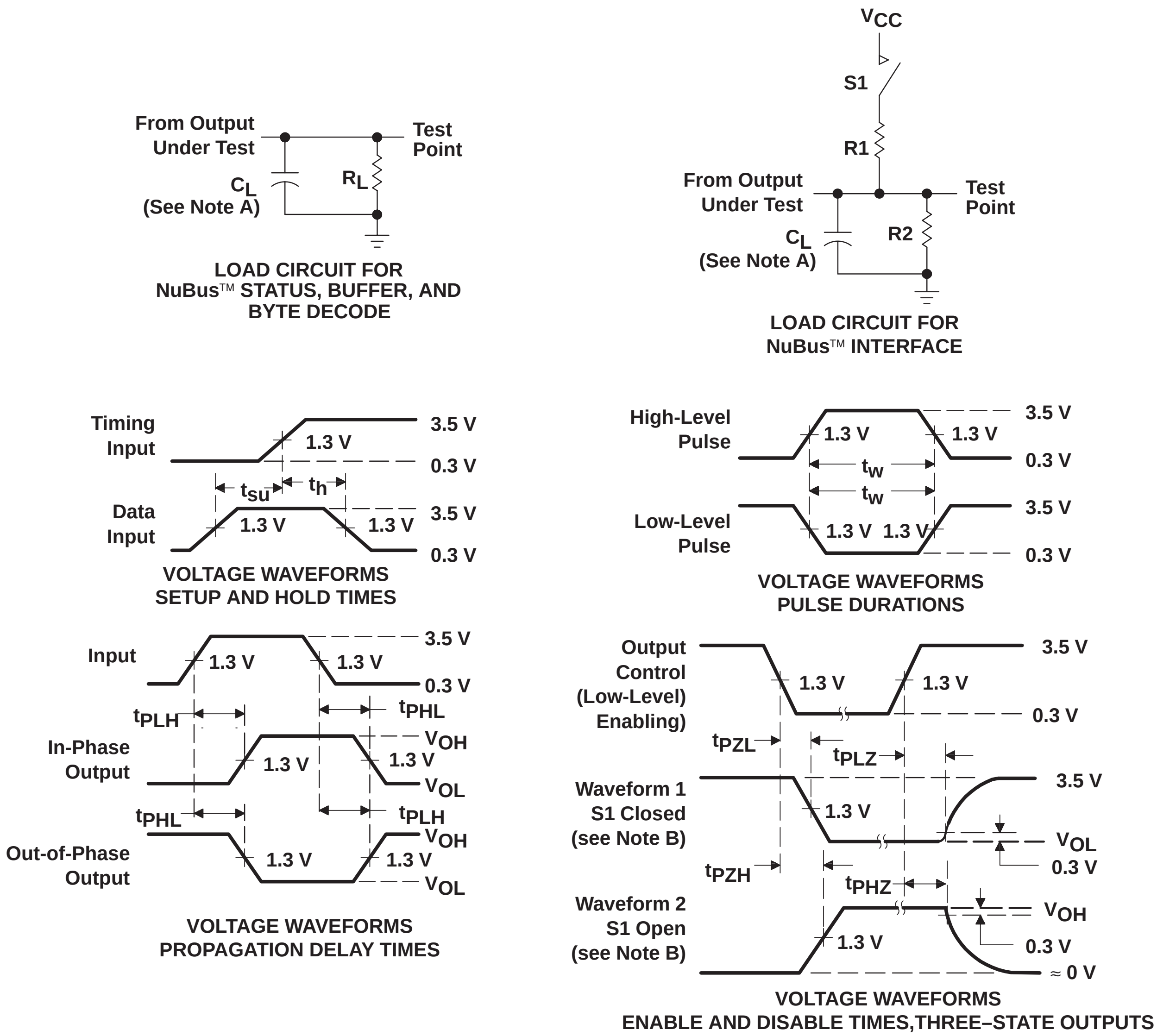
PARAMETER		LOAD	MIN	TYP‡	MAX	UNIT
t_{pd}	Propagation delay time, A0, A1, to $\overline{BT}$x	R_L= 500 Ω		17	28	ns

propagation delay relationships, C_L = 50 pF†

PARAMETER		LOAD	MIN	MAX	UNIT
t_{pd}§	Propagation delay time, MDONE, NLOCK, NMSTR, $\overline{SEREQ}$, $\overline{NLRST}$ before $\overline{NCLK}$↑	R_L= 500 Ω	15		ns
t_{pd}§	Propagation delay time, NLTMO, NLTM1 before $\overline{NCLK}$↑	R_L= 500 Ω	10		ns
t_{pd}¶	Propagation delay time, NSTART, NACK, NTMO, NTM1 after $\overline{NCLK}$↑	R_L= 500 Ω	5		ns

† See Parameter Measurement Information for load circuit and voltage waveforms.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The propagation delay minimums ensure that the status signals generated by the ’ACT2440 from the NuBus™ clock signal ($\overline{CLK}$) will be valid before the rising edge of $\overline{NCLK}$.
¶ This specification assumes the $\overline{START}$, $\overline{ACK}$, $\overline{TM0}$ and $\overline{TM1}$ NuBus™ signals have been generated by the ’ACT2440. During SLAVE cycles, this relationship is a function of the other MASTER driving these input signals.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%
D. The outputs are measured one at a time with one transition per measurement.

Figure 17. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN74ACT2440FN	OBSOLETE	PLCC	FN	68		TBD	Call TI	Call TI	
SN74ACT2440FNR	OBSOLETE	PLCC	FN	68		TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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