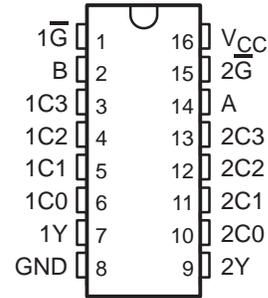


# SN54ALS352, SN74ALS352 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SDAS221A – APRIL 1982 – REVISED DECEMBER 1994

- Inverting Versions of the 'ALS153
- Permit Multiplexing From n Lines to One Line
- Perform Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (n Lines to n Lines)
- Typical Power Per Multiplexer Is 16 mW
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

**SN54ALS352 . . . J PACKAGE  
SN74ALS352 . . . D OR N PACKAGE  
(TOP VIEW)**

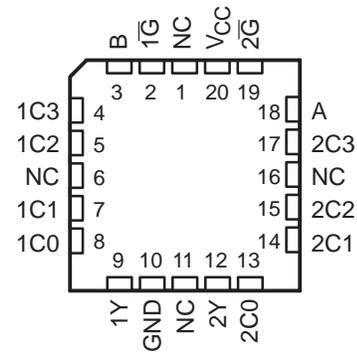


## description

These data selectors/multiplexers contain inverters and drivers to supply fully complementary binary decoding data selection to the AND-OR-invert gates. Separate strobe ( $\overline{G}$ ) inputs are provided for each of the two 4-line sections.

The SN54ALS352 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS352 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**SN54ALS352 . . . FK PACKAGE  
(TOP VIEW)**



NC – No internal connection

**FUNCTION TABLE**

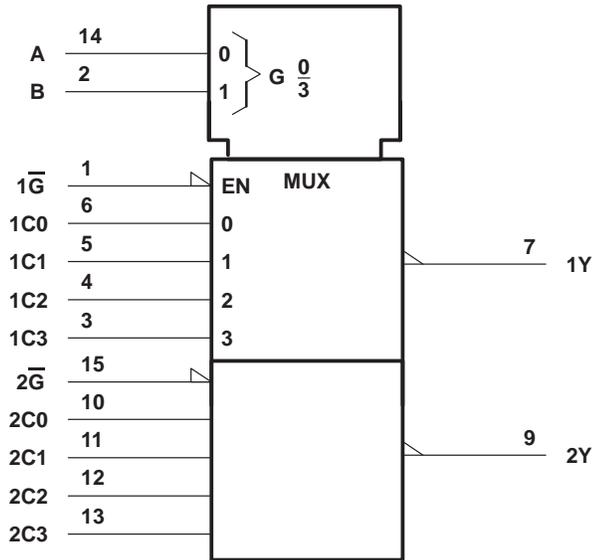
INPUTS						STROBE $\overline{G}$	OUTPUT Y
SELECT		DATA					
B	A	C0	C1	C2	C3		
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

# SN54ALS352, SN74ALS352 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

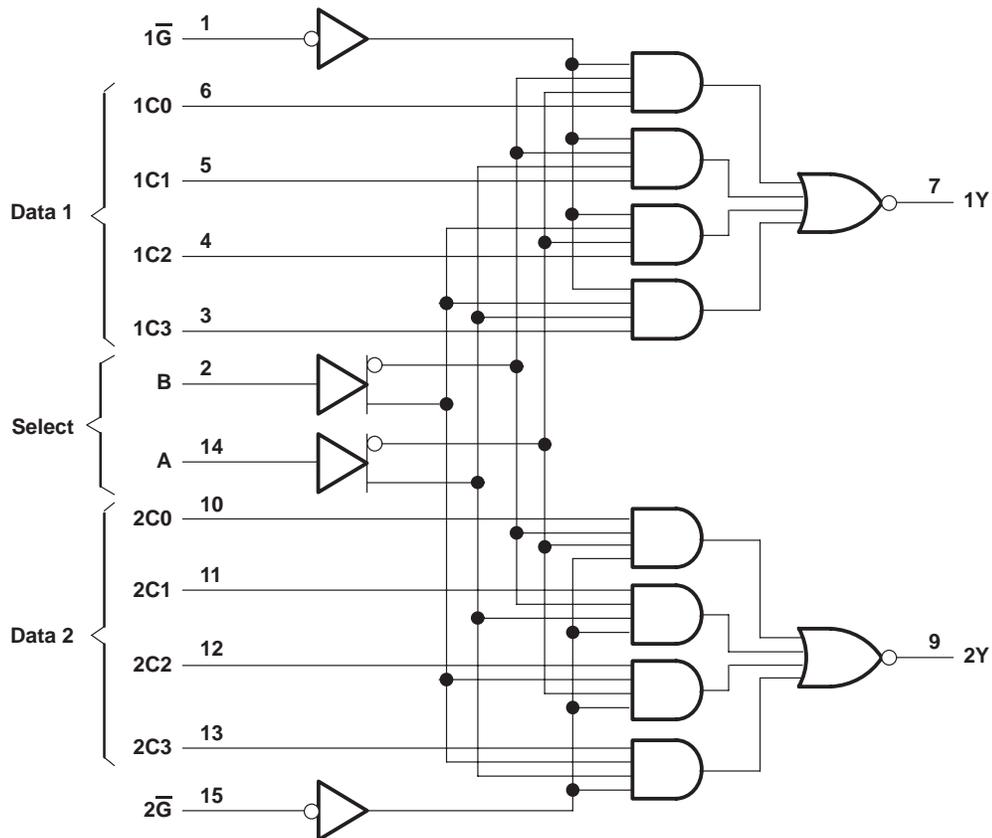
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

## logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

# SN54ALS352, SN74ALS352 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SDAS221A – APRIL 1982 – REVISED DECEMBER 1994

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ .....	7 V
Operating free-air temperature range, $T_A$ : SN54ALS352 .....	–55°C to 125°C
SN74ALS352 .....	0°C to 70°C
Storage temperature range .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN54ALS352			SN74ALS352			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			–1			–2.6	mA
$I_{OL}$	Low-level output current			12			24	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS352			SN74ALS352			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			–1.5			–1.5	V
$V_{OH}$	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -1\text{ mA}$	2.4	3.3					
	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -2.6\text{ mA}$				2.4	3.2		
$V_{OL}$	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 12\text{ mA}$		0.25	0.4		0.25	0.4	V
	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 24\text{ mA}$					0.35	0.5	
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$			20			20	μA
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$			–0.1			–0.1	mA
$I_{O}^{\S}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$	–20		–112	–30		–112	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$ , See Note 1		6.5	10		6.5	10	mA

‡ All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 1:  $I_{CC}$  is measured with data and select inputs at 4.5 V and G inputs grounded.



# SN54ALS352, SN74ALS352 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

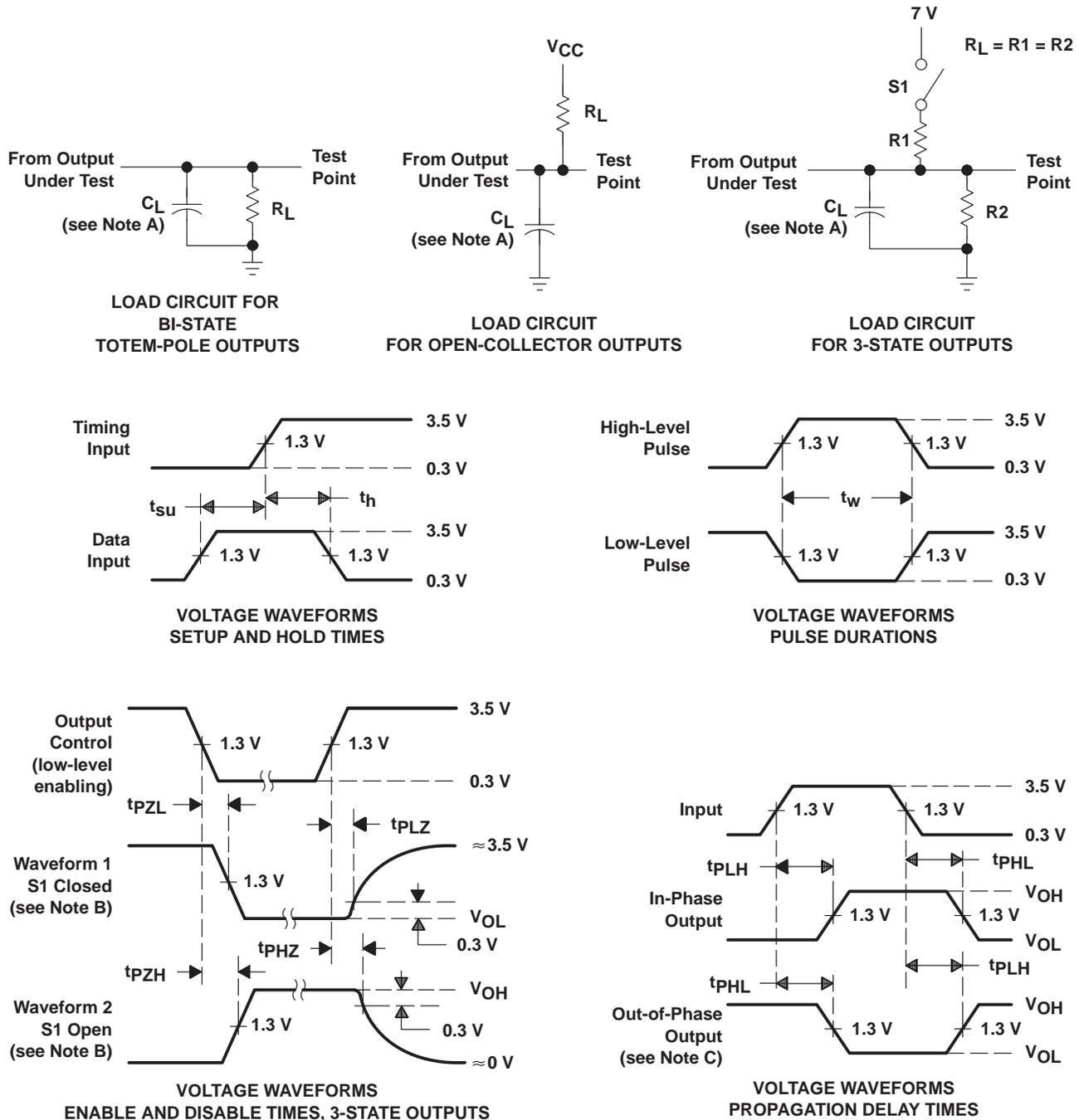
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## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}^\dagger$				UNIT
			SN54ALS352		SN74ALS352		
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	Y	5	32	5	24	ns
$t_{PHL}$			5	24	5	21	
$t_{PLH}$	Data (any C)	Y	3	24	3	18	ns
$t_{PHL}$			2	15	2	13	
$t_{PLH}$	$\bar{G}$	Y	4	26	4	18	ns
$t_{PHL}$			4	24	4	20	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION  
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN54ALS352J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74ALS352D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74ALS352DR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74ALS352N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SNJ54ALS352FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54ALS352J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

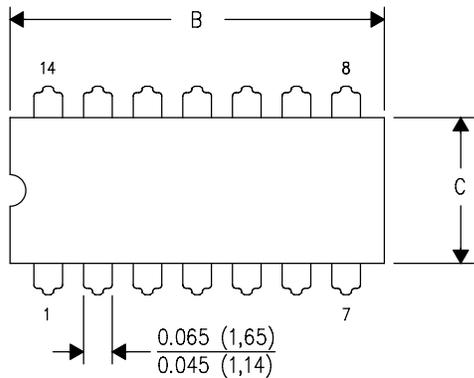
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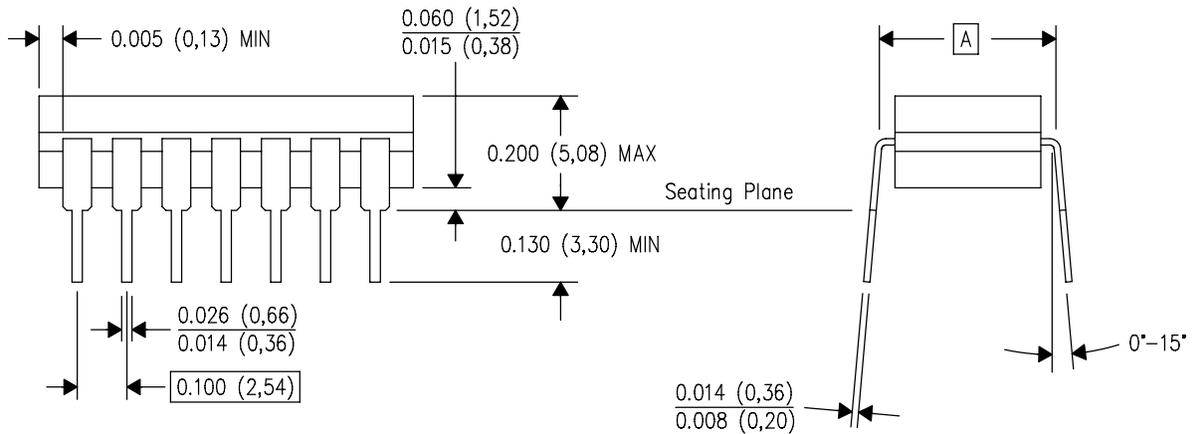
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



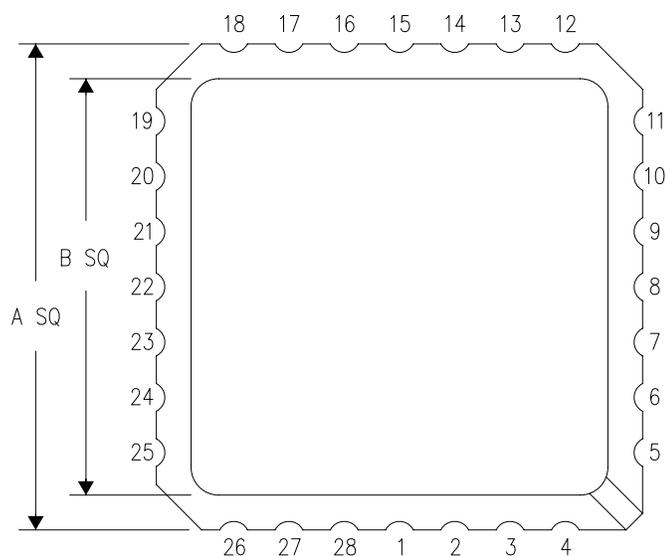
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

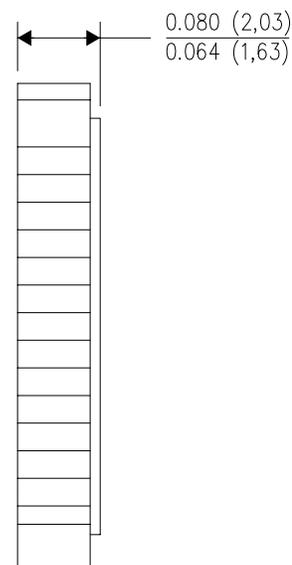
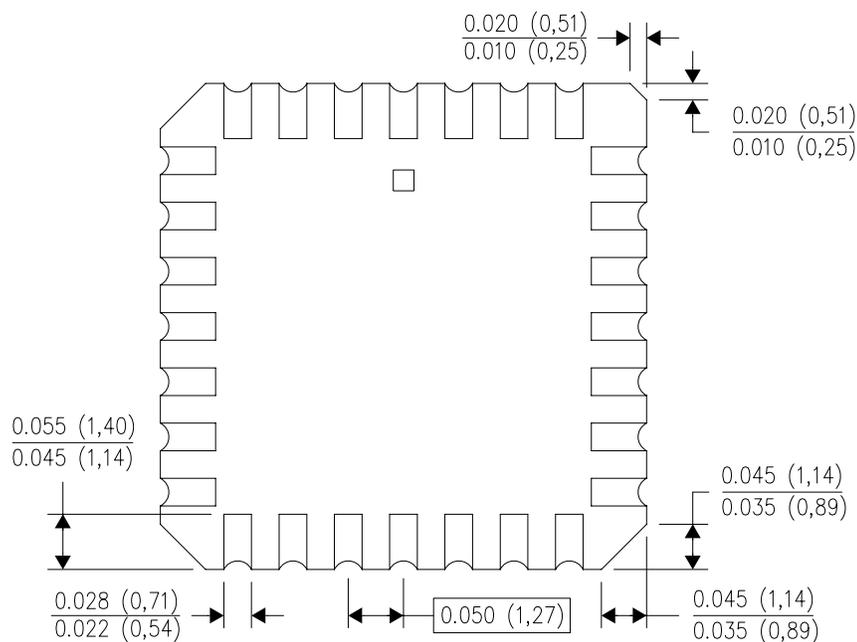
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

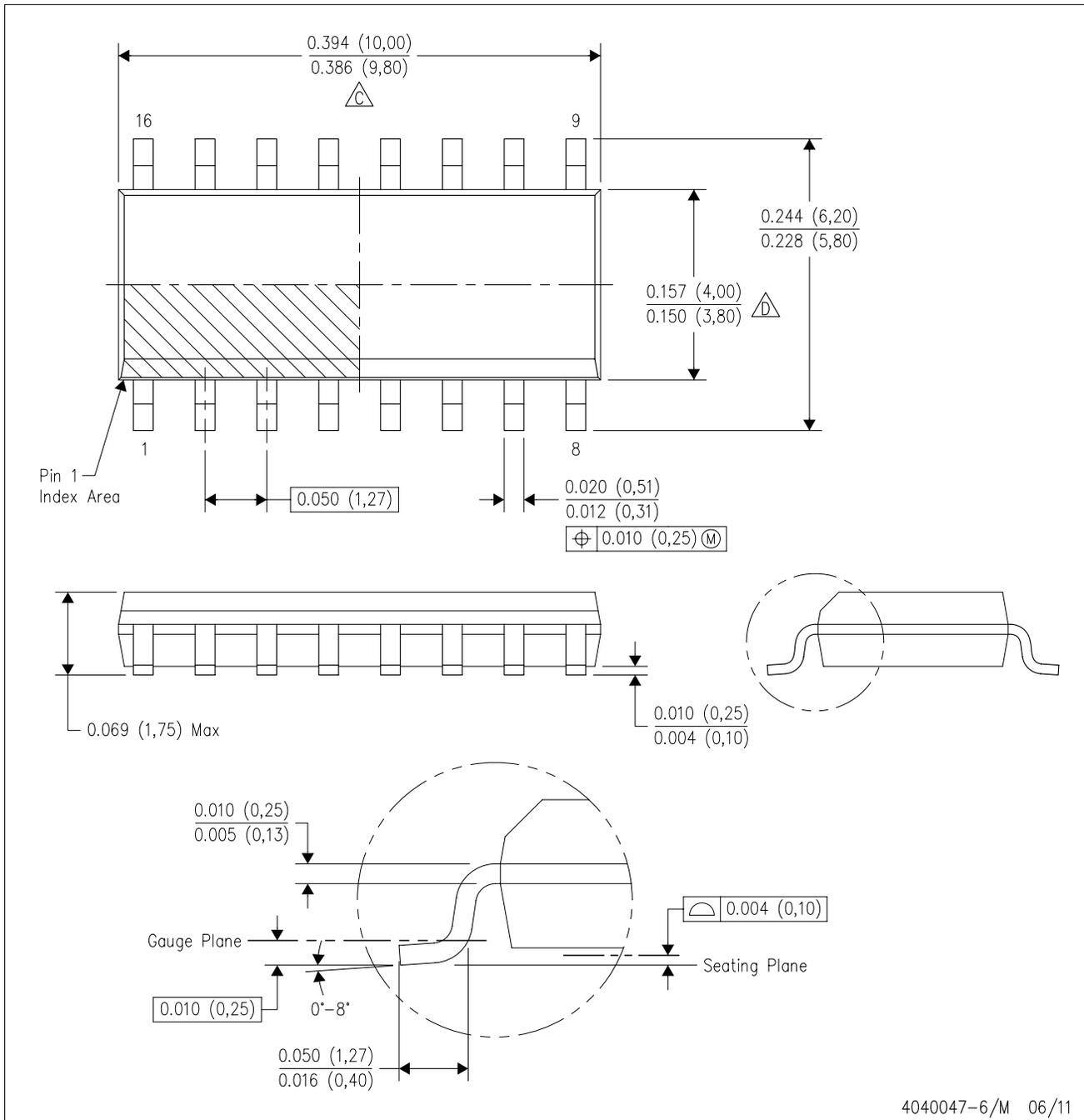


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

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