

# SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

SDAS229A – APRIL 1982 – REVISED JANUARY 1995

- 3-State Q Outputs Drive Bus Lines Directly
- Counter Operation Independent of 3-State Output
- Fully Synchronous Clear, Count, and Load
- Asynchronous Clear Is Also Provided
- Fully Cascadable
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

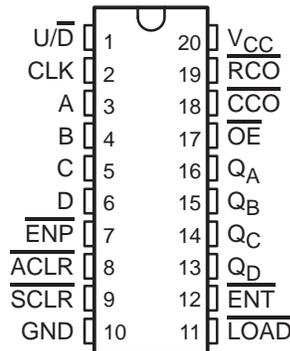
The SN74ALS568A decade counter and 'ALS569A binary counters are programmable, count up or down, and offer both synchronous and asynchronous clearing. All synchronous functions are executed on the positive-going edge of the clock (CLK) input.

The clear function is initiated by applying a low level to either asynchronous clear ( $\overline{\text{ACLR}}$ ) or synchronous clear ( $\overline{\text{SCLR}}$ ). Asynchronous (direct) clearing overrides all other functions of the device, while synchronous clearing overrides only the other synchronous functions. Data is loaded from the A, B, C, and D inputs by holding load ( $\overline{\text{LOAD}}$ ) low during a positive-going clock transition. The counting function is enabled only when enable P ( $\overline{\text{ENP}}$ ) and enable T ( $\overline{\text{ENT}}$ ) are low and  $\overline{\text{ACLR}}$ ,  $\overline{\text{SCLR}}$ , and  $\overline{\text{LOAD}}$  are high. The up/down ( $\overline{\text{U/D}}$ ) input controls the direction of the count. These counters count up when  $\overline{\text{U/D}}$  is high and count down when  $\overline{\text{U/D}}$  is low.

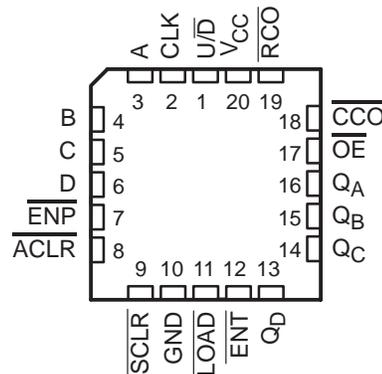
A high level at the output-enable ( $\overline{\text{OE}}$ ) input forces the Q outputs into the high-impedance state, and a low level enables those outputs. Counting is independent of  $\overline{\text{OE}}$ .  $\overline{\text{ENT}}$  is fed forward to enable the ripple-carry output ( $\overline{\text{RCO}}$ ) to produce a low-level pulse while the count is zero (all Q outputs low) when counting down or maximum (9 or 15) when counting up. The clocked carry output ( $\overline{\text{CCO}}$ ) produces a low-level pulse for a duration equal to that of the low level of the clock when  $\overline{\text{RCO}}$  is low and the counter is enabled (both  $\overline{\text{ENP}}$  and  $\overline{\text{ENT}}$  are low); otherwise,  $\overline{\text{CCO}}$  is high.  $\overline{\text{CCO}}$  does not have the glitches commonly associated with a ripple-carry output. Cascading is normally accomplished by connecting  $\overline{\text{RCO}}$  or  $\overline{\text{CCO}}$  of the first counter to  $\overline{\text{ENT}}$  of the next counter. However, for very high-speed counting,  $\overline{\text{RCO}}$  should be used for cascading since  $\overline{\text{CCO}}$  does not become active until the clock returns to the low level.

The SN54ALS569A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS568A and SN74ALS569A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS569A . . . J PACKAGE  
SN74ALS568A, SN74ALS569A . . . DW OR N PACKAGE  
(TOP VIEW)



SN54ALS569A . . . FK PACKAGE  
(TOP VIEW)



**SN54ALS569A, SN74ALS568A, SN74ALS569A**  
**SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS**  
**WITH 3-STATE OUTPUTS**

SDAS229A – APRIL 1982 – REVISED JANUARY 1995

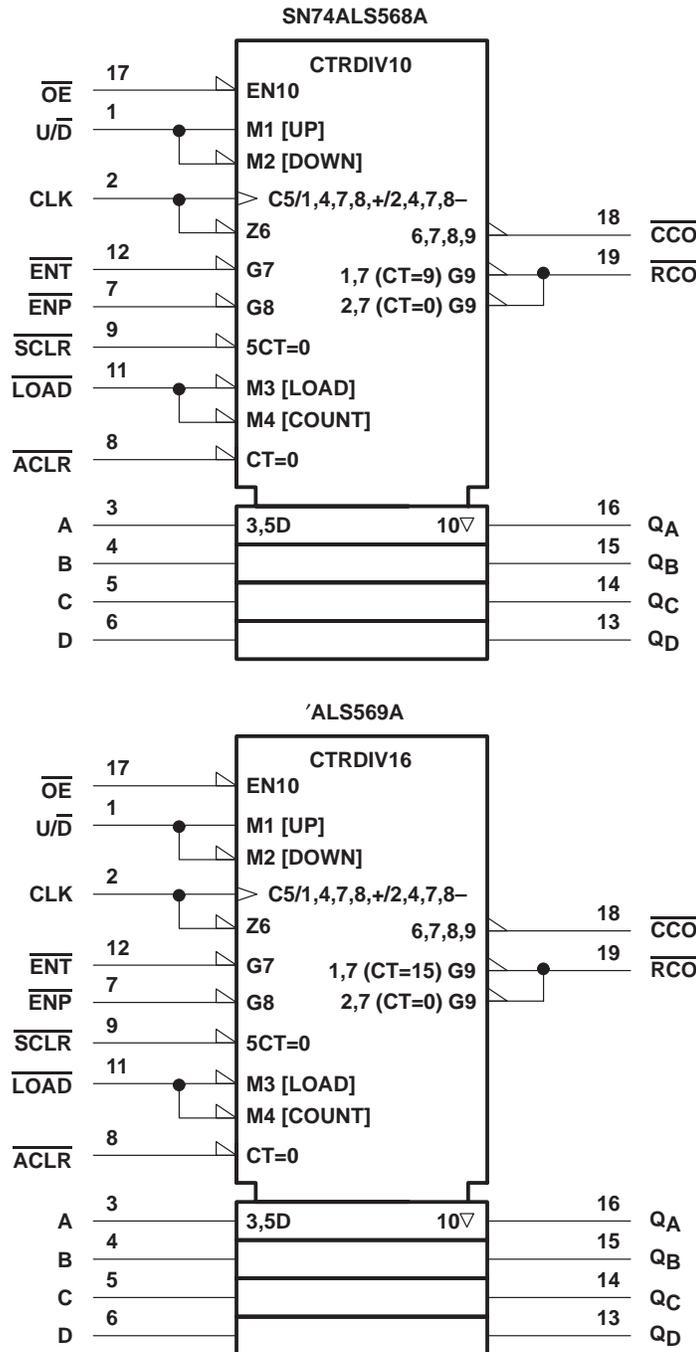
FUNCTION TABLE

INPUTS								OPERATION
$\overline{OE}$	$\overline{ACLR}$	$\overline{SCLR}$	$\overline{LOAD}$	$\overline{ENT}$	$\overline{ENP}$	U/D	CLK	
H	X	X	X	X	X	X	X	Q outputs disabled
L	L	X	X	X	X	X	X	Asynchronous clear
L	H	L	X	X	X	X	↑	Synchronous clear
L	H	H	L	X	X	X	↑	Load
L	H	H	H	L	L	H	↑	Count up
L	H	H	H	L	L	L	↑	Count down
L	H	H	H	H	X	X	X	Inhibit count
L	H	H	H	X	H	X	X	Inhibit count

# SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

SDAS229A – APRIL 1982 – REVISED JANUARY 1995

logic symbols†

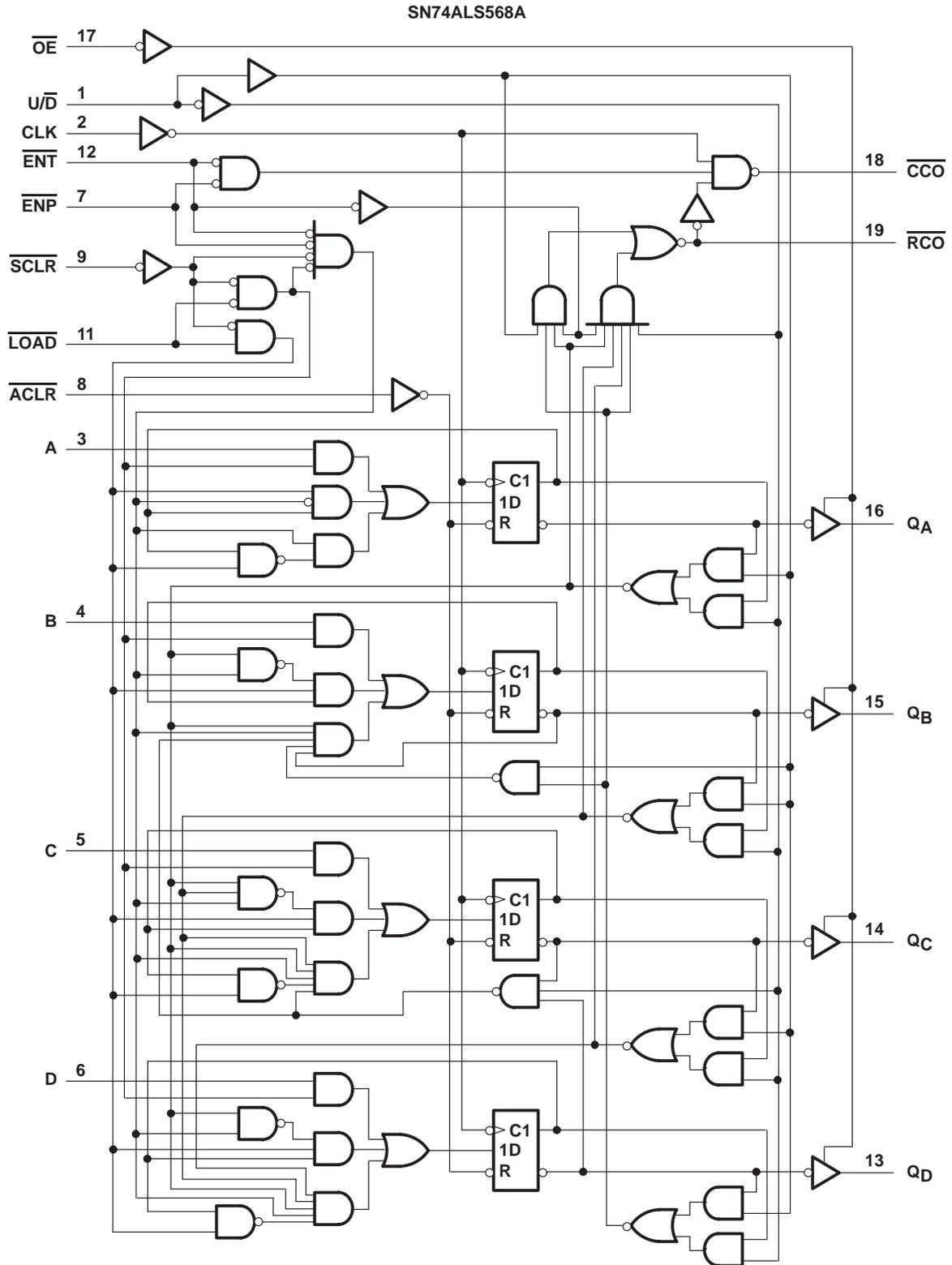


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

SDAS229A – APRIL 1982 – REVISED JANUARY 1995

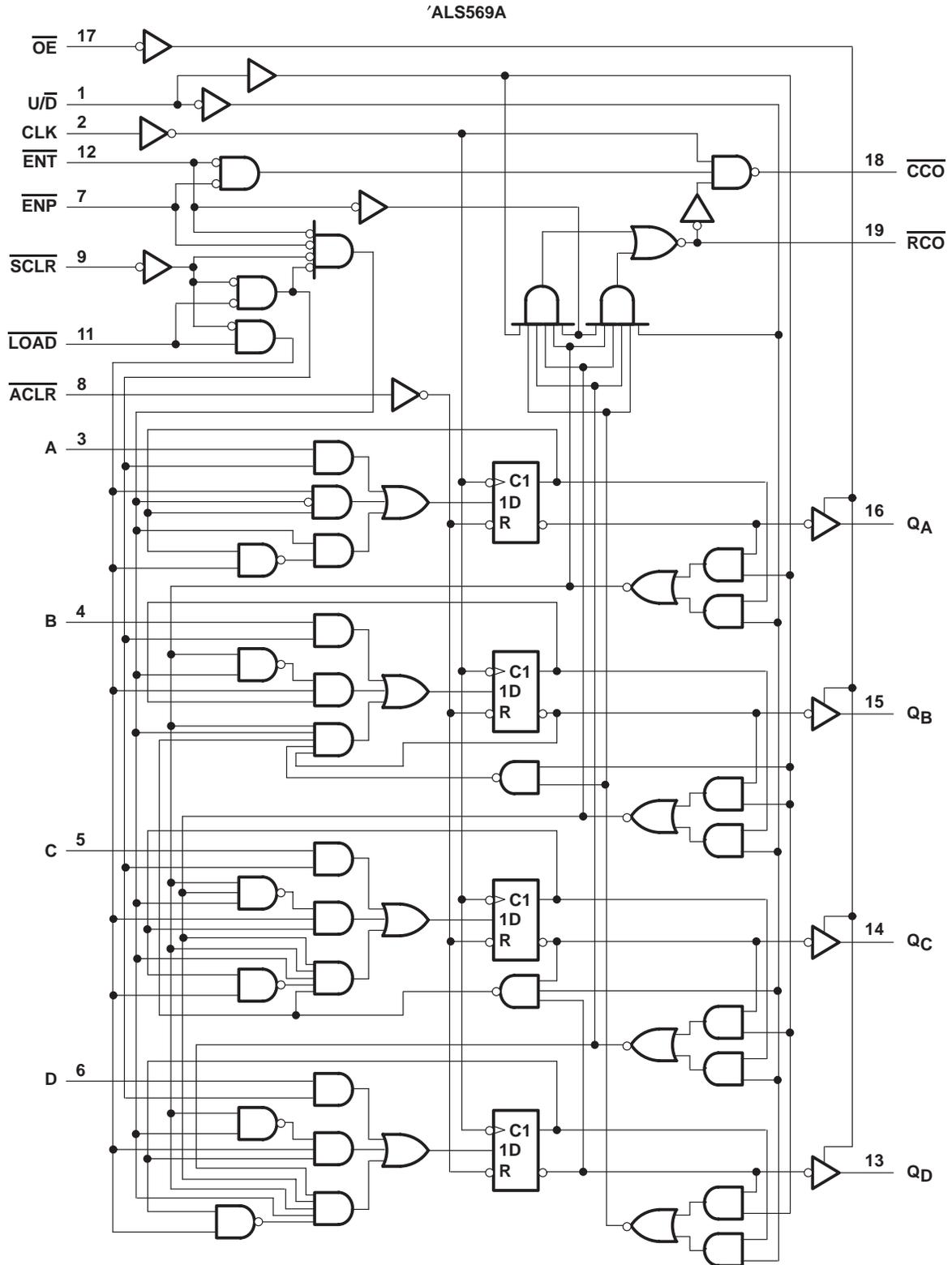
## logic diagrams (positive logic)



SN54ALS569A, SN74ALS568A, SN74ALS569A  
 SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS  
 WITH 3-STATE OUTPUTS

SDAS229A - APRIL 1982 - REVISED JANUARY 1995

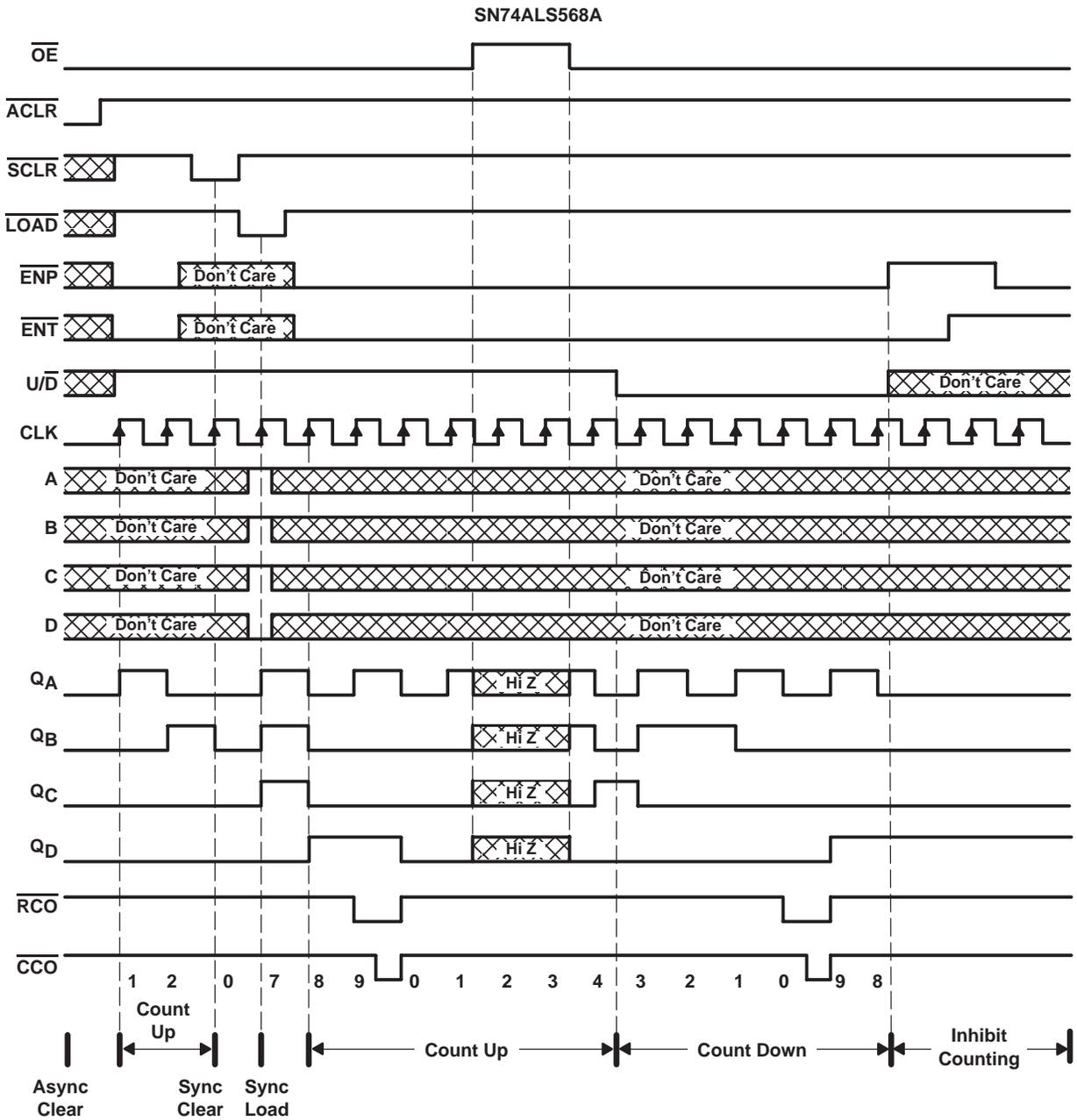
logic diagrams (positive logic) (continued)



# SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

SDAS229A – APRIL 1982 – REVISED JANUARY 1995

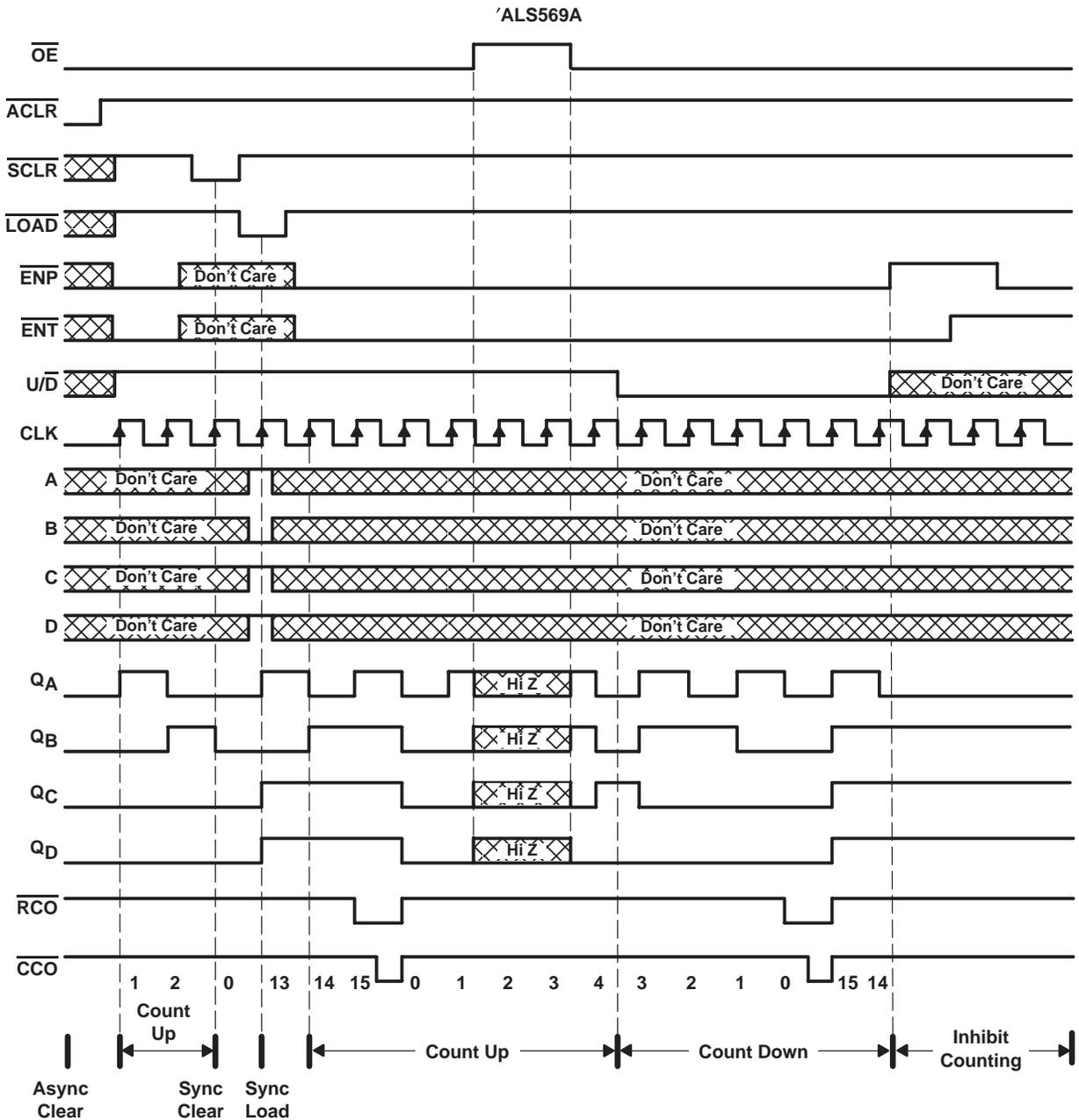
## typical load, count, and inhibit sequences



# SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

SDAS229A – APRIL 1982 – REVISED JANUARY 1995

## typical load, count, and inhibit sequences (continued)



# SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

SDAS229A – APRIL 1982 – REVISED JANUARY 1995

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS569A	-55°C to 125°C
SN74ALS568A, SN74ALS569A	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN54ALS569A			SN74ALS568A SN74ALS569A			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
$V_{IH}$	High-level input voltage	2			2			V		
$V_{IL}$	Low-level input voltage			0.7			0.8	V		
$I_{OH}$	High-level output current	Q outputs		-1			-2.6	mA		
		$\overline{CCO}$ and $\overline{RCO}$				-0.4	-0.4			
$I_{OL}$	Low-level output current	Q outputs				12	24	mA		
		$\overline{CCO}$ and $\overline{RCO}$				4	8			
$f_{clock}$	Clock frequency	SN74ALS568A				0	20	MHz		
		'ALS569A				0	30			
$t_w$	Pulse duration	$\overline{ACLR}$ or $\overline{LOAD}$ low				20	15	ns		
		SN74ALS568A	CLK high				25			
			CLK low				25			
		'ALS569A	CLK high				20		16.5	
CLK low					23	16.5				
$t_{su}$	Setup time before $CLK\uparrow$	Data at A, B, C, D				25	20	ns		
		$\overline{ENP}$ , $\overline{ENT}$	High				35		30	
			Low				25		20	
		$\overline{SCLR}$	Low				20		15	
			High (inactive)				35		30	
		$\overline{LOAD}$	Low				20		15	
			High (inactive)				35		30	
$\overline{U/D}$						35	30			
$\overline{ACLR}$ inactive						10	10			
$t_h$	Hold time after $CLK\uparrow$ for any input					0	0	ns		
$T_A$	Operating free-air temperature					-55	125	0	70	°C



# SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

SDAS229A – APRIL 1982 – REVISED JANUARY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS569A			SN74ALS568A SN74ALS569A			UNIT	
				MIN	TYP†	MAX	MIN	TYP†	MAX		
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$		-1.5			-1.5			V	
$V_{OH}$	All outputs	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$		$V_{CC} - 2$			$V_{CC} - 2$			V	
	Q outputs	$V_{CC} = 4.5\text{ V}$		2.4 3.3			2.4 3.2				
$V_{OL}$	Q outputs	$V_{CC} = 4.5\text{ V}$		0.25 0.4						0.25 0.4	
				0.35 0.5			0.25 0.4				
	$\overline{CCO}$ and $\overline{RCO}$		$V_{CC} = 4.5\text{ V}$		0.25 0.4			0.25 0.4			
					0.35 0.5			0.35 0.5			
$I_{OZH}$		$V_{CC} = 5.5\text{ V}$ , $V_O = 2.7\text{ V}$		20			20			$\mu\text{A}$	
$I_{OZL}$		$V_{CC} = 5.5\text{ V}$ , $V_O = 0.4\text{ V}$		-20			-20			$\mu\text{A}$	
$I_I$		$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$		0.1			0.1			mA	
$I_{IH}$		$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$		20			20			$\mu\text{A}$	
$I_{IL}$		$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$		-0.2			-0.2			mA	
$I_{O\ddagger}$	$\overline{CCO}$ and $\overline{RCO}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$		-15 -70			-15 -70			mA	
	Q outputs			-20 -112			-30 -112				
$I_{CC}$		$V_{CC} = 5.5\text{ V}$		16 26			16 26			mA	
				20 32			20 32				
				20 32			20 32				

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

# SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

SDAS229A – APRIL 1982 – REVISED JANUARY 1995

## switching characteristics (see Figure 1)

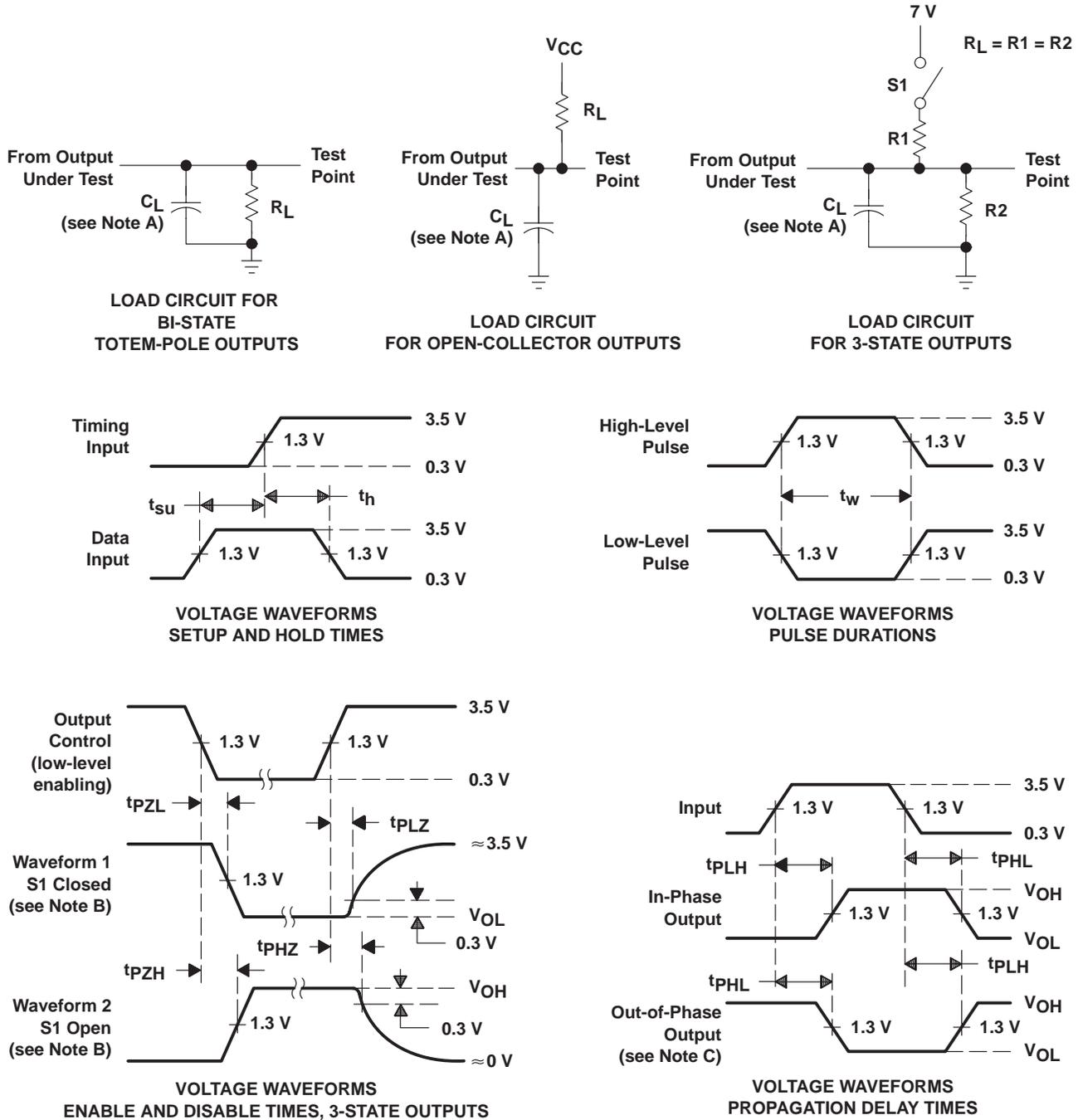
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54ALS569A		SN74ALS568A SN74ALS569A		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>	SN74ALS568A				20	MHz	
	'ALS569A		22	30			
t <sub>PLH</sub>	CLK	Any Q	4	21	4	13	ns
t <sub>PHL</sub>			7	19	7	16	
t <sub>PLH</sub>	CLK	$\overline{RCO}$	12	37	12	28	ns
t <sub>PHL</sub>			10	28	10	19	
t <sub>PLH</sub>	CLK	$\overline{CCO}$	5	17	5	13	ns
t <sub>PHL</sub>			6	30	6	25	
t <sub>PLH</sub>	U/ $\overline{D}$	$\overline{RCO}$	9	31	9	23	ns
t <sub>PHL</sub>			9	33	9	19	
t <sub>PLH</sub>	$\overline{ENT}$	$\overline{RCO}$	6	21	6	15	ns
t <sub>PHL</sub>			4	20	4	13	
t <sub>PLH</sub>	$\overline{ENT}$	$\overline{CCO}$	5	18	5	13	ns
t <sub>PHL</sub>			9	32	9	23	
t <sub>PLH</sub>	$\overline{ENP}$	$\overline{CCO}$	4	18	4	12	ns
t <sub>PHL</sub>			5	18	5	14	
t <sub>PHL</sub>	$\overline{ACLR}$	Any Q	9	25	9	20	ns
t <sub>PZH</sub>	$\overline{OE}$	Any Q	6	23	6	18	ns
t <sub>PZL</sub>			6	29	6	24	
t <sub>PHZ</sub>	$\overline{OE}$	Any Q	1	12	1	10	ns
t <sub>PLZ</sub>			3	29	3	13	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

SDAS229A – APRIL 1982 – REVISED JANUARY 1995

## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
83025022A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
8302502RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
8302502SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
SN54ALS569AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN74ALS568AN	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	
SN74ALS569ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS569ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS569ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS569AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS569ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SNJ54ALS569AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54ALS569AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54ALS569AW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54ALS569A, SN74ALS569A :**

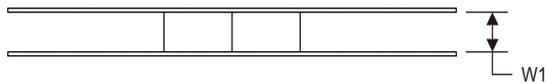
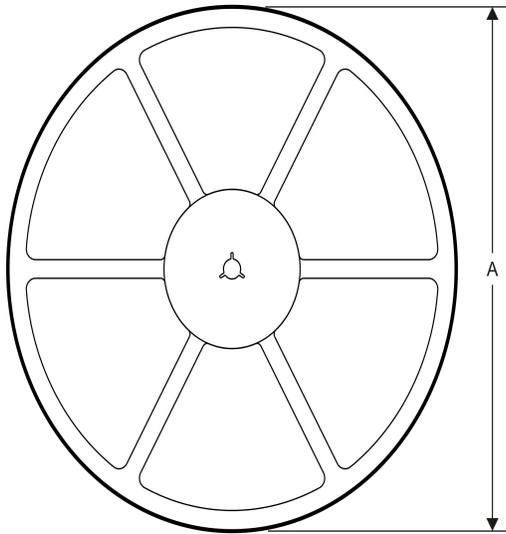
- Catalog: [SN74ALS569A](#)
- Military: [SN54ALS569A](#)

NOTE: Qualified Version Definitions:

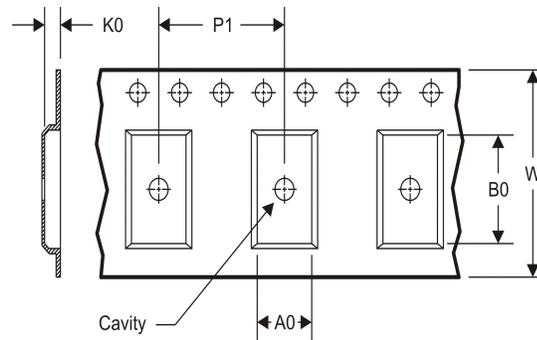
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



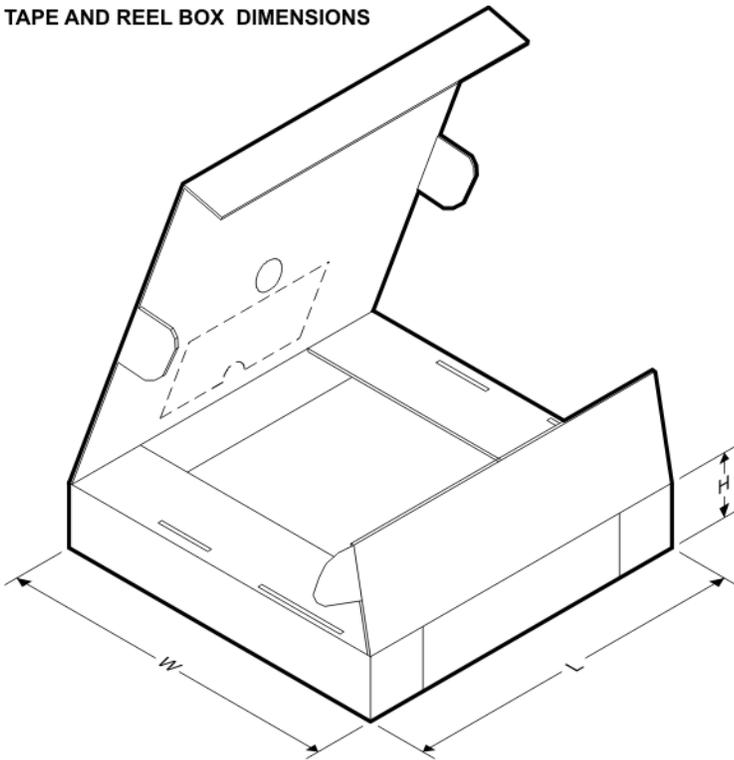
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS569ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



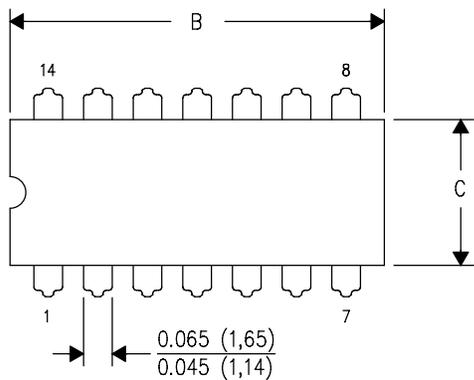
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS569ADWR	SOIC	DW	20	2000	367.0	367.0	45.0

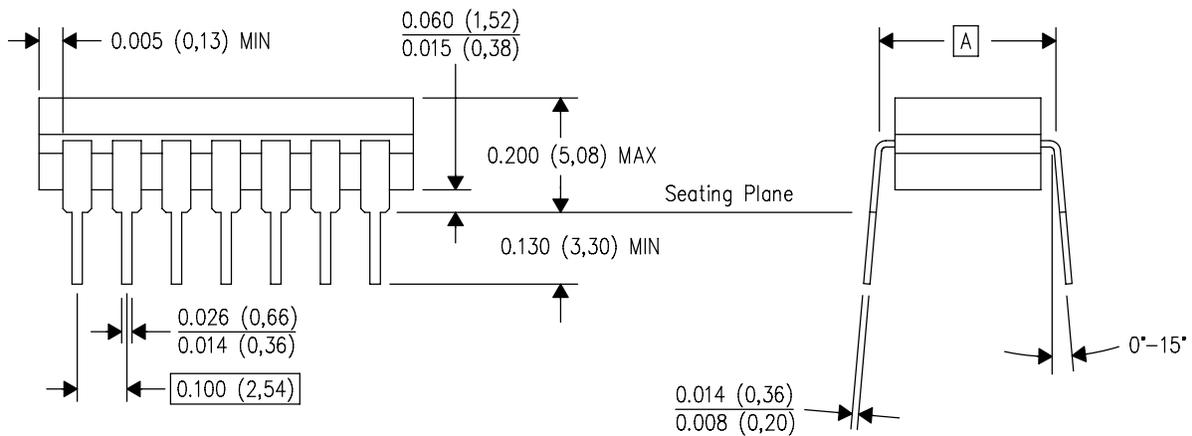
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

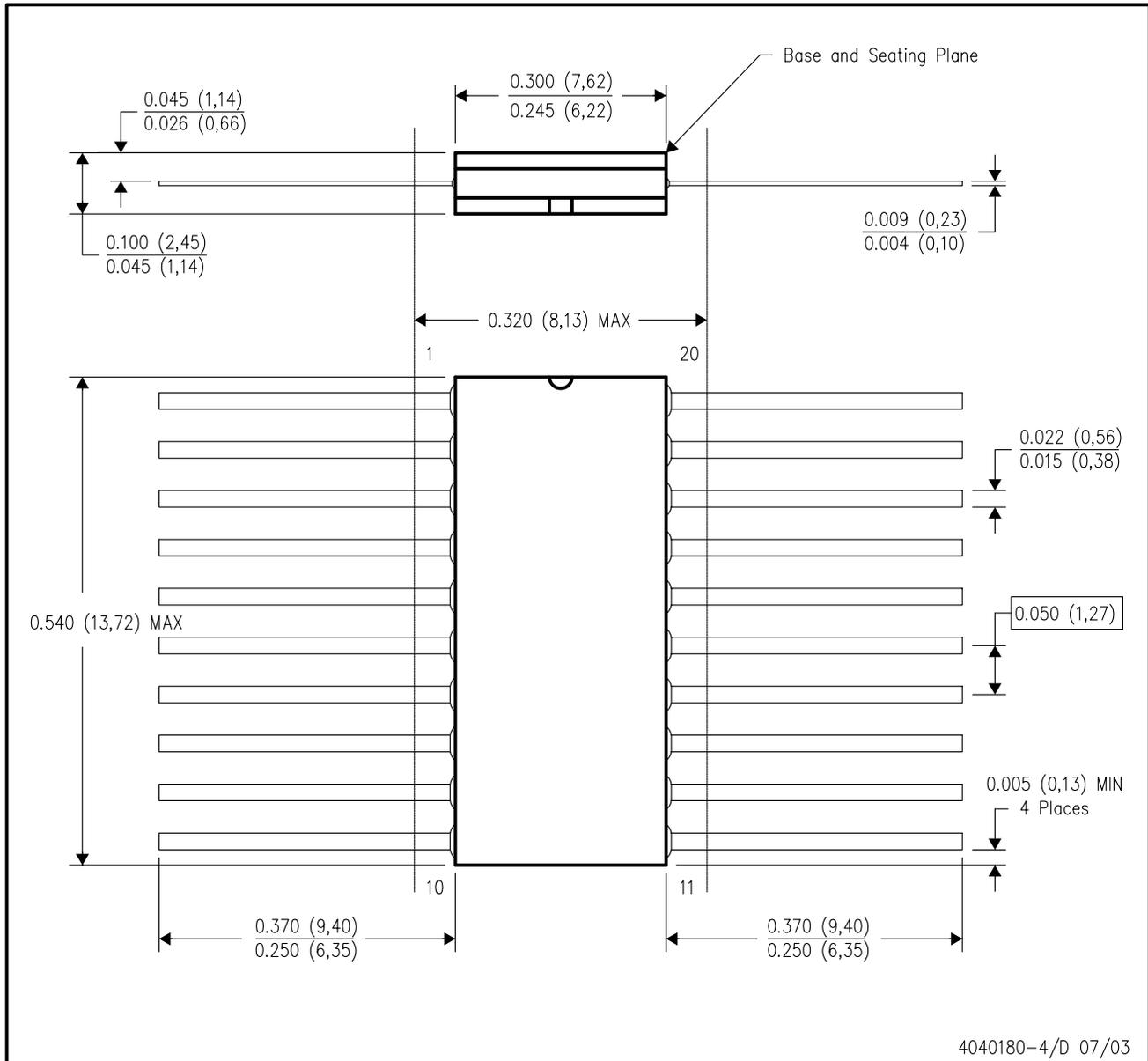


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



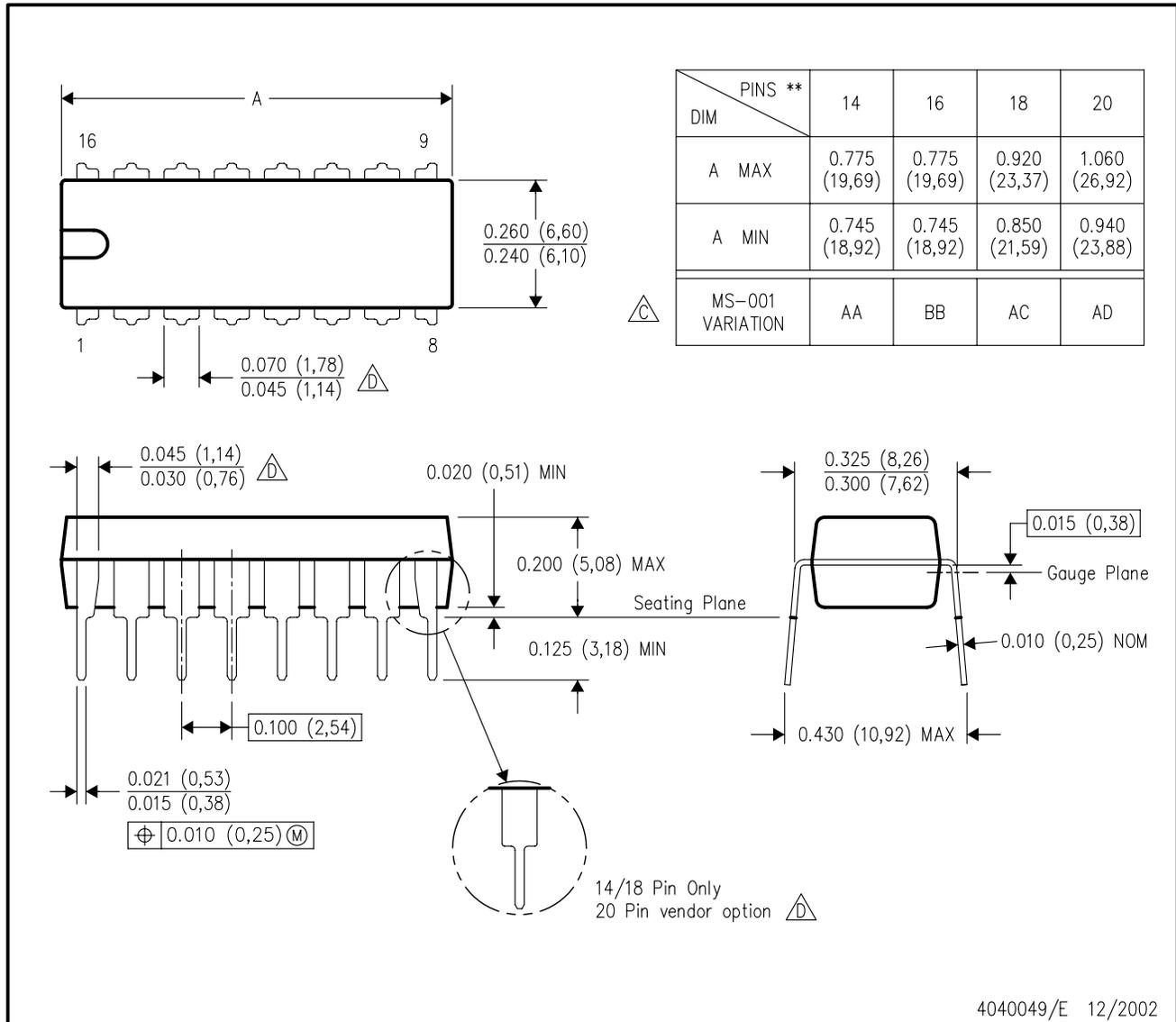
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

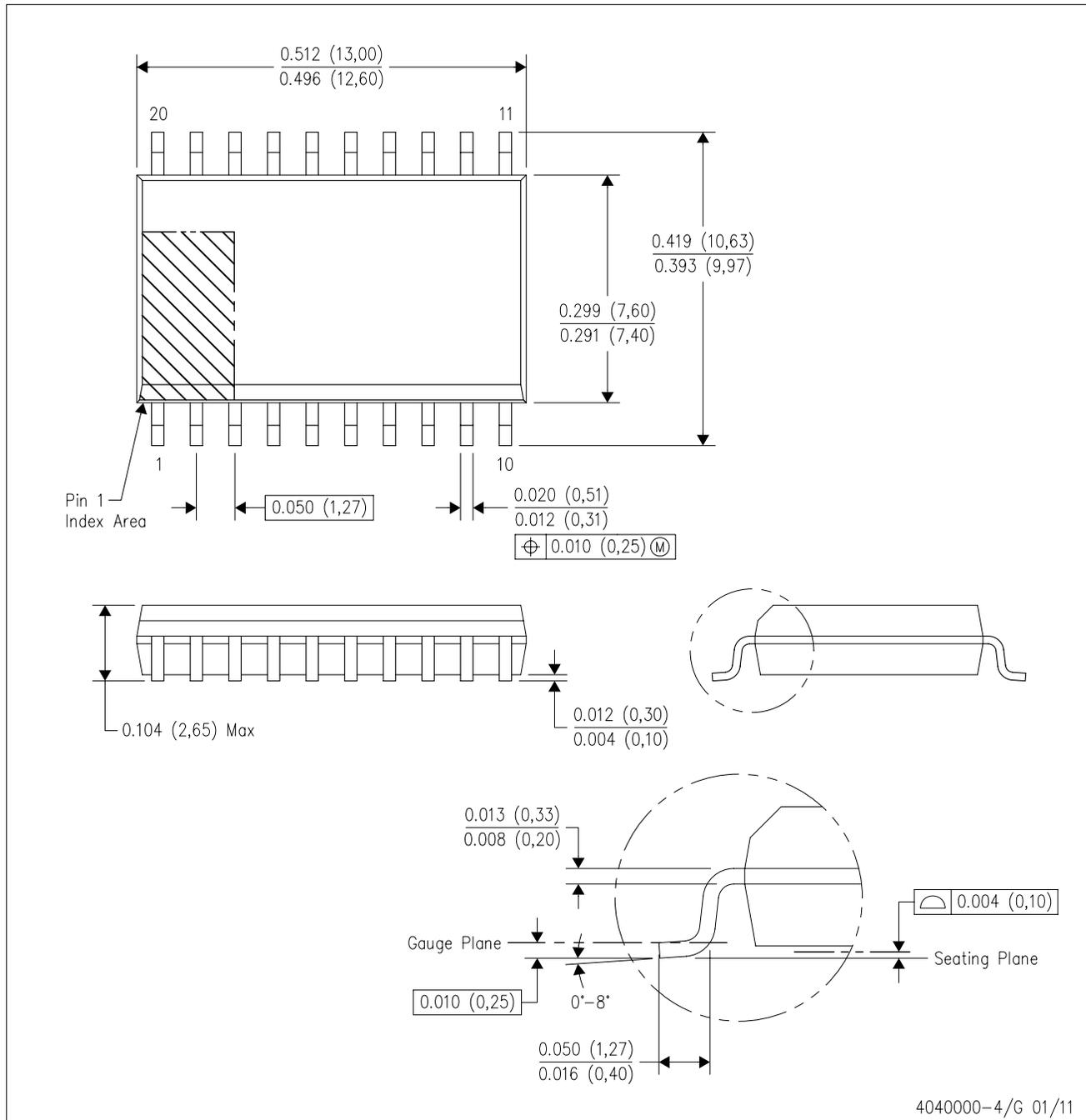
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

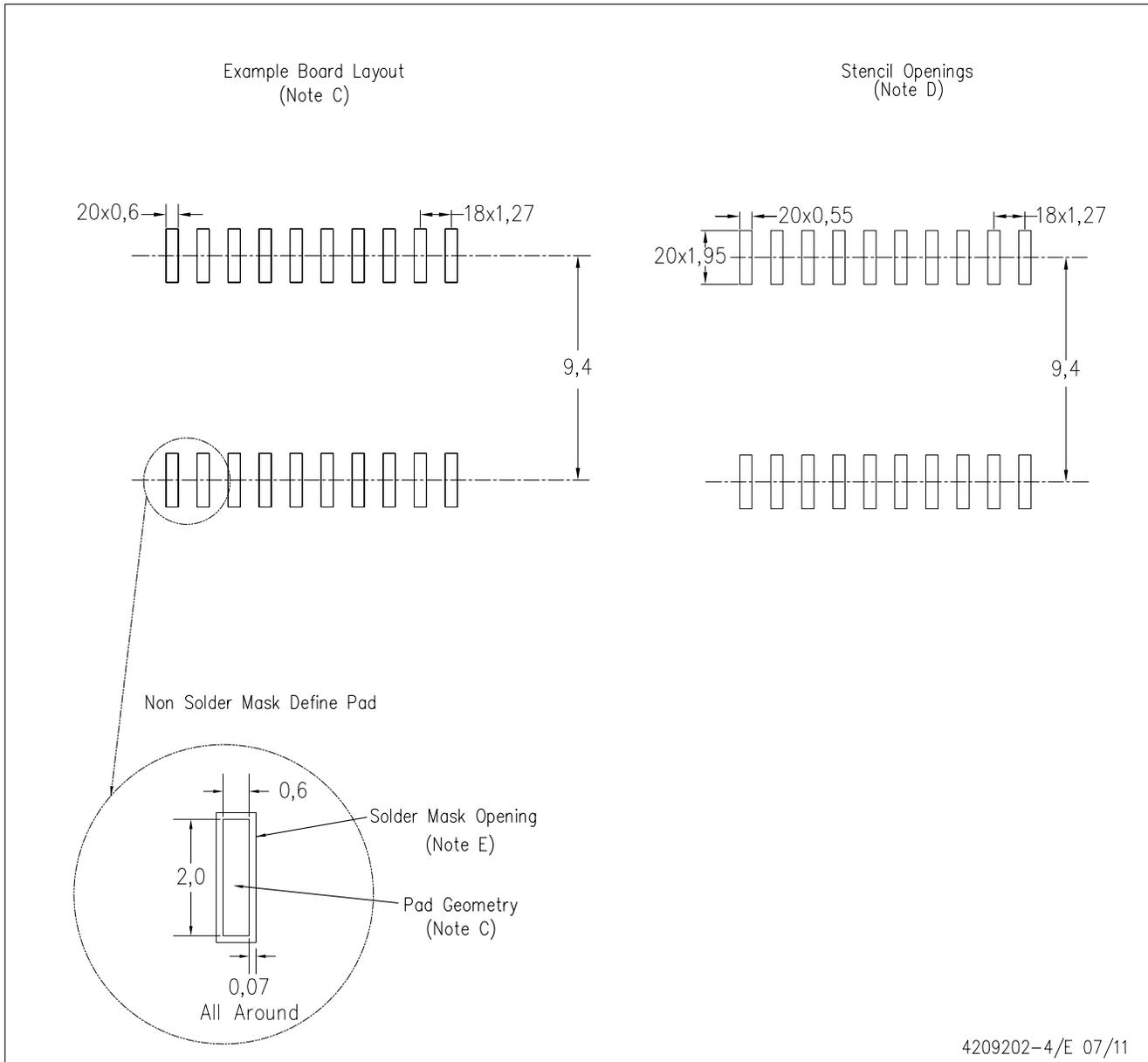
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4209202-4/E 07/11

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46C and to discontinue any product or service per JESD48B. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Mobile Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

**TI E2E Community** [e2e.ti.com](http://e2e.ti.com)