# LOW-POWER SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

Check for Samples: SN74AUP1G80

FEATURES

- **Available in the Texas Instruments NanoStar™ Package**
- **Low Static-Power Consumption (I_{CC} = 0.9 μA Max)**
- **Low Dynamic-Power Consumption (C_{pd} = 4.3 pF Typ at 3.3 V)**
- **Low Input Capacitance (C_i = 1.5 pF Typ)**
- **Low Noise – Overshoot and Undershoot <10% of V_{CC}**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Schmitt-Trigger Action Allows Slow Input Transition and Better Switching Noise Immunity at the Input (V_{hys} = 250 mV Typ at 3.3 V)**

- **Wide Operating V_{CC} Range of 0.8 V to 3.6 V**
- **Optimized for 3.3-V Operation**
- **3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation**
- **t_{pd} = 4.4 ns Max at 3.3 V**
- **Suitable for Point-to-Point Applications**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

DBV PACKAGE (TOP VIEW)

DCK PACKAGE (TOP VIEW)

DRY PACKAGE (TOP VIEW)

DSF PACKAGE (TOP VIEW)

YFP PACKAGE (TOP VIEW)

YZP PACKAGE (TOP VIEW)
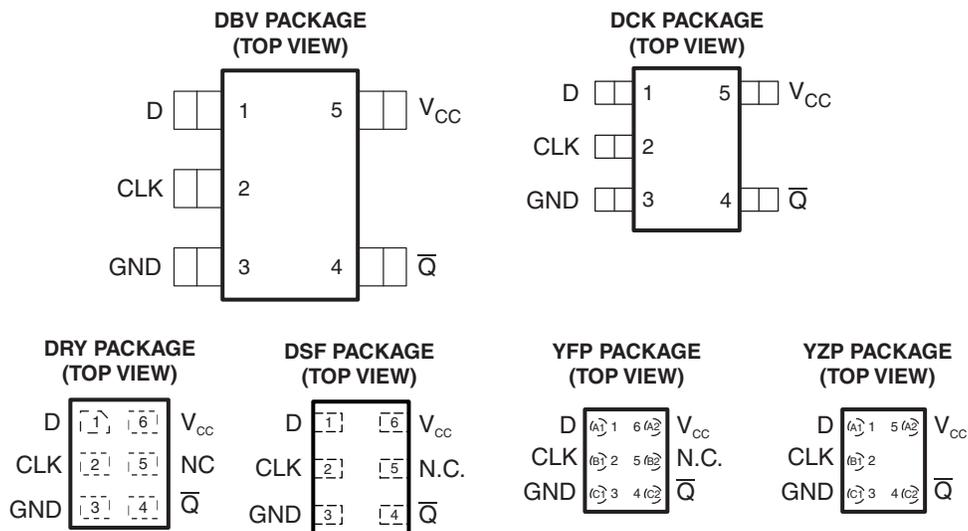
See mechanical drawings for dimensions.

N.C. – No internal connection

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life (see Figure 1). This product also maintains excellent signal integrity (see Figure 2).

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74AUP1G80
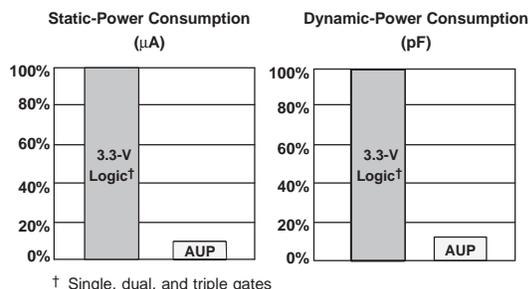
Figure 1. AUP – The Lowest-Power Family
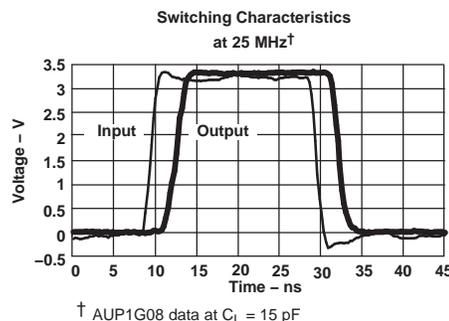
† AUP1G08 data at C_L = 15 pF

Figure 2. Excellent Signal Integrity

This is a single positive-edge-triggered D-type flip-flop. When data at the data (D) input meets the setup time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION[1]

T_A	PACKAGE[2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[3]
−40°C to 85°C	NanoStar – WCSP (DSBGA) 0.23-mm Large Bump – YFP	Reel of 3000	SN74AUP1G80YFPR	_ _ _HX_
	NanoStar – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUP1G80YZPR	_ _ _HX_
	QFN – DRY	Reel of 5000	SN74AUP1G80DRYR	HX
	uQFN – DSF	Reel of 5000	SN74AUP1G80DSFR	HX
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G80DBVR	H80_
		Reel of 250	SN74AUP1G80DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G80DCKR	HX_
		Reel of 250	SN74AUP1G80DCKT	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DBV/DCK: The actual top-side marking has one additional character that designates the wafer fab/assembly site.
YFP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUTS		OUTPUT
CLK	D	$\overline{Q}$
↑	H	L
↑	L	H
L or H	X	$\overline{Q}_0$

LOGIC DIAGRAM (POSITIVE LOGIC)

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Product Folder Link(s): SN74AUP1G80
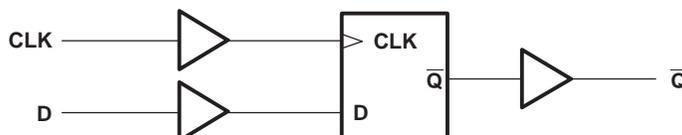
ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range [2]		–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state [2]		–0.5	4.6	V
V_O	Voltage range applied to any output in the high or low state [2]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance [3]	DBV package		206	°C/W
		DCK package		252	
		DSF package		300	
		DRY package		243	
		YFP/YZP package		132	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Product Folder Link(s): *SN74AUP1G80*

RECOMMENDED OPERATING CONDITIONS[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	$0.65 \times V_{CC}$		
		V_{CC} = 2.3 V to 2.7 V	1.6		
		V_{CC} = 3 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		$0.35 \times V_{CC}$	
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.9	
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current[2]	V_{CC} = 0.8 V		−20	µA
		V_{CC} = 1.1 V		−1.1	mA
		V_{CC} = 1.4 V		−1.7	
		V_{CC} = 1.65		−1.9	
		V_{CC} = 2.3 V		−3.1	
		V_{CC} = 3 V		−4	
I_{OL}	Low-level output current[2]	V_{CC} = 0.8 V		20	µA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 0.8 V to 3.6 V		200	ns/V
T_A	Operating free-air temperature		−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.
(2) Defined by the signal integrity requirements and design-goal priorities.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V$_{CC}$	T$_A$ = 25°C			T$_A$ = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V$_{OH}$		I$_{OH}$ = −20 µA	0.8 V to 3.6 V	V$_{CC}$ − 0.1			V$_{CC}$ − 0.1		V
		I$_{OH}$ = −1.1 mA	1.1 V	0.75 × V$_{CC}$			0.7 × V$_{CC}$		
		I$_{OH}$ = −1.7 mA	1.4 V	1.11			1.03		
		I$_{OH}$ = −1.9 mA	1.65 V	1.32			1.3		
		I$_{OH}$ = −2.3 mA	2.3 V	2.05			1.97		
		I$_{OH}$ = −3.1 mA		1.9			1.85		
		I$_{OH}$ = −2.7 mA	3 V	2.72			2.67		
		I$_{OH}$ = −4 mA		2.6			2.55		
V$_{OL}$		I$_{OL}$ = 20 µA	0.8 V to 3.6 V			0.1		0.1	V
		I$_{OL}$ = 1.1 mA	1.1 V			0.3 × V$_{CC}$		0.3 × V$_{CC}$	
		I$_{OL}$ = 1.7 mA	1.4 V			0.31		0.37	
		I$_{OL}$ = 1.9 mA	1.65 V			0.31		0.35	
		I$_{OL}$ = 2.3 mA	2.3 V			0.31		0.33	
		I$_{OL}$ = 3.1 mA				0.44		0.45	
		I$_{OL}$ = 2.7 mA	3 V			0.31		0.33	
		I$_{OL}$ = 4 mA				0.44		0.45	
I$_I$	D or CLK input	V$_I$ = GND to 3.6 V	0 V to 3.6 V			0.1		0.5	µA
I$_{off}$		V$_I$ or V$_O$ = 0 V to 3.6 V	0 V			0.2		0.6	µA
ΔI$_{off}$		V$_I$ or V$_O$ = 0 V to 3.6 V	0 V to 0.2 V			0.2		0.6	µA
I$_{CC}$		V$_I$ = GND or V$_{CC}$ to 3.6 V, I$_O$ = 0	0.8 V to 3.6 V			0.5		0.9	µA
ΔI$_{CC}$		V$_I$ = V$_{CC}$ − 0.6 V,[1] I$_O$ = 0	3.3 V			40		50	µA
C$_i$		V$_I$ = V$_{CC}$ or GND	0 V		1.5				pF
			3.6 V		1.5				
C$_o$		V$_O$ = GND	0 V		3				pF

(1) One input at V$_{CC}$ − 0.6 V, other input at V$_{CC}$ or GND

Product Folder Link(s): *SN74AUP1G80*

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

		V_{CC}	T_A = 25°C	T_A = −40°C to 85°C		UNIT
			TYP	MIN	MAX	
f_{clock}	Clock frequency	0.8 V			20	MHz
		1.2 V ± 0.1 V			80	
		1.5 V ± 0.1 V			120	
		1.8 V ± 0.15 V			160	
		2.5 V ± 0.2 V			220	
		3.3 V ± 0.3 V			260	
t_w	Pulse duration, CLK high or low	0.8 V		5.5		
		1.2 V ± 0.1 V		2.5		
		1.5 V ± 0.1 V		1.5		
		1.8 V ± 0.15 V		1.6		
		2.5 V ± 0.2 V		1.7		
		3.3 V ± 0.3 V		1.9		
t_{su}	Setup time before CLK↑	Data high	0.8 V	3.4	6.7	ns
		1.2 V ± 0.1 V		2.4		
		1.5 V ± 0.1 V		1.2		
		1.8 V ± 0.15 V		0.8		
		2.5 V ± 0.2 V		0.6		
		3.3 V ± 0.3 V		0.4		
		Data low	0.8 V	3.4	8.9	ns
		1.2 V ± 0.1 V		2		
		1.5 V ± 0.1 V		1.3		
		1.8 V ± 0.15 V		1.1		
		2.5 V ± 0.2 V		0.8		
		3.3 V ± 0.3 V		0.7		
t_h	Hold time, data after CLK↑	0.8 V	0	1		ns
		1.2 V ± 0.1 V		0		
		1.5 V ± 0.1 V		0		
		1.8 V ± 0.15 V		0		
		2.5 V ± 0.2 V		0		
		3.3 V ± 0.3 V		0		

Product Folder Link(s): *SN74AUP1G80*

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		91		90		MHz
			1.2 V ± 0.1 V		175		220		
			1.5 V ± 0.1 V		237		230		
			1.8 V ± 0.15 V		269		240		
			2.5 V ± 0.2 V		280		250		
			3.3 V ± 0.3 V		280		260		
t_{pd}	CLK	$\overline{Q}$	0.8 V		17.2				ns
			1.2 V ± 0.1 V	3.2	7.1	14.9	2.7	16.3	
			1.5 V ± 0.1 V	1.9	5	9.8	2.1	10.3	
			1.8 V ± 0.15 V	1.7	3.9	7.6	1.6	8.1	
			2.5 V ± 0.2 V	1.4	2.8	5.3	1.2	5.6	
			3.3 V ± 0.3 V	1.2	2.2	4.1	1	4.4	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		68		70		MHz
			1.2 V ± 0.1 V		128		170		
			1.5 V ± 0.1 V		189		220		
			1.8 V ± 0.15 V		234		240		
			2.5 V ± 0.2 V		273		250		
			3.3 V ± 0.3 V		280		260		
t_{pd}	CLK	$\overline{Q}$	0.8 V		19.4				ns
			1.2 V ± 0.1 V	4.4	8.2	16.2	3.4	17.7	
			1.5 V ± 0.1 V	3.6	5.8	10.7	2.6	11.3	
			1.8 V ± 0.15 V	2.9	4.6	8.4	2.1	3	
			2.5 V ± 0.2 V	2.2	3.3	5.9	1.7	6.3	
			3.3 V ± 0.3 V	1.9	2.7	4.7	1.4	4.9	

Product Folder Link(s): *SN74AUP1G80*

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		52		50		MHz
			1.2 V ± 0.1 V		98		130		
			1.5 V ± 0.1 V		148		180		
			1.8 V ± 0.15 V		196		240		
			2.5 V ± 0.2 V		249		250		
			3.3 V ± 0.3 V		280		260		
t_{pd}	CLK	$\overline{Q}$	0.8 V		21.5				ns
			1.2 V ± 0.1 V	3	9.1	17.4	4.1	19	
			1.5 V ± 0.1 V	3.2	6.5	11.7	3.2	12.3	
			1.8 V ± 0.15 V	2.7	4.2	9.2	2.6	9.8	
			2.5 V ± 0.2 V	2.2	3.8	6.5	2.1	6.9	
			3.3 V ± 0.3 V	1.9	3.1	5.1	1.8	5.5	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		32		20		MHz
			1.2 V ± 0.1 V		71		80		
			1.5 V ± 0.1 V		104		120		
			1.8 V ± 0.15 V		133		160		
			2.5 V ± 0.2 V		181		220		
			3.3 V ± 0.3 V		257		260		
t_{pd}	CLK	$\overline{Q}$	0.8 V		28.4				ns
			1.2 V ± 0.1 V	5.1	11.8	20.7	6.2	28.7	
			1.5 V ± 0.1 V	4.8	8.5	14.1	6.9	16.7	
			1.8 V ± 0.15 V	4	6.9	11.2	2	13.3	
			2.5 V ± 0.2 V	3.3	5.1	7.9	3.2	9.3	
			3.3 V ± 0.3 V	2.9	4.2	6.4	2.8	7.5	

OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	0.8 V	4	pF
			1.2 V ± 0.1 V	4	
			1.5 V ± 0.1 V	4	
			1.8 V ± 0.15 V	4	
			2.5 V ± 0.2 V	4.1	
			3.3 V ± 0.3 V	4.3	

Product Folder Link(s): *SN74AUP1G80*

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Duration)
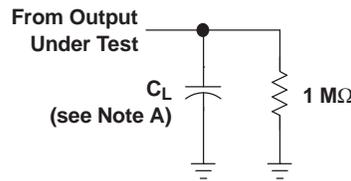
LOAD CIRCUIT

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)
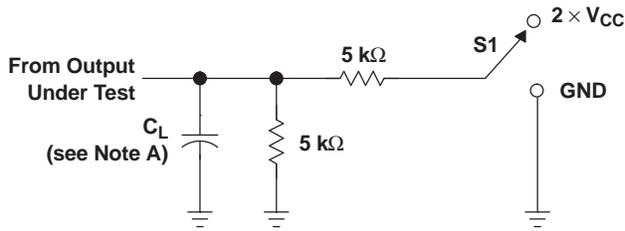
LOAD CIRCUIT

TEST	S1
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

	$V_{CC} = 0.8$ V	$V_{CC} = 1.2$ V ± 0.1 V	$V_{CC} = 1.5$ V ± 0.1 V	$V_{CC} = 1.8$ V ± 0.15 V	$V_{CC} = 2.5$ V ± 0.2 V	$V_{CC} = 3.3$ V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50$ Ω, $t_r/t_f = 3$ ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

Product Folder Link(s): SN74AUP1G80

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74AUP1G80DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H80R	Samples
SN74AUP1G80DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H80R	Samples
SN74AUP1G80DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H80R	Samples
SN74AUP1G80DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H80R	Samples
SN74AUP1G80DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H80R	Samples
SN74AUP1G80DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H80R	Samples
SN74AUP1G80DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HX5, HXF, HXK, HXO, HXR)	Samples
SN74AUP1G80DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HX5, HXF, HXK, HXO, HXR)	Samples
SN74AUP1G80DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HX5, HXF, HXK, HXO, HXR)	Samples
SN74AUP1G80DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HX5, HXO, HXR)	Samples
SN74AUP1G80DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HX5, HXO, HXR)	Samples
SN74AUP1G80DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HX5, HXO, HXR)	Samples
SN74AUP1G80DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HX	Samples
SN74AUP1G80DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HX	Samples
SN74AUP1G80YFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM		(HX2, HXN)	Samples
SN74AUP1G80YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(HX7, HXN)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] Only one of markings shown within the brackets will appear on the physical device.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
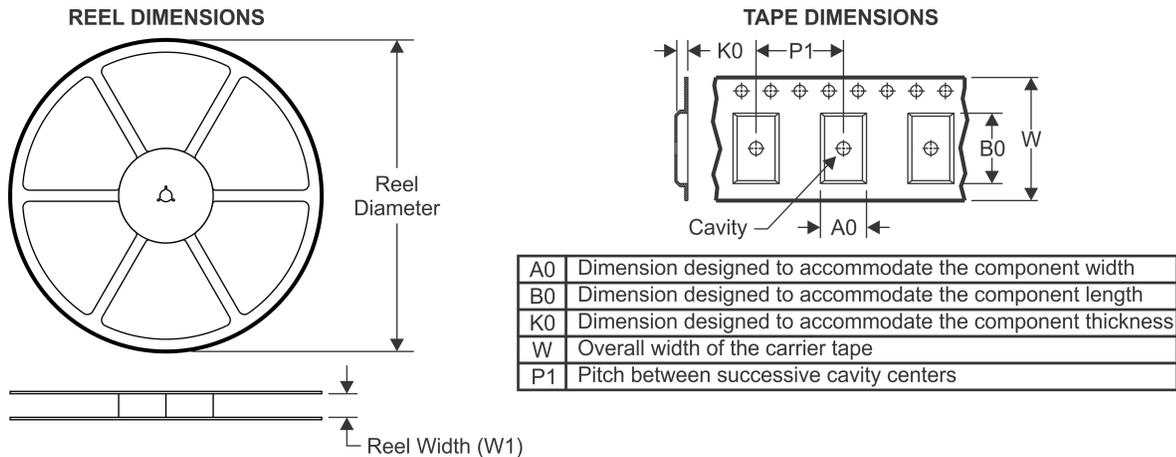
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G80DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G80DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G80DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AUP1G80DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G80DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G80DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G80DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G80YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1G80YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS
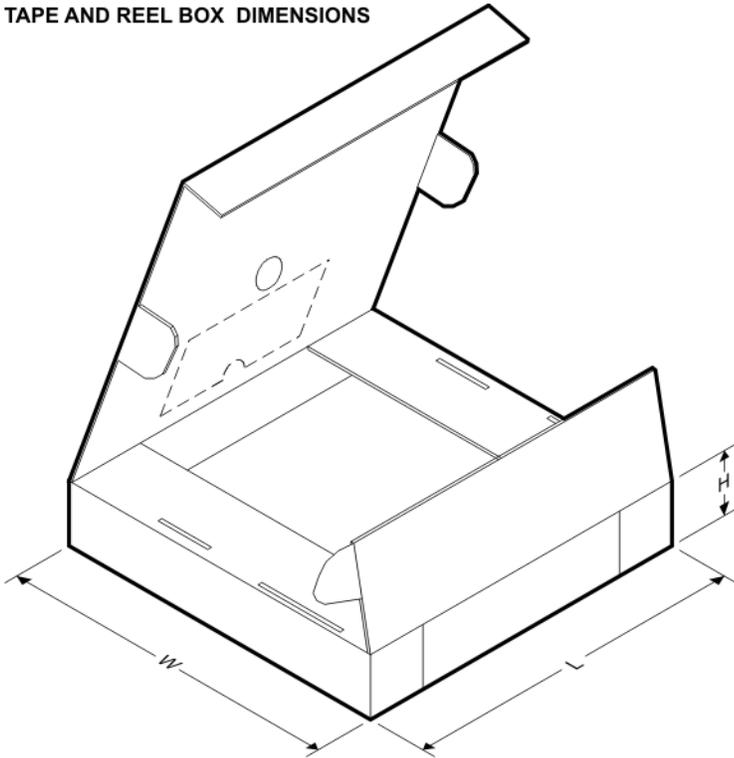
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G80DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G80DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G80DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74AUP1G80DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G80DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G80DRYR	SON	DRY	6	5000	180.0	180.0	30.0
SN74AUP1G80DSFR	SON	DSF	6	5000	180.0	180.0	30.0
SN74AUP1G80YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1G80YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

DBV (R−PDSO−G5)   **PLASTIC SMALL−OUTLINE PACKAGE**
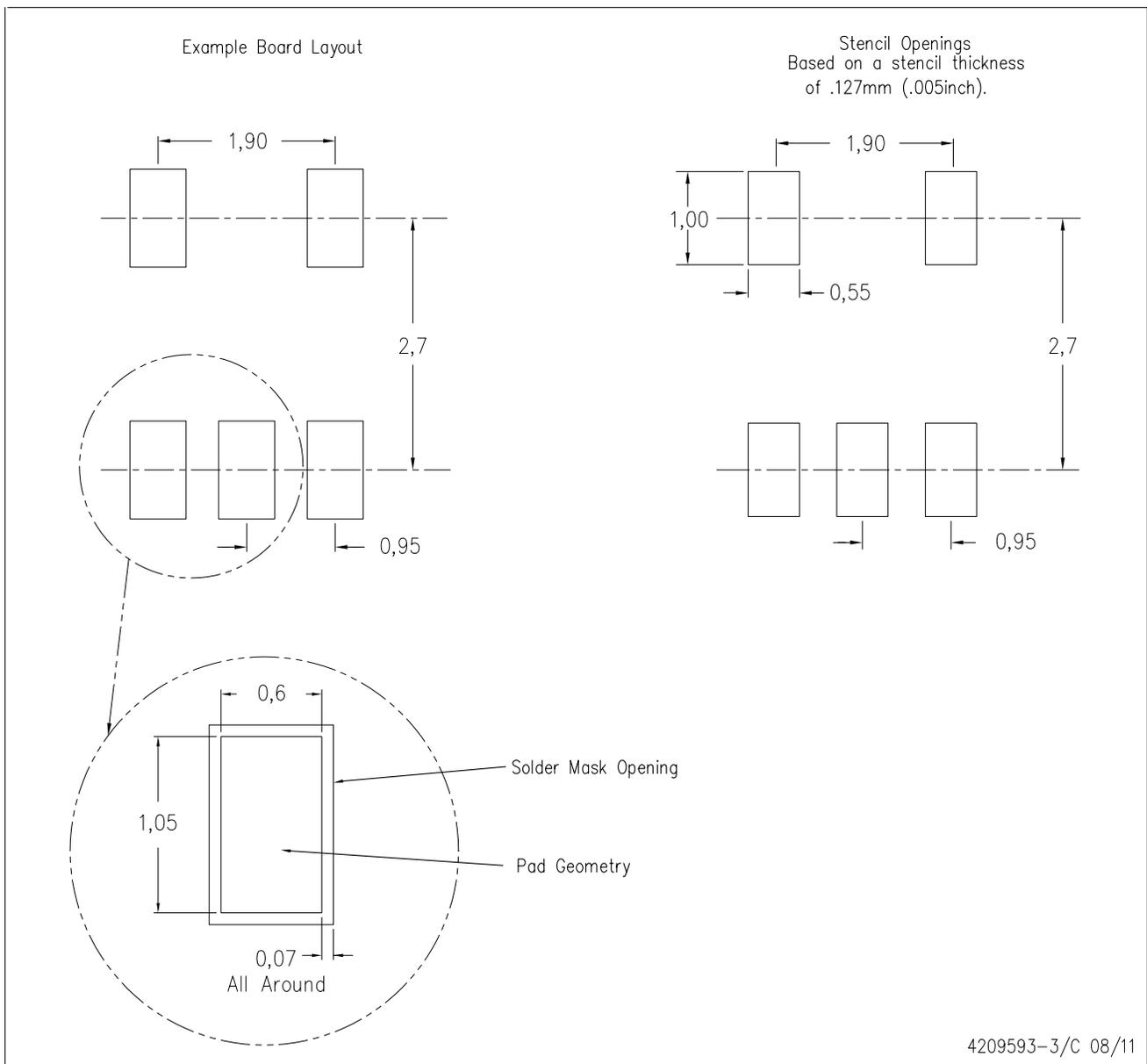
0,95

5X $\frac{0,50}{0,30}$ ⊕ 0,20 Ⓜ

5   4

$\frac{1,75}{1,45}$ $\frac{3,00}{2,60}$

Pin 1
Index Area

1   3

$\frac{3,05}{2,75}$

$\frac{0,22}{0,08}$

Gage Plane

0°−8°

0,25

$\frac{0,55}{0,30}$

1,45 MAX

$\frac{0,15}{0,00}$

Seating Plane

◁ 0,10

4073253−4/K 03/2006

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
          D.   Falls within JEDEC MO−178 Variation AA.

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DBV (R–PDSO–G5)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

1,90

1,90

1,00

0,55

2,7

2,7

0,95

0,95

0,6

Solder Mask Opening

1,05

Pad Geometry

0,07
All Around

4209593–3/C 08/11

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
        D. Publication IPC–7351 is recommended for alternate designs.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
            metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DCK (R−PDSO−G5) PLASTIC SMALL−OUTLINE PACKAGE
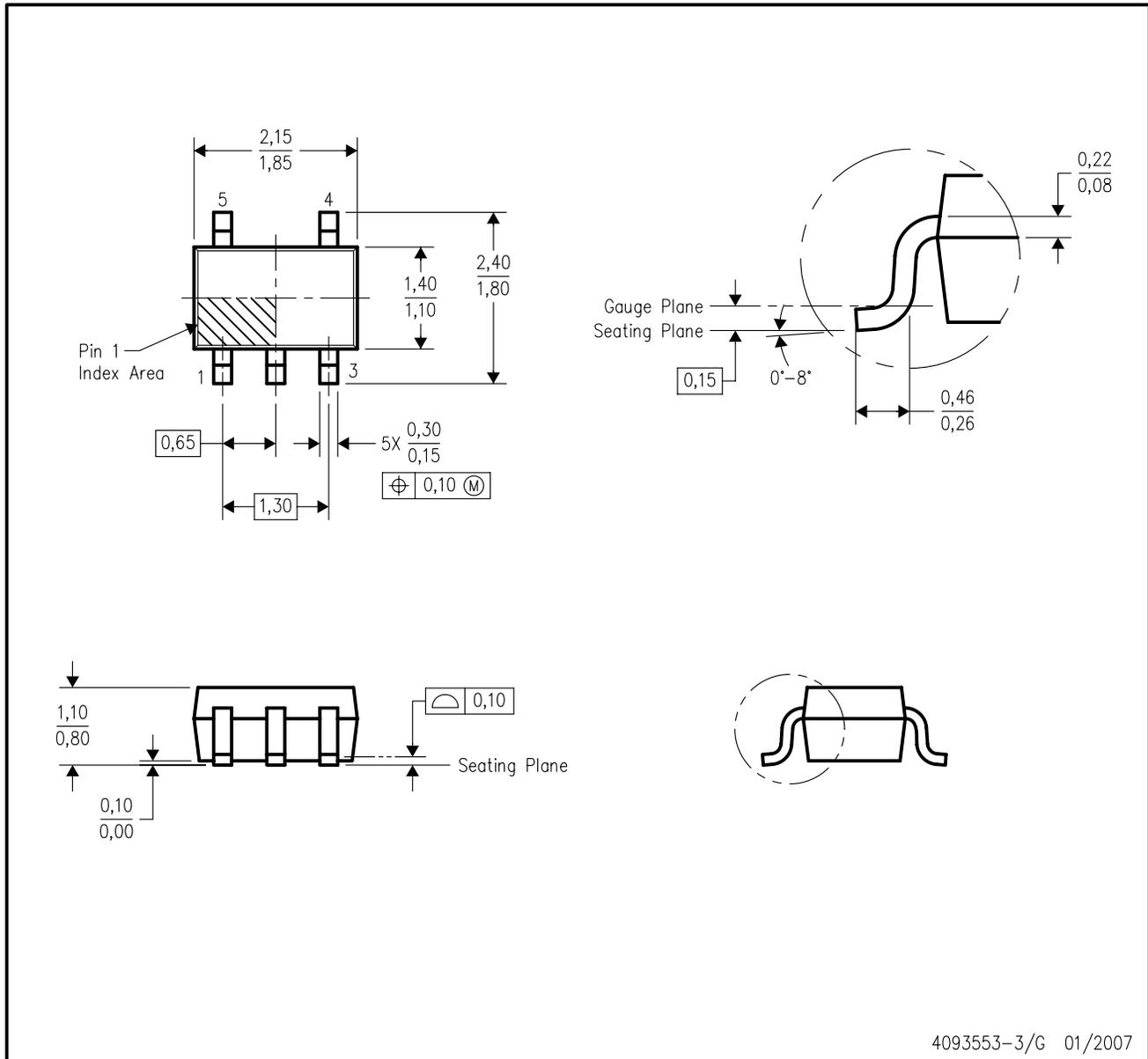
4093553−3/G 01/2007

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO−203 variation AA.

DCK (R−PDSO−G5)   PLASTIC SMALL OUTLINE
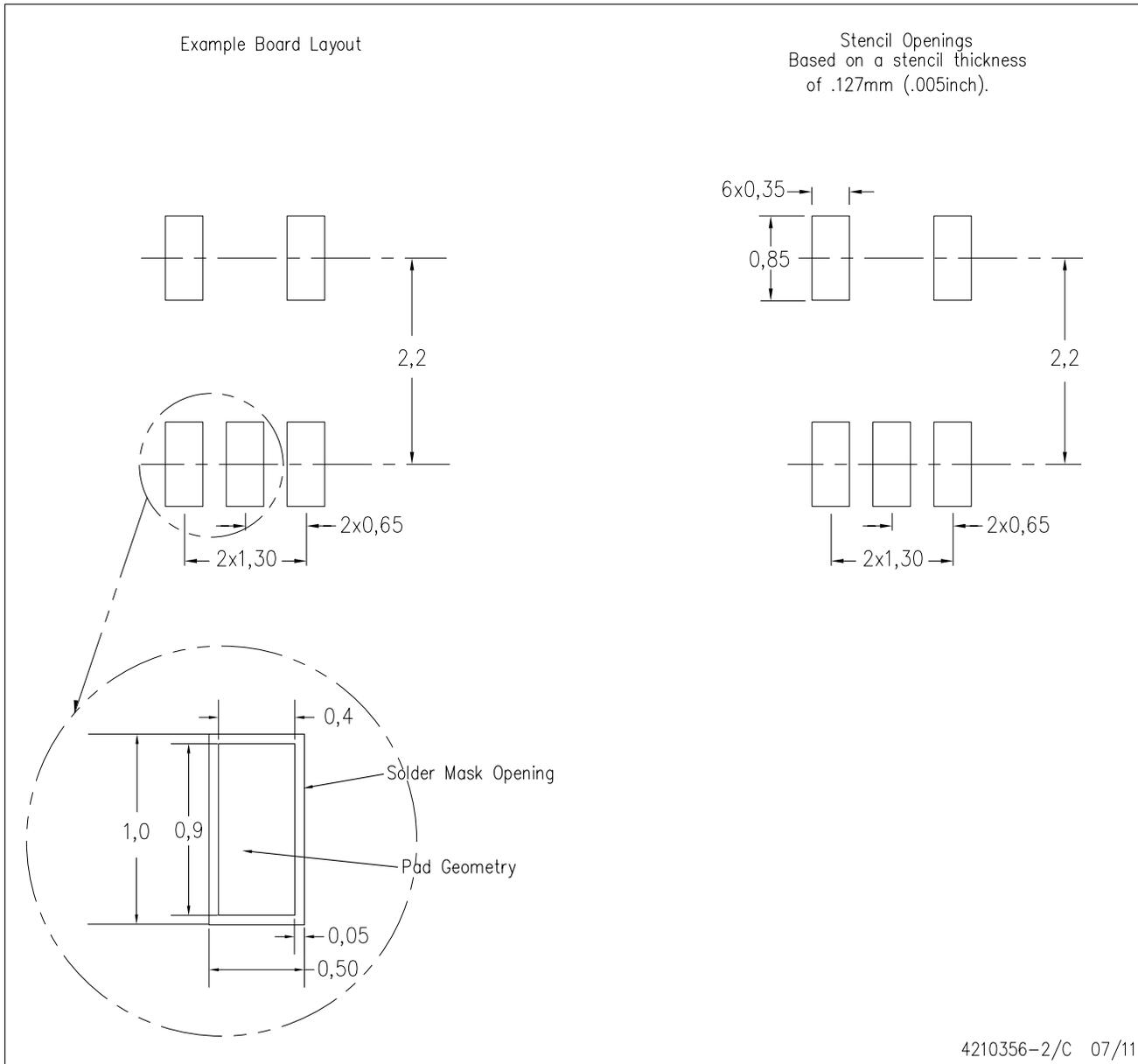
Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

2,2

6x0,35

0,85

2,2

2x0,65

2x1,30

2x0,65

2x1,30

0,4

Solder Mask Opening

1,0   0,9

Pad Geometry

0,05

0,50

4210356−2/C 07/11

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
        D. Publication IPC−7351 is recommended for alternate designs.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
            metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

DRY (R−PUSON−N6)   PLASTIC SMALL OUTLINE NO−LEAD

1,50
1,40
⟦A⟧

⟦B⟧

6   5   4

1,05
0,95

Pin 1 Index Area

1   2   3

0,60
0,51

∥ | 0,05 | C

0,15 Nominal
Lead Frame △D

Seating Plane

⌒ | 0,05 | C

0,05
0,00
Seating Height

⟦C⟧

1,00

0,50

6X 0,10
    0,00

1   2   3

△F Pin 1 Identifier
    Pin shape will be
    modified per device.

5X 0,45
    0,25

5X 0,35
    0,25

6   5   4

6X 0,25
    0,15

⊕ | 0,10 Ⓜ | C | A | B
  | 0,05 Ⓜ | C
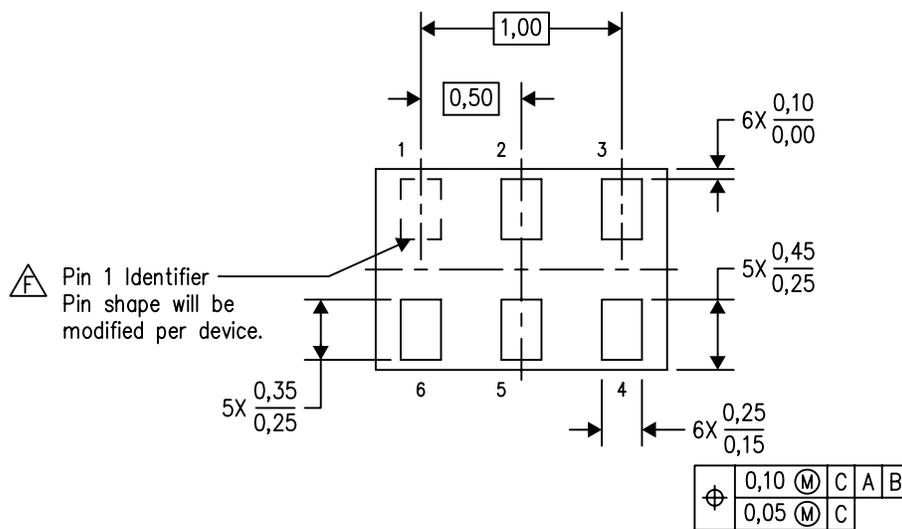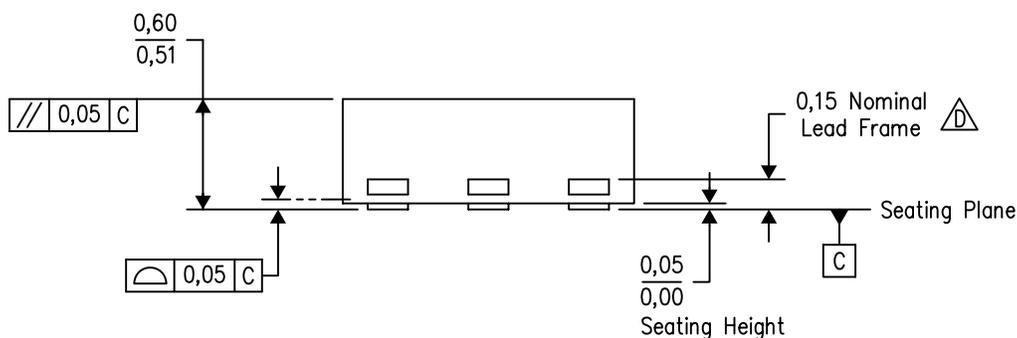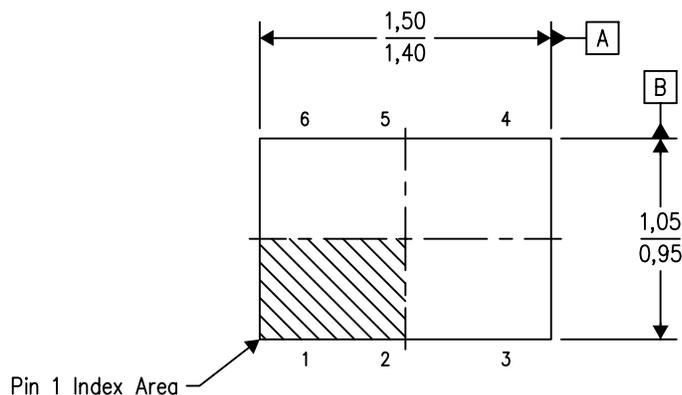
Bottom View

4207181/F   12/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. SON (Small Outline No−Lead) package configuration.
       △D The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
        E. This package complies to JEDEC MO−287 variation UFAD.
       △F See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

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DSF (S−PX2SON−N6)   PLASTIC SMALL OUTLINE NO−LEAD

$\frac{1,05}{0,95}$

A

B

6 5 4

$\frac{1,05}{0,95}$

Pin 1 Index Area

1 2 3

$\frac{0,40}{0,34}$

0,05 C

Seating Plane

$\frac{0,05}{0,00}$

C

Seating Height

0,70

0,35

1 2 3

$\frac{0,13}{0,07}$

6X $\frac{0,45}{0,35}$

Pin 1 Identifier

6 5 4

6X $\frac{0,20}{0,14}$

⊕	0,07 Ⓜ	C	A	B
	0,05 Ⓜ	C		

Bottom View
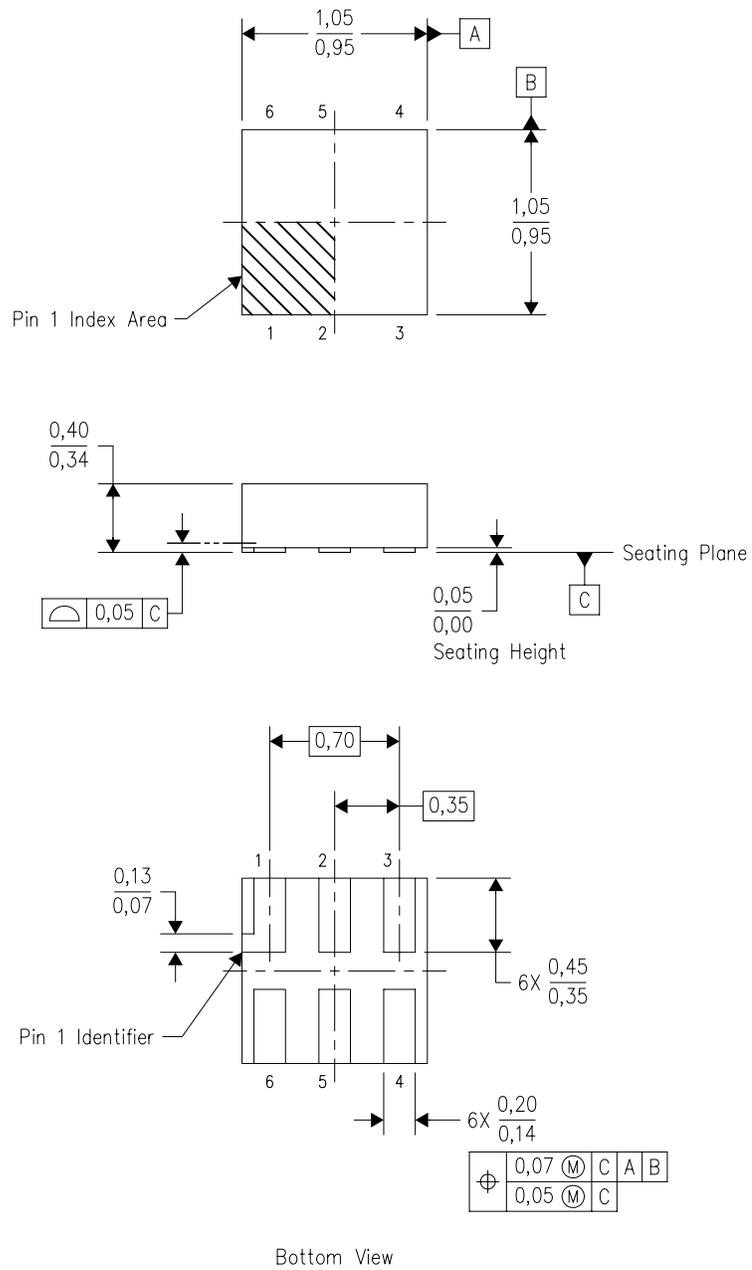
4208186/E   03/11

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   SON (Small Outline No−Lead) package configuration.
         D.   This package complies to JEDEC MO−287 variation X2AAF.

DSF (S-PX2SON-N6)   PLASTIC SMALL OUTLINE NO-LEAD

Land Pattern   Stencil Pattern

0.20   0.165

0.35   0.35

0.53   0.53

0.15   1.20   0.15   1.20

0.70   0.70

Contact your PCB vendor for
allowable Solder Mask clearance (Notes C, D.)

0.53

0.20
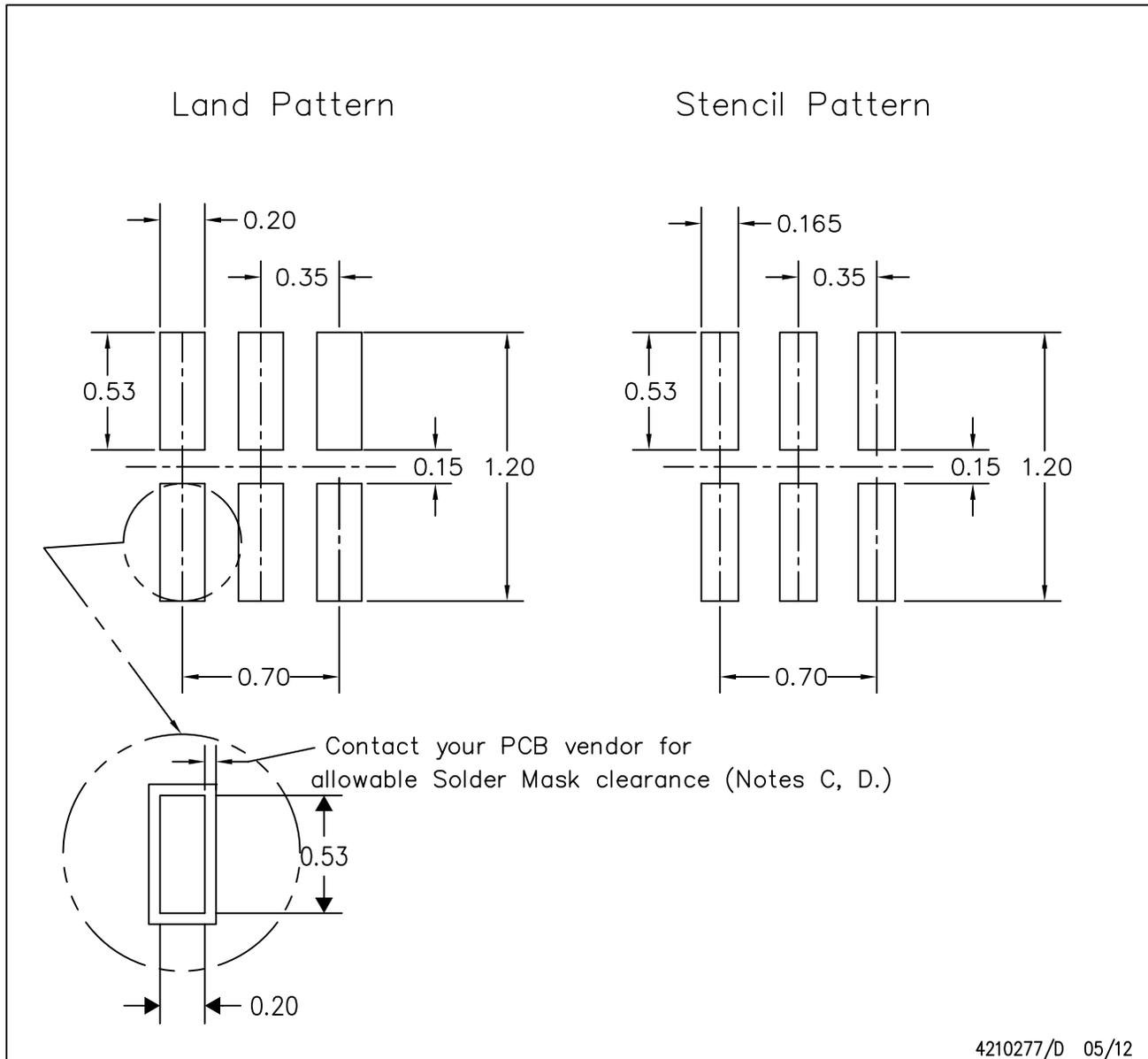
4210277/D 05/12

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC-7351 is recommended for alternate designs.
         D.   Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
              If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
         E.   Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
         F.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
         G.   Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
         H.   Component placement force should be minimized to prevent excessive paste block deformation.

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YZP (R−XBGA−N5)   DIE−SIZE BALL GRID ARRAY
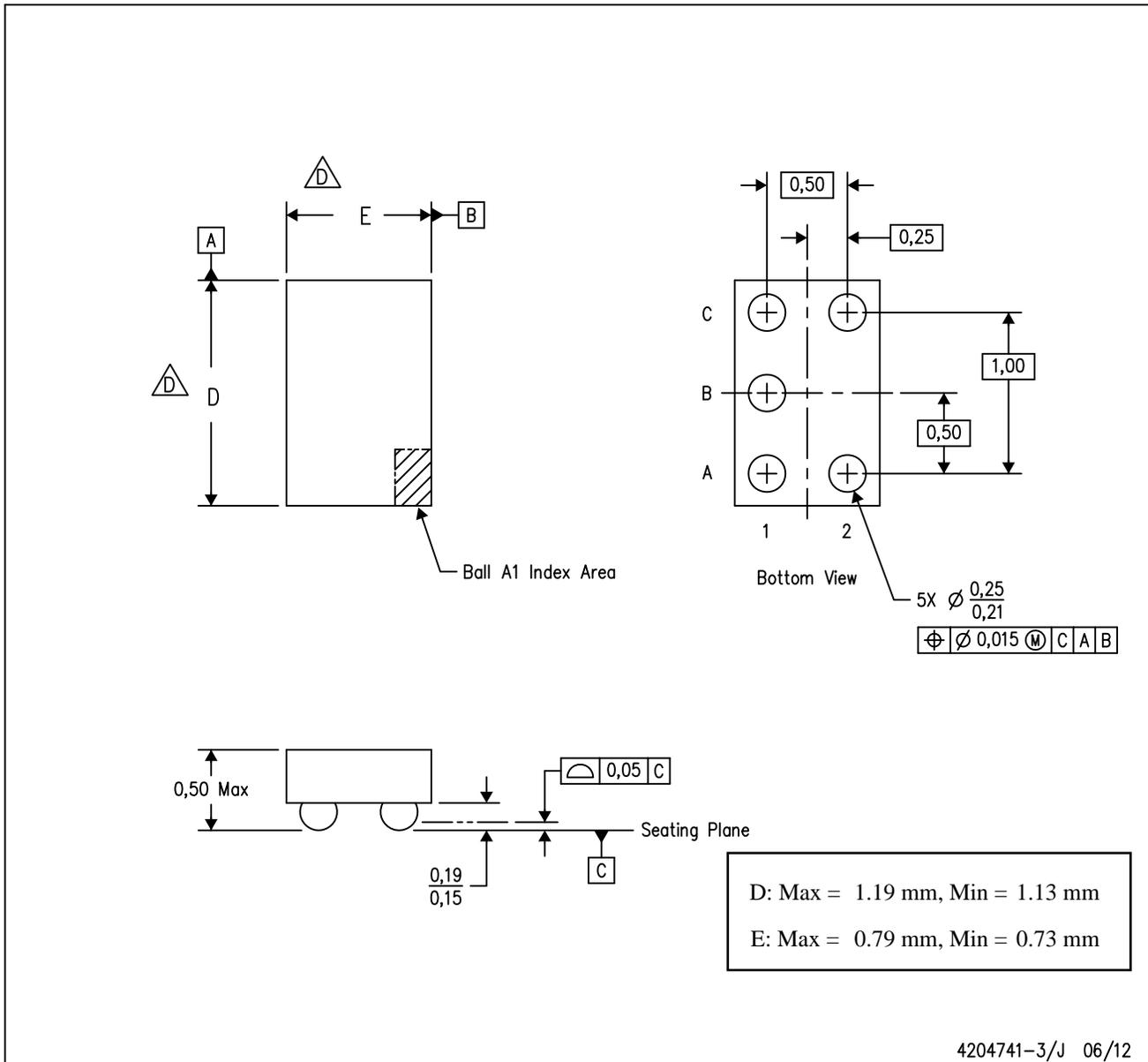
Ball A1 Index Area

Bottom View

0,50

0,25

1,00

0,50

5X Ø $\frac{0,25}{0,21}$

⊕ Ø 0,015 Ⓜ C A B

0,50 Max

0,05 C

Seating Plane

$\frac{0,19}{0,15}$

C

D: Max = 1.19 mm, Min = 1.13 mm

E: Max = 0.79 mm, Min = 0.73 mm

4204741−3/J 06/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B. This drawing is subject to change without notice.
         C. NanoFree™ package configuration.
         D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version
             of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
         E. This package is a Pb−free solder ball design. Refer to the 5 YEP package (drawing 4204725) for tin−lead (SnPb).

NanoFree is a trademark of Texas Instruments.

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YFP (R−XBGA−N6)   DIE−SIZE BALL GRID ARRAY

Ball A1 Index Area

0,40

0,20

C

B

A

1   2

0,80

0,40

Bottom View

6X Ø $\frac{0,25}{0,21}$

⊕ Ø 0,015 Ⓜ C A B

A

E   B

D

D

0,50 Max

0,05 C

Seating Plane

$\frac{0,19}{0,13}$

C

D: Max = 1.19 mm, Min = 1.13 mm

E: Max = 0.79 mm, Min = 0.73 mm
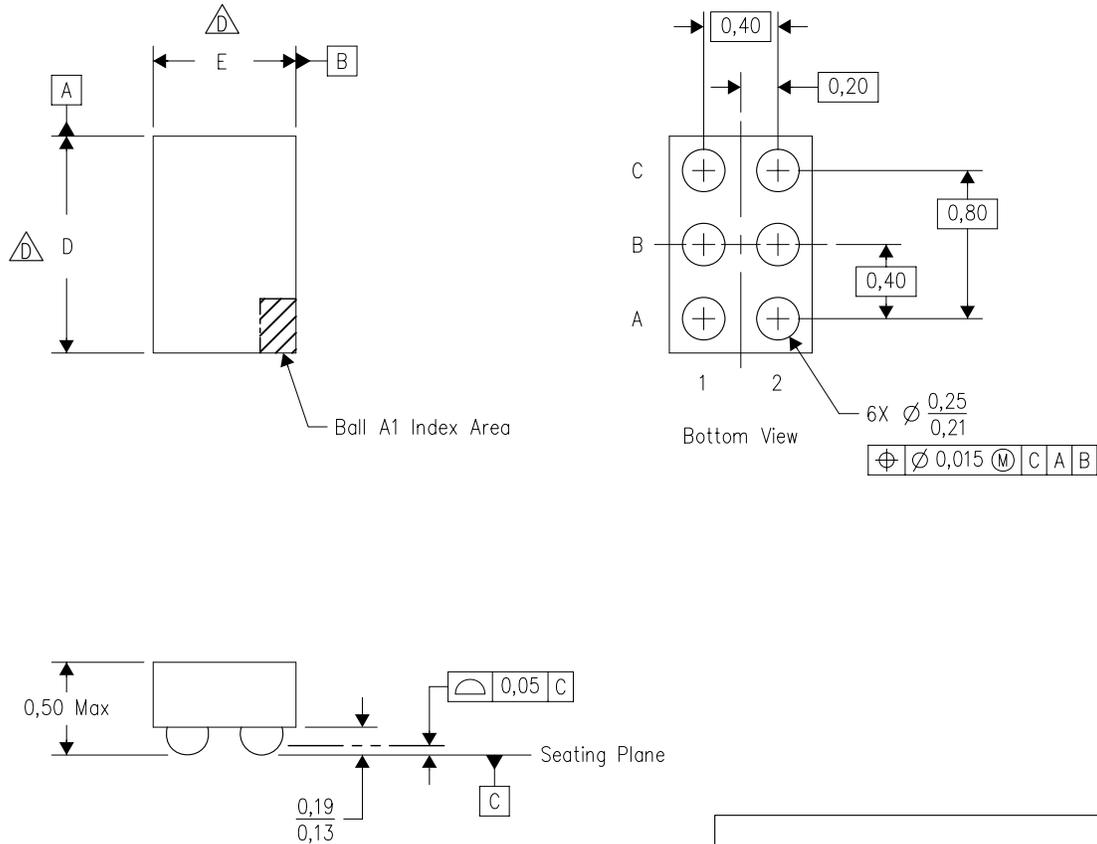
4206986−3/R 02/12

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
          C.   NanoFree™ package configuration.
          D.   The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version
               of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
          E.   Reference Product Data Sheet for array population.
               2 x 3 matrix pattern is shown for illustration only.
          F.   This package contains Pb−free balls.

NanoFree is a trademark of Texas Instruments

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