SCES410C - AUGUST 2002 - REVISED DECEMBER 2002

- Member of the Texas Instruments
 Widebus+™ Family
- Optimized for 1.8-V Operation and is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub 1-V Operable
- Max t_{pd} of 2 ns at 1.8 V

- Low Power Consumption, 40-μA Max I_{CC}
- ◆ ±8-mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

This 32-bit noninverting bus transceiver is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUC32245 is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as four 8-bit transceivers, two 16-bit transceivers, or one 32-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKE	Tape and reel	SN74AUC32245GKER	MM245

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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Widebus+ is a trademark of Texas Instruments.



SN74AUC32245 32-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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GKE PACKAGE (TOP VIEW)

		1	2	3	4	5	6
Α	/	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\circ
В		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
С		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
D		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
Е		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
F		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
G		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
н		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
J		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
κ		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
L		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
М		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
N		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
Р		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
R		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
T		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
	1						/

terminal assignments

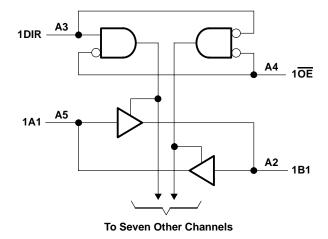
	1	2	3	4	5	6
Α	1B2	1B1	1DIR	10E	1A1	1A2
В	1B4	1B3	GND	GND	1A3	1A4
С	1B6	1B5	Vcc	Vcc	1A5	1A6
D	1B8	1B7	GND	GND	1A7	1A8
Ε	2B2	2B1	GND	GND	2A1	2A2
F	2B4	2B3	Vcc	Vcc	2A3	2A4
G	2B6	2B5	GND	GND	2A5	2A6
н	2B7	2B8	2DIR	2OE	2A8	2A7
J	3B2	3B1	3DIR	3OE	3A1	3A2
K	3B4	3B3	GND	GND	3A3	3A4
L	3B6	3B5	Vcc	Vcc	3A5	3A6
M	3B8	3B7	GND	GND	3A7	3A8
N	4B2	4B1	GND	GND	4A1	4A2
Р	4B4	4B3	Vcc	Vcc	4A3	4A4
R	4B6	4B5	GND	GND	4A5	4A6
T	4B7	4B8	4DIR	4OE	4A8	4A7

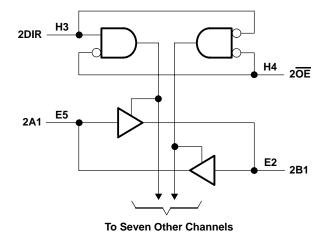
FUNCTION TABLE (each 8-bit section)

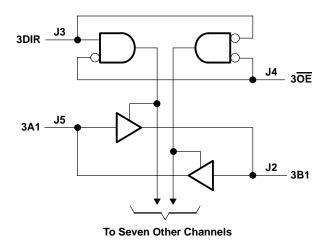
INP	UTS	OPERATION				
OE	DIR	OPERATION				
L	L	B data to A bus				
L	Н	A data to B bus				
Н	X	Isolation				

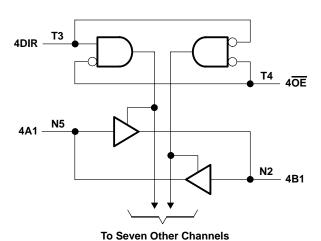


logic diagram (positive logic)









absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	–0.5 V to 3.6 V
Input voltage range, V _I (see Note 1)	–0.5 V to 3.6 V
Voltage range applied to any output in the high-impedance or power-off state, V	O
(see Note 1)	–0.5 V to 3.6 V
Output voltage range, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±20 mA
Continuous current through V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 2)	40°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
Vcc	Supply voltage		0.8	2.7	V
		V _{CC} = 0.8 V	Vcc		
ViH	High-level input voltage	V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 0.8 V		0	
٧ _{IL}	Low-level input voltage	V _{CC} = 1.1 V to 1.95 V		0.35 × V _{CC}	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
٧ı	Input voltage		0	3.6	V
\/-	Output valtage	Active state	0	Vcc	V
۷o	Output voltage	3-state	0	3.6	V
		V _{CC} = 0.8 V		-0.7	
		V _{CC} = 1.1 V		-3	
loн	High-level output current	V _{CC} = 1.4 V		- 5	mA
	3-state V _{CC} = 0.8 V V _{CC} = 1.1 V V _{CC} = 1.4 V V _{CC} = 1.65 V V _{CC} = 2.3 V V _{CC} = 0.8 V V _{CC} = 0.8 V V _{CC} = 0.8 V V _{CC} = 0.8 V V _{CC} = 0.8 V V _{CC} = 0.8 V V _{CC} = 0.8 V V _{CC} = 0.8 V			-8	
		V _{CC} = 2.3 V		-9	
		V _{CC} = 0.8 V		0.7	
		V _{CC} = 1.1 V		3	
lOL	Low-level output current	V _{CC} = 1.4 V		5	mA
		V _{CC} = 1.65 V		8	
		V _{CC} = 2.3 V		9	
Δt/Δν	Input transition rise or fall rate			5	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		VCC	MIN	TYP†	MAX	UNIT
	$I_{OH} = -100 \mu\text{A}$		0.8 V to 2.7 V	V _{CC} -0.	1		
	$I_{OH} = -0.7 \text{ mA}$		0.8 V		0.55		
l vou	$I_{OH} = -3 \text{ mA}$		1.1 V	0.8			V
VOH	$I_{OH} = -5 \text{ mA}$		1.4 V	1			V
	$I_{OH} = -8 \text{ mA}$		1.65 V	1.2			
	I _{OH} = -9 mA		2.3 V	1.8			
	I _{OL} = 100 μA		0.8 V to 2.7 V			0.2	
	$I_{OL} = 0.7 \text{ mA}$		0.8 V		0.25		
l va	I _{OL} = 3 mA		1.1 V			0.3	V
VOL	I _{OL} = 5 mA		1.4 V			0.4	V
	I _{OL} = 8 mA		1.65 V			0.45	
	I _{OL} = 9 mA		2.3 V			0.6	
I _I All inputs	$V_I = V_{CC}$ or GND		0 to 2.7 V			±5	μΑ
l _{off}	V_I or $V_O = 2.7 V$		0			±10	μΑ
loz [‡]	$V_O = V_{CC}$ or GND		2.7 V			±10	μΑ
Icc	$V_I = V_{CC}$ or GND,	= 0	0.8 V to 2.7 V			40	μΑ
Ci	V _I = V _{CC} or GND		2.5 V		3		pF
C _{iO}	$V_O = V_{CC}$ or GND		2.5 V		7		pF

[†] All typical values are at $T_A = 25$ °C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	FROM TO (INPUT) (OUTPUT)		V _{CC} =		V _{CC} =	: 1.5 V 1 V		C = 1.8 0.15 V		V _{CC} =	2.5 V 2 V	UNIT
	(INFOT)	(001F01)	TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t _{pd}	A or B	B or A	5.6	0.5	3.1	0.5	2	0.5	1.5	2	0.4	1.9	ns
t _{en}	ŌĒ	A or B	10	0.7	4.6	0.7	3.1	0.7	2.1	3.1	0.7	2.6	ns
^t dis	ŌĒ	A or B	12.8	0.8	6.8	0.8	5	0.8	3.4	4.8	0.5	2.9	ns

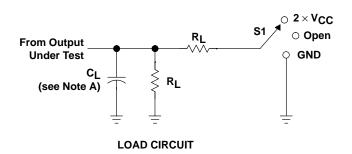
operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST	V _{CC} = 0.8 V	V _{CC} = 1.2 V	V _{CC} = 1.5 V	V _{CC} = 1.8 V	V _{CC} = 2.5 V	UNIT	
	FARAMETER		CONDITIONS	TYP	TYP	TYP	TYP	TYP	ONIT
Cont	Power	Outputs enabled	f = 10 MHz	22	23	24	25	29	pF
Ора	C _{pd} dissipation capacitance	Outputs disabled	1 = 10 WHZ	1	1	1	1	1	рг



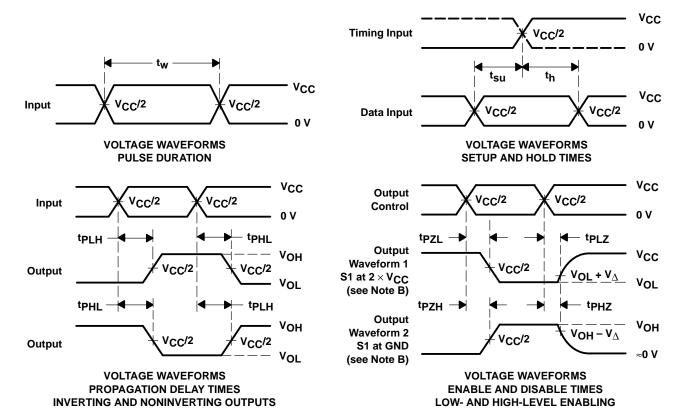
[‡] For I/O ports, the parameter IOZ includes the input leakage current.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	2×V _{CC}
tPHZ/tPZH	GND

Vcc	CL	RL	$v_{\scriptscriptstyle\Delta}$
0.8 V	15 pF	2 k Ω	0.1 V
1.2 V \pm 0.1 V	15 pF	2 k Ω	0.1 V
1.5 V \pm 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V \pm 0.15 V	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	30 pF	500 Ω	0.15 V



NOTES: A. C_L includes probe and jig capacitance.

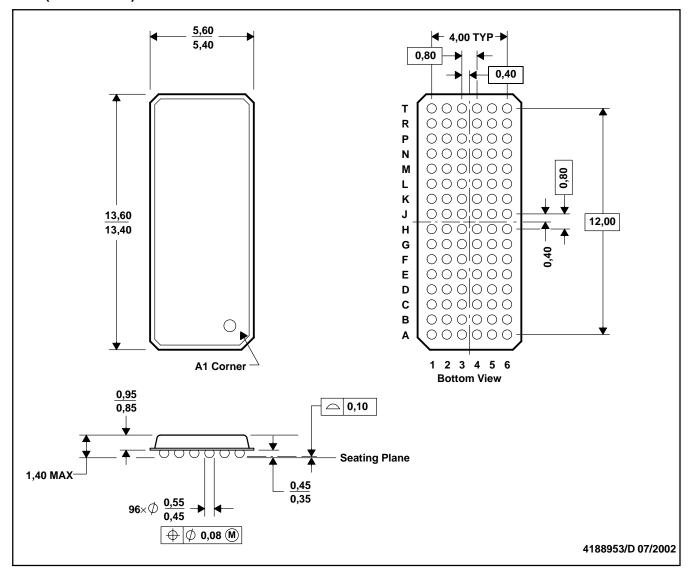
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, slew rate \geq 1 V/ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



GKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MicroStar BGA™ configuration
 - D. Falls within JEDEC MO-205 variation CC.
 - E. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

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