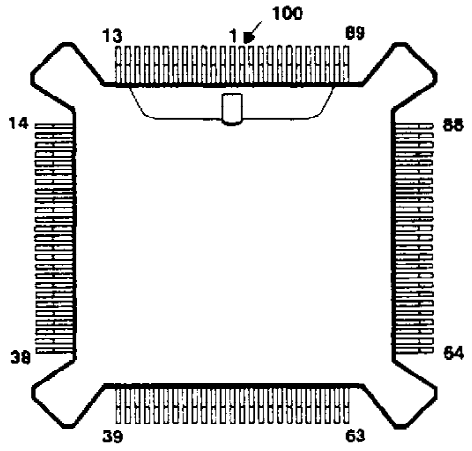
SN74BCT2425
MCP NuBus™ ADDRESS/DATA REGISTERED TRANSCEIVER

SDIS011B D3361, FEBRUARY 1990–REVISED JANUARY 1991

- **Designed to Support Apple Computer Macintosh Coprocessor Platform (MCP) Interface Applications**
- **Designed to Operate with the SN74ACT2441 MCP NuBus™ Interface Controller**
- **Includes NuBus™ Address and Data Path Circuitry Along with Memory Address Drivers**
- **Conforms to Apple Computer Macintosh II Family NuBus™ Interface Specifications**
- **BiCMOS Design Substantially Reduces Standby Current**
- **Available in 100-pin Plastic Quad Flat Package**

PQ PACKAGE
(TOP VIEW)



description

The SN74BCT2425 consists of bus transceiver circuits, D-type flip-flops, memory drivers, and control circuitry arranged for multiplexed transmission of address and data information in Macintosh Coprocessor Platform (MCP) applications.

The MCP is a generic software and hardware foundation developed by Apple Computer and may be used in the development of add-in cards and software applications for the Macintosh II computer.

The MCP provides an intelligent NuBus™ interface that includes hardware support for an MC68000 processor, an application specific I/O processor, ROM, and dynamic memory. Software support for the MCP architecture consists of the A/ROSE operating system (Apple Real-time Operating System Enviroment). A/ROSE is downloaded onto the Macintosh II I/O card for execution by the on-board MC68000.

For a complete description of the Apple Macintosh NuBus™ implementation, see *Designing Cards and Drivers for Macintosh II and Macintosh SE* published by Addison Wesley, or contact the Apple Programmers and Developers Association (APDA). For additional information on MCP or A/ROSE, contact Apple Computer directly.

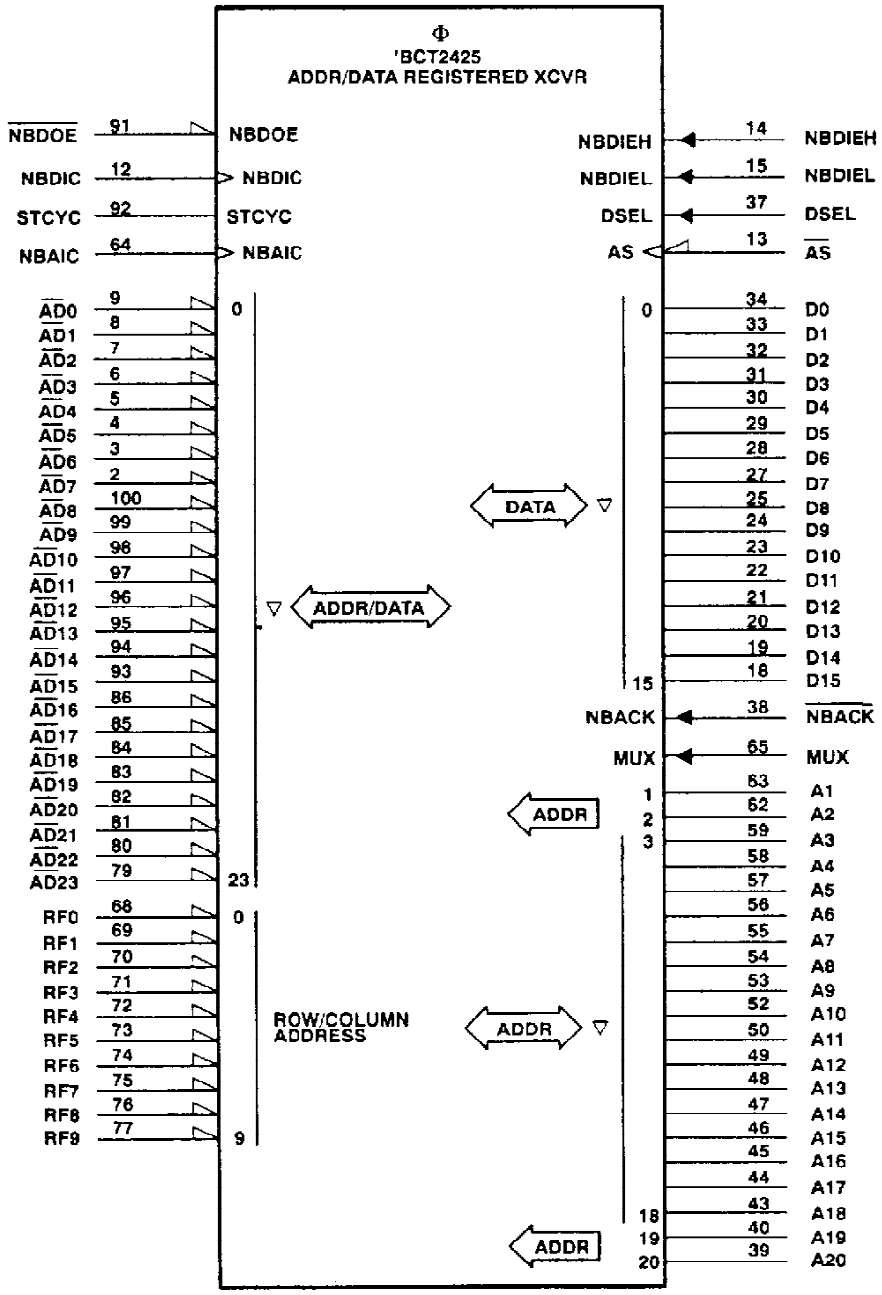
The SN74BCT2425 is characterized for operation from 0°C to 70°C.

NuBus is a trademark of Texas Instruments Incorporated.

Pin Assignments

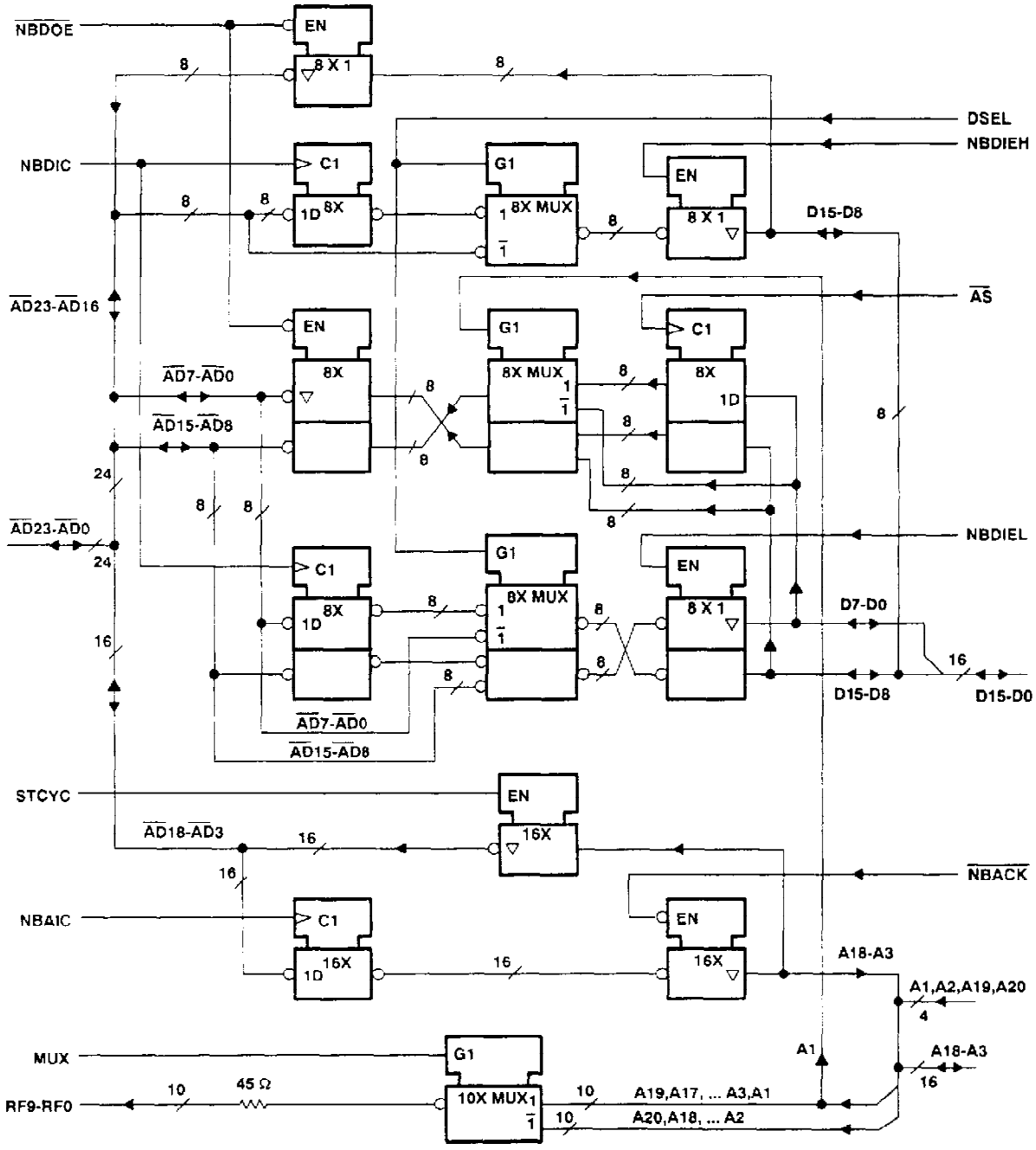
PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	GND	21	D12	41	V_{CC}	61	V_{CC}	81	$\overline{AD}21$
2	$\overline{AD}7$	22	D11	42	GND	62	A2	82	$\overline{AD}20$
3	$\overline{AD}6$	23	D10	43	A18	63	A1	83	$\overline{AD}19$
4	$\overline{AD}5$	24	D9	44	A17	64	NBAIC	84	$\overline{AD}18$
5	$\overline{AD}4$	25	D8	45	A16	65	MUX	85	$\overline{AD}17$
6	$\overline{AD}3$	26	GND	46	A15	66	V_{CC}	86	$\overline{AD}16$
7	$\overline{AD}2$	27	D7	47	A14	67	GND	87	GND
8	$\overline{AD}1$	28	D6	48	A13	68	RF0	88	V_{CC}
9	$\overline{AD}0$	29	D5	49	A12	69	RF1	89	V_{CC}
10	GND	30	D4	50	A11	70	RF2	90	GND
11	V_{CC}	31	D3	51	GND	71	RF3	91	$\overline{NBDOE}$
12	NBDIC	32	D2	52	A10	72	RF4	92	STCYC
13	$\overline{AS}$	33	D1	53	A9	73	RF5	93	$\overline{AD}15$
14	NBDIEH	34	D0	54	A8	74	RF6	94	$\overline{AD}14$
15	NBDIEL	35	GND	55	A7	75	RF7	95	$\overline{AD}13$
16	V_{CC}	36	V_{CC}	56	A6	76	RF8	96	$\overline{AD}12$
17	GND	37	DSEL	57	A5	77	RF9	97	$\overline{AD}11$
18	D15	38	$\overline{NBACK}$	58	A4	78	GND	98	$\overline{AD}10$
19	D14	39	A20	59	A3	79	$\overline{AD}23$	99	$\overline{AD}9$
20	D13	40	A19	60	GND	80	$\overline{AD}22$	100	$\overline{AD}8$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

logic diagram



TERMINAL FUNCTIONS

PIN NAME	DESCRIPTION
A20–A1	Local Address Bus. This 20-bit I/O port directly interfaces to the local address bus A23-A0.
$\overline{AD}23$-$\overline{AD}0$	Address/Data Port. This 24-bit active low I/O port directly interfaces to the NuBus™ address/data lines. These lines are multiplexed to carry address at the beginning of a NuBus™ cycle, and data information in the last portion of the NuBus™ cycle.
$\overline{AS}$	Address Strobe. This input is used for saving data information on the low-to-high transition of $\overline{AS}$. The $\overline{AS}$ input is typically connected to both the 'ACT2441 and the MC6800.
D15–D0	Data Address Bus. This 16-bit I/O port directly interfaces to the local data bus.
DSEL	Data Select. This input controls the data multiplexer for the local data bus. When this input is driven low, the NuBus™ addresses $\overline{AD}23$-$\overline{AD}0$ are selected as inputs to the output data buffer. When DSEL is driven high, the NuBus™ data saved in the data input registers are selected as inputs to the output data buffer.
MUX	Multiplex Row/Column Addresses. This input is used to select between row and column addresses when reading or writing to memory. This signal is driven by the 'ACT2441.
$\overline{NBACK}$	NuBus™ Acknowledge. This active-low input is used to enable NuBus™ address information, saved via the NBAIC input, onto the local A20-A1 address lines.
NBAIC	NuBus™ Address Input Clock. This input is used for saving the address portion of NuBus™ read or write cycles. Data present at the $\overline{AD}18$-$\overline{AD}3$ I/O port is clocked into the address register on the low-to-high transition of NBAIC.
NBDIC	NuBus™ Data Input Clock. This input is used for saving the data portion of NuBus™ read or write cycles. Data present at the $\overline{AD}23$-$\overline{AD}0$ I/O port is clocked into the data registers on the low-to-high transition of NBDIC.
NBDIEL	NuBus™ Data Input Enable Low. This active-high input is used to enable NuBus™ data information onto the local bus (D15-D0) for the lower 16-bits corresponding to $\overline{AD}15$-$\overline{AD}0$.
NBDIEH	NuBus™ Data Input Enable High. This active-high input is used to enable NuBus™ data information onto the local bus (D15-D8) for the upper 8-bits corresponding to $\overline{AD}23$-$\overline{AD}16$. The remaining 8-bits D7-D0, corresponding to $\overline{AD}31$-$\overline{AD}24$, are supplied by the 'ACT2441.
$\overline{NBDOE}$	NuBus™ Data Output Enable. This active-low input is used to enable the $\overline{AD}23$-$\overline{AD}0$ outputs. When $\overline{NBDOE}$ is taken inactive (high), the $\overline{AD}23$-$\overline{AD}0$ outputs are at high impedance (assuming STCYC is also inactive).
RF0-RF9	Memory Row/Column Addresses. These outputs are used for driving row and column address information onto the DRAM address bus. Each output has an internal 45-Ω resistor in series with the output pin for the purpose of supressing signal overshoot and undershoot.
STCYC	Start Cycle Active. This active-high input is used to enable the local bus address lines A18-A3 onto the NuBus™ $\overline{AD}18$-$\overline{AD}3$ bus lines. The remainder of the 24-bit address lines are driven directly from the 'ACT2441 MCP NuBus™ controller. When STCYC is taken inactive (low), the $\overline{AD}18$-$\overline{AD}3$ outputs are at high impedance.

Function Tables

DATA BUS PORT MODE

CONTROL INPUTS				DATA INPUTS			OUTPUTS	
DSEL	NBDIC	NBDIEL	NBDIEH	AD23-AD16	AD15-AD8	AD7-AD0	D15-D8	D7-D0
X	X	L	L	X	X	X	Z	Z
L	X	L	H	L	X	X	H	Z
				H	X	X	L	Z
L	X	H	L	X	H	L	H	L
				X	L	H	L	H
L	X	H	H	Unallowed input condition				
H	↑	L	H	L	X	X	H	Z
				H	X	X	L	Z
	No↑			X	X	X	NC	Z
H	↑	H	L	X	H	L	H	L
				X	L	H	L	H
	No↑			X	X	X	NC	NC
H	X	H	H	Unallowed input condition				

Inputs $\overline{AD}$15-$\overline{AD}$8 map to outputs D7-D0, and inputs $\overline{AD}$7-$\overline{AD}$0 map to outputs D15-D8, respectively, in the applicable mode.
Inputs $\overline{AD}$23-$\overline{AD}$16 map to outputs D15-D8, respectively, in the applicable mode.

NuBus™ PORT OUTPUT MODE

CONTROL INPUTS				DATA INPUTS			OUTPUTS			
A1	$\overline{AS}$	$\overline{NBDOE}$	STCYC	A18-A3	D15-D8	D7-D0	$\overline{AD}$23-$\overline{AD}$19	$\overline{AD}$18-$\overline{AD}$16	$\overline{AD}$15-$\overline{AD}$3	$\overline{AD}$2-$\overline{AD}$0
X	X	H	L	X	X	X	Z	Z	Z	Z
L	X	H	H	L	X	X	Z	H	H	Z
				H	X	X	Z	L	L	Z
L	X	L	L	X	L	L	H	H	H	H
				X	H	H	L	L	L	L
L	X	L	H	Unallowed input condition						
H	X	H	H	L	X	X	Z	H	H	Z
				H	X	X	Z	L	L	Z
H	↑	L	L	X	L	L	H	H	H	H
				X	H	H	L	L	L	L
H	No↑	L	L	X	L	L	H	H	NC	NC
				X	H	H	L	L	NC	NC
H	X	L	H	Unallowed input condition						

Inputs A18-A3 map to outputs $\overline{AD}$18-$\overline{AD}$3, respectively in the applicable mode.
Inputs D15-D8 map to outputs $\overline{AD}$23-$\overline{AD}$16, respectively in the applicable mode.
Inputs D7-D0 map to outputs $\overline{AD}$15-$\overline{AD}$8, and inputs D15-D8 map to outputs $\overline{AD}$7-$\overline{AD}$0, respectively in the applicable mode
H denotes a high level, L denotes a low level, Z denotes a high-impedance state, ↑ denotes a low-to-high logic level transition, NC denotes no change, and X denotes a level that does not affect the result.

Function Tables

MEMORY DRIVER PORT

CONTROL	DATA INPUTS		OUTPUTS
MUX	A20, A18, A16, A14, A12, A10, A8, A6, A4, A2	A19, A17, A15, A13, A11, A9, A7, A5, A3, A1	RF9-RF0
L	L	X	H
	H	X	L
H	X	L	H
	X	H	L

Inputs A20, A18, A16, A14, A12, A10, A8, A6, A4, A2 map to outputs RF9-RF0, respectively.
Inputs A19, A17, A15, A13, A11, A9, A7, A5, A3, A1 map to outputs RF9-RF0, respectively.

ADDRESS PORT OUTPUT MODE

CONTROL		DATA INPUTS	OUTPUTS
NBAIC	$\overline{\text{NBACK}}$	$\overline{\text{AD18}}$-$\overline{\text{AD3}}$	A18–A3
X	H	X	Z
↑	L	L	H
↑		H	L
No ↑		X	NC

Inputs $\overline{\text{AD18}}$-$\overline{\text{AD3}}$ map to A18-A3, respectively.
H denotes a high level, L denotes a low level, Z denotes a high-impedance state, ↑ denotes a low-to-high logic level transition, NC denotes no change, and X denotes a level that does not affect the result.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage range, V_I . . . . . 5.5 V
Operating free-air temperature, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminal.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current	Ax, Dx, $\overline{\text{ADx}}$, outputs			24	mA
		RFx outputs			12	
t_w	Pulse duration	Clocks high	12.5			ns
		Clocks low	12.5			
t_{su}	Setup time		10			ns
t_h	Hold time		3			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = – 18 mA			– 1.2	V
V_{OH}		V_{CC} = 4.5 to 5.5 V,	I_{OH} = – 400 µA	V_{CC} – 1.5			V
		V_{CC} = 4.5 V,	I_{OH} = – 3 mA	2.8	3.6		
		V_{CC} = 4.5 V,	I_{OH} = – 15 mA	2			
V_{OL}	Ax, Dx, $\overline{ADx}$	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
	Ax, Dx, $\overline{ADx}$	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	RF	V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.2	0.4	
	RF	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.8	1	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			100	µA
I_{OL}	RF	V_{CC} = 4.5 V,	V_O = 2 V	15			mA
I_{IH}‡	$\overline{NBACK}$, NBDIEL, $\overline{NBDOE}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	All other inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			– 100	
I_{IL}‡	NBDIEL, NBDIEH, $\overline{NBDOE}$, STCYC	V_{CC} = 5.5 V,	V_I = 0.4 V			– 300	µA
	All other inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			– 200	
I_O§	Ax, Dx, $\overline{ADx}$	V_{CC} = 5.5 V,	V_O = 2.25 V	– 30		– 112	mA
	RF	V_{CC} = 5.5 V,	V_O = 2.25 V	– 20		– 50	
I_{CC}		V_{CC} = 5.5 V, V_{IH} = 3 V, V_{IL} = 0, Outputs open	Maximum number of outputs low		111	172	mA
			Maximum number of outputs disabled (high-Z)		40	68	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been selected to produce a current that closely approximates one half of the true short-circuit current I_{OS}.

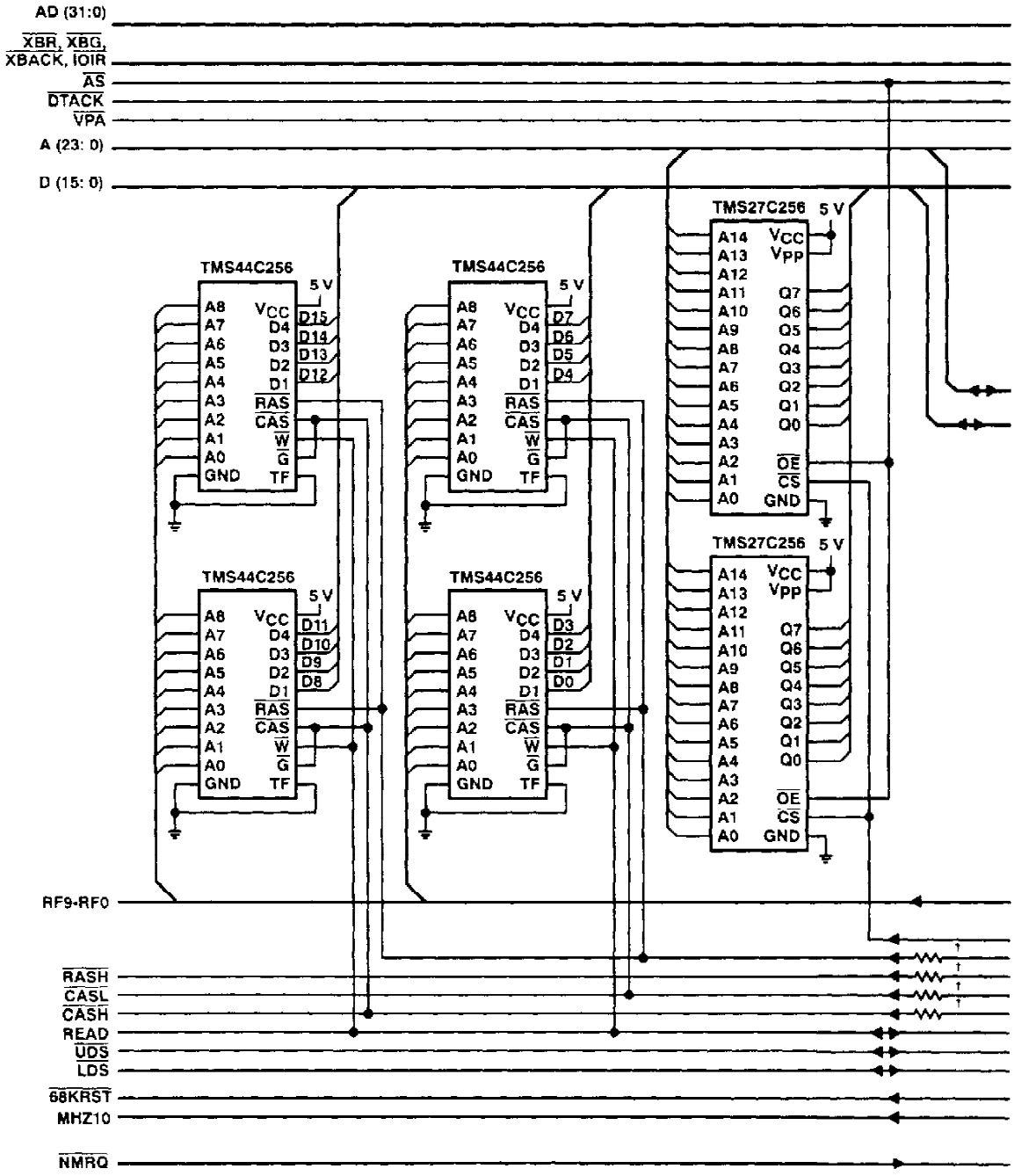
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)†

PARAMETER	FROM (INPUT)	TO (OUTPUT)†	TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
			V_L (V)	R1 (Ω)	R2 (Ω)	C_L (pF)				
t_{pd}	A3-A18	$\overline{AD3}$-$\overline{AD18}$	V_{CC}	270	470	130		11	18	ns
t_{pd}	D0-D15	$\overline{AD0}$-$\overline{AD15}$						11	18	ns
t_{pd}	D8-D15	$\overline{AD16}$-$\overline{AD23}$						11	18	ns
t_{pd}	$\overline{AS}$↑	$\overline{AD0}$-$\overline{AD15}$						14	22	ns
t_{pd}	A1	$\overline{AD0}$-$\overline{AD15}$						14	22	ns
t_{pd}	$\overline{AD0}$-$\overline{AD23}$	D0-D15	open	open	500	50		9	16	ns
t_{pd}	NBDIC↑	D0-D15						12	21	ns
t_{pd}	DSEL	D0-D15						15	23	ns
t_{pd}	NBAIC↑	A3-A18						10	18	ns
t_{pd}	A1-A20	RF0-RF9	open	open	2 k	50		9	16	ns
t_{pd}	MUX	RF0-RF9						9	16	ns
t_{en}	$\overline{NBDOE}$	$\overline{AD0}$-$\overline{AD23}$	V_{CC}	270	470	130		12	20	ns
t_{en}	STCYC	$\overline{AD3}$-$\overline{AD18}$						14	22	ns
t_{en}	NBDIEL	D0-D15	7	500	500	50		11	22	ns
t_{en}	NBDIEH	D8-D15						11	22	ns
t_{en}	$\overline{NBACK}$	A3-A18						10	20	ns
t_{dis}	$\overline{NBDOE}$	$\overline{AD0}$-$\overline{AD23}$	V_{CC}	270	470	50		6	10	ns
t_{dis}	STCYC	$\overline{AD3}$-$\overline{AD18}$						6	10	ns
t_{dis}	NBDIEL	D0-D15	7	500	500	50		6	10	ns
t_{dis}	NBDIEH	D8-D15						6	10	ns
t_{dis}	$\overline{NBACK}$	A3-A18						6	10	ns

† The outputs are measured one at a time with one transition per measurement or in the PAD mode two outputs switching at one time.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

APPLICATION INFORMATION



† Series damping resistors are recommended but may not be required depending on system environment.

Figure 1. MacIntosh Coprocessor Platform (MCP) Architecture (configured with 1 row of 245K x 4 DRAMs)

APPLICATION INFORMATION

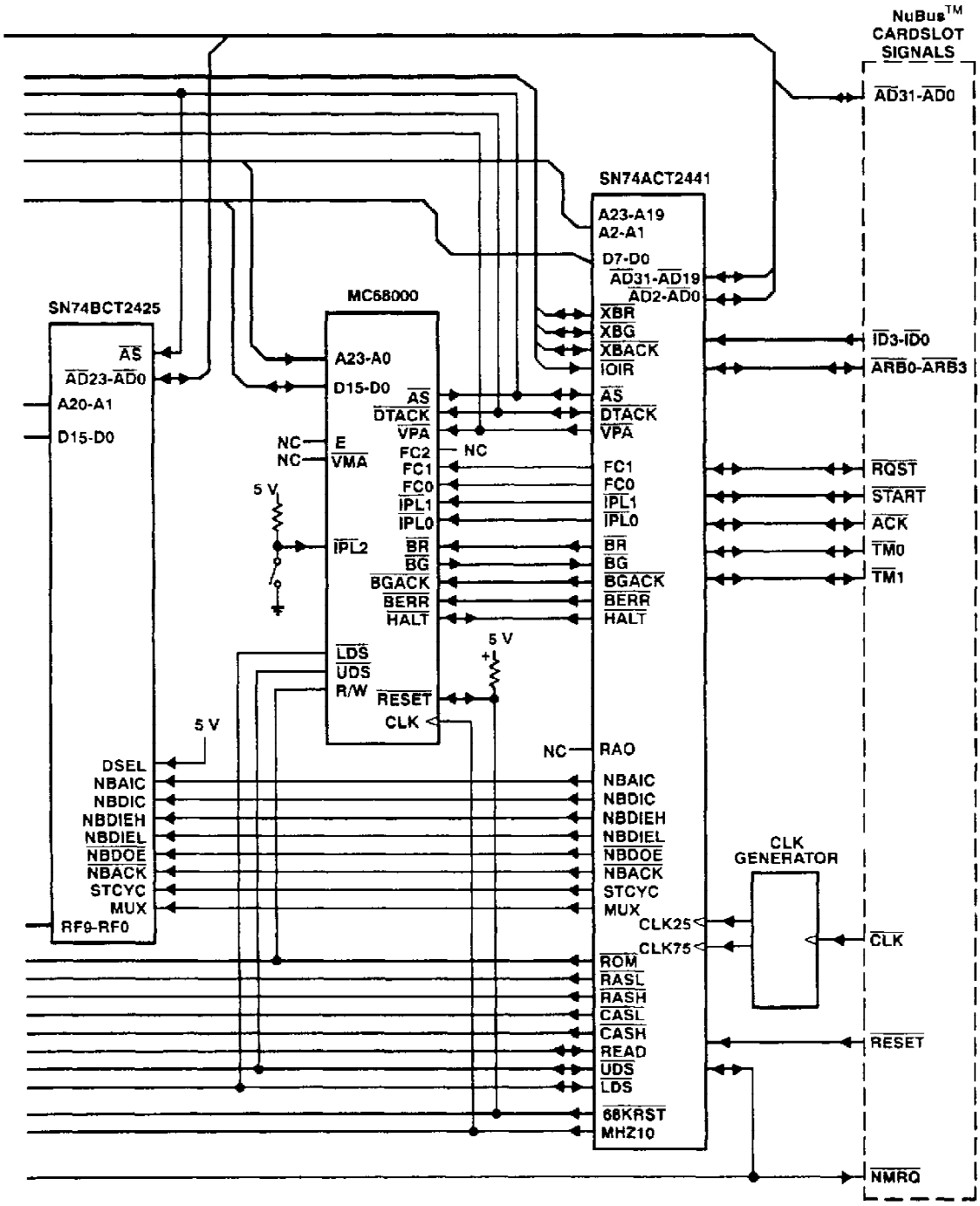
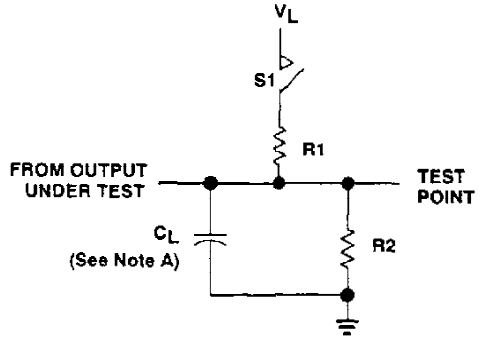


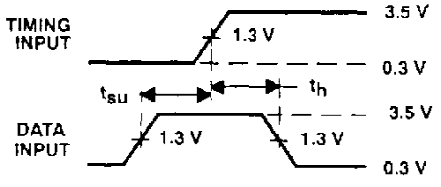
Figure 1. Macintosh Coprocessor Platform (MCP) Architecture (Continued)
(configured with 1 row of 245K x 4 DRAMs)

PARAMETER MEASUREMENT INFORMATION

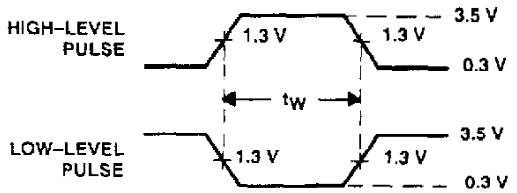
SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

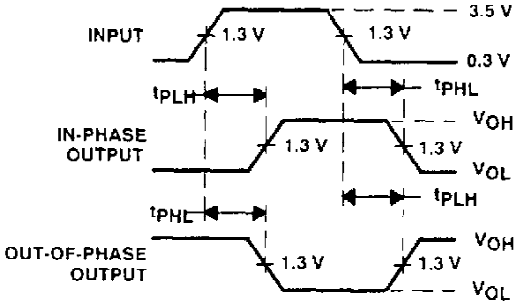




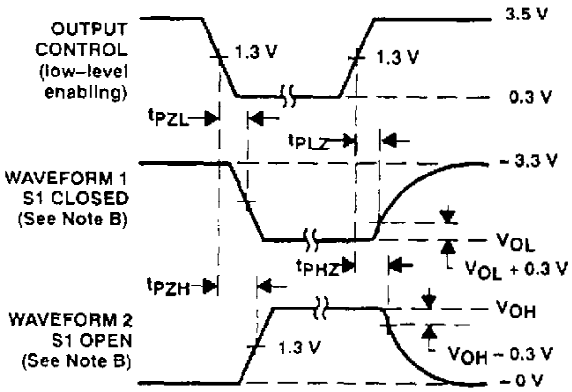
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74BCT2425PQ	OBSOLETE	BQFP	PQ	100		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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