

SN74BCT657

OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER AND 3-STATE OUTPUTS

SCBS079B – NOVEMBER 1991 – REVISED APRIL 1994

- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- 3-State B Outputs Sink 48 mA or 64 mA and Source 12 mA or 15 mA
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (NT)

description

The SN74BCT657 contains eight noninverting transceivers with 3-state outputs and an 8-bit parity generator/checker. It is intended for bus-oriented applications.

The transmit/receive (T/\bar{R}) input determines the direction of the data flow through the bidirectional transceivers. When T/\bar{R} is high, data is transmitted from the A port to the B port. When T/\bar{R} is low, data is received at the A port from the B port.

When the output-enable (\overline{OE}) input is high, both the A and B ports are placed in a high-impedance state (disabled). The ODD/ \overline{EVEN} input allows the user to select between odd or even parity systems.

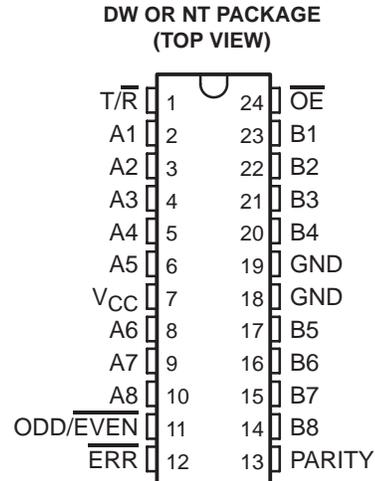
When transmitting from A port to B port (T/\bar{R} high), PARITY is an output from the generator/checker. When receiving from B port to A port (T/\bar{R} low), PARITY is an input.

When transmitting (T/\bar{R} high), the parity-select (ODD/ \overline{EVEN}) input is made high or low as appropriate. The A port is then polled to determine the number of high bits. The PARITY output goes to the logic state determined by the parity-select (ODD/ \overline{EVEN}) input and the number of high bits on A port. When ODD/ \overline{EVEN} is low (for even parity) and the number of high bits on A port is odd, the PARITY will be high, transmitting even parity. If the number of high bits on A port is even, the PARITY will be low, keeping even parity.

When in the receive mode (T/\bar{R} low), the B port is polled to determine the number of high bits. If ODD/ \overline{EVEN} is low (for even parity) and the number of highs on B port is as follows:

- Odd and the PARITY input is high, then \overline{ERR} will be high signifying no error.
- Even and the PARITY input is high, then \overline{ERR} will be low indicating an error.

The SN74BCT657 is characterized for operation from 0°C to 70°C.



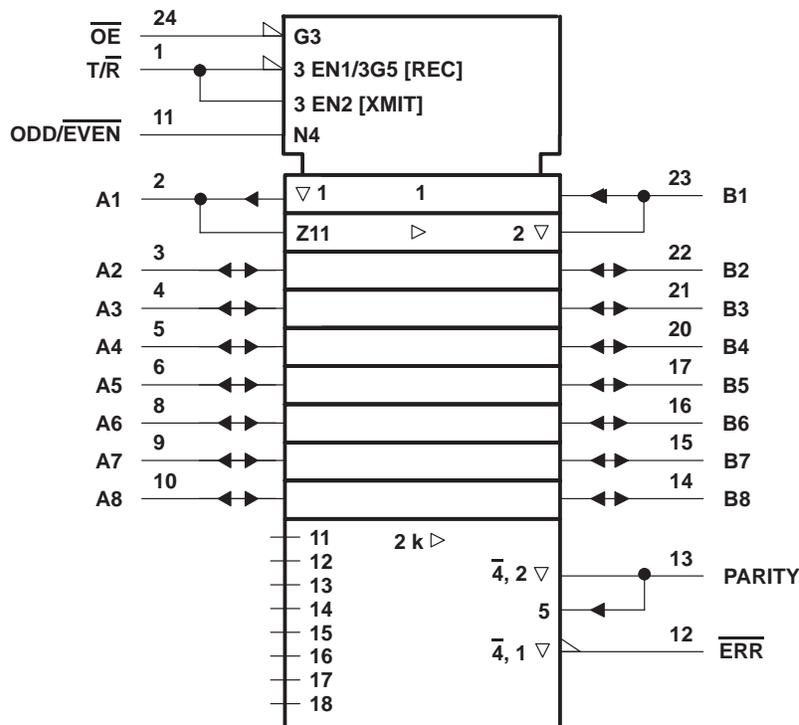
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FUNCTION TABLE

NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT PARITY	OUTPUTS	
	\overline{OE}	$\overline{T/R}$	ODD/ \overline{EVEN}		ERR	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

logic symbol†

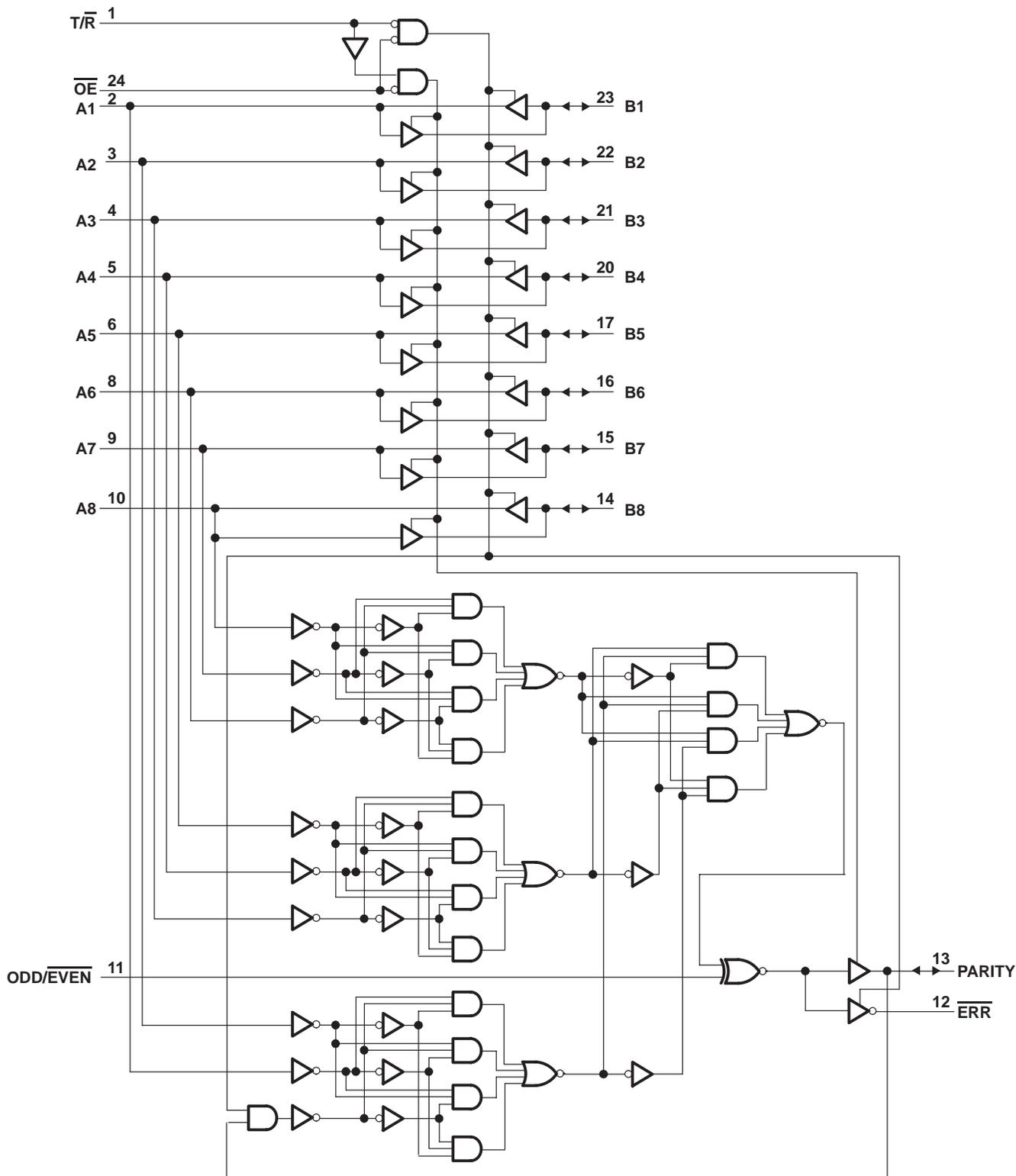


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O	-0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O	-0.5 V to V_{CC}
Input clamp current, I_{IK} ($V_I < 0$)	-30 mA
Current into any output in the low state, I_O	128 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current	A port		-3	mA
		B port, PARITY, \overline{ERR}		-15	
I_{OL}	Low-level output current	A port		24	mA
		B port, PARITY, \overline{ERR}		64	
T_A	Operating free-air temperature	0		70	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}		V _{CC} = 4.5 V,	I _I = -18 mA			-1.2	V
V _{OH}	Any output	V _{CC} = 4.5 V,	I _{OH} = -3 mA	2.4	3.3		V
	B port, PARITY, $\overline{\text{ERR}}$	V _{CC} = 4.5 V,	I _{OH} = -15 mA	2	3.1		
	Any output	V _{CC} = 4.75 V,	I _{OH} = -3 mA	2.7			
V _{OL}	A port	V _{CC} = 4.5 V,	I _{OL} = 24 mA		0.35	0.5	V
	B port, PARITY, $\overline{\text{ERR}}$	V _{CC} = 4.5 V,	I _{OL} = 64 mA		0.42	0.55	
I _I	$\overline{\text{T/R}}$	V _{CC} = 0,	V _I = 7 V, $\overline{\text{OE}} = 4.5$ V			20	μA
	$\overline{\text{OE}}$	V _{CC} = 0,	V _I = 7 V, $\overline{\text{T/R}} = 4.5$ V			20	
	$\overline{\text{ODD/EVEN}}$	V _{CC} = 0,	V _I = 7 V			20	
	A port					100	
	B port, PARITY	V _{CC} = 5.5 V,	V _I = 5.5 V			200	
I _{IH} ‡	A or B port, PARITY	V _{CC} = 5.5 V,	V _I = 2.7 V			200	μA
	$\overline{\text{T/R}}$, $\overline{\text{OE}}$					20	
	$\overline{\text{ODD/EVEN}}$					20	
I _{IL} ‡	A or B port, PARITY	V _{CC} = 5.5 V,	V _I = 0.5 V			-70	μA
	$\overline{\text{T/R}}$, $\overline{\text{OE}}$					-20	
	$\overline{\text{ODD/EVEN}}$					-20	
I _{OS} §	A port	V _{CC} = 5.5 V,	V _O = 0			-60	mA
	B port, PARITY, $\overline{\text{ERR}}$					-125	
I _{OZH}	$\overline{\text{ERR}}$	V _{CC} = 5.5 V,	V _O = 2.7 V			50	μA
I _{OZL}	$\overline{\text{ERR}}$	V _{CC} = 5.5 V,	V _O = 0.5 V			-50	μA
I _{CCL}		V _{CC} = 5.5 V,	Outputs open			90	mA
I _{CCH}		V _{CC} = 5.5 V,	Outputs open			2	mA
I _{CCZ}		V _{CC} = 5.5 V,	Outputs open			1	mA
C _i	Control input	V _{CC} = 5 V,	V _I = 2.5 V or 0.5 V		6.5		pF
C _{io}	A port	V _{CC} = 5 V,	V _O = 2.5 V or 0.5 V		10		pF
	B port, PARITY				14		
C _o	$\overline{\text{ERR}}$	V _{CC} = 5 V,	V _O = 2.5 V or 0.5 V		10		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	1.1	3.1	6	1.1	6.6	ns
t_{PHL}			2	5.3	8.5	2	9	
t_{PLH}	A	PARITY	3	7.4	12.7	3	15.4	ns
t_{PHL}			4.6	8.6	14.1	4.6	15.9	
t_{PLH}	ODD/EVEN	PARITY, \overline{ERR}	1.1	4.1	6.4	1.1	7.1	ns
t_{PHL}			2.6	5.5	8.3	2.6	9	
t_{PLH}	B	\overline{ERR}	3.1	7.4	12.6	3.1	15.3	ns
t_{PHL}			4.4	6.5	13.3	4.4	15.5	
t_{PLH}	PARITY	\overline{ERR}	3.4	7.7	10.7	3.4	13.2	ns
t_{PHL}			5.5	8.8	12	5.5	13.9	
t_{PZH}	\overline{OE}	A, B, PARITY, or \overline{ERR}	1.8	5.1	7.7	1.8	9.1	ns
t_{PZL}			3.2	6.7	14.2	3.2	16.3	
t_{PHZ}	\overline{OE}	A, B, PARITY, or \overline{ERR}	2.6	5.7	8	2.6	9.1	ns
t_{PLZ}			2	5	7.4	2	8	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74BCT657DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN74BCT657DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN74BCT657NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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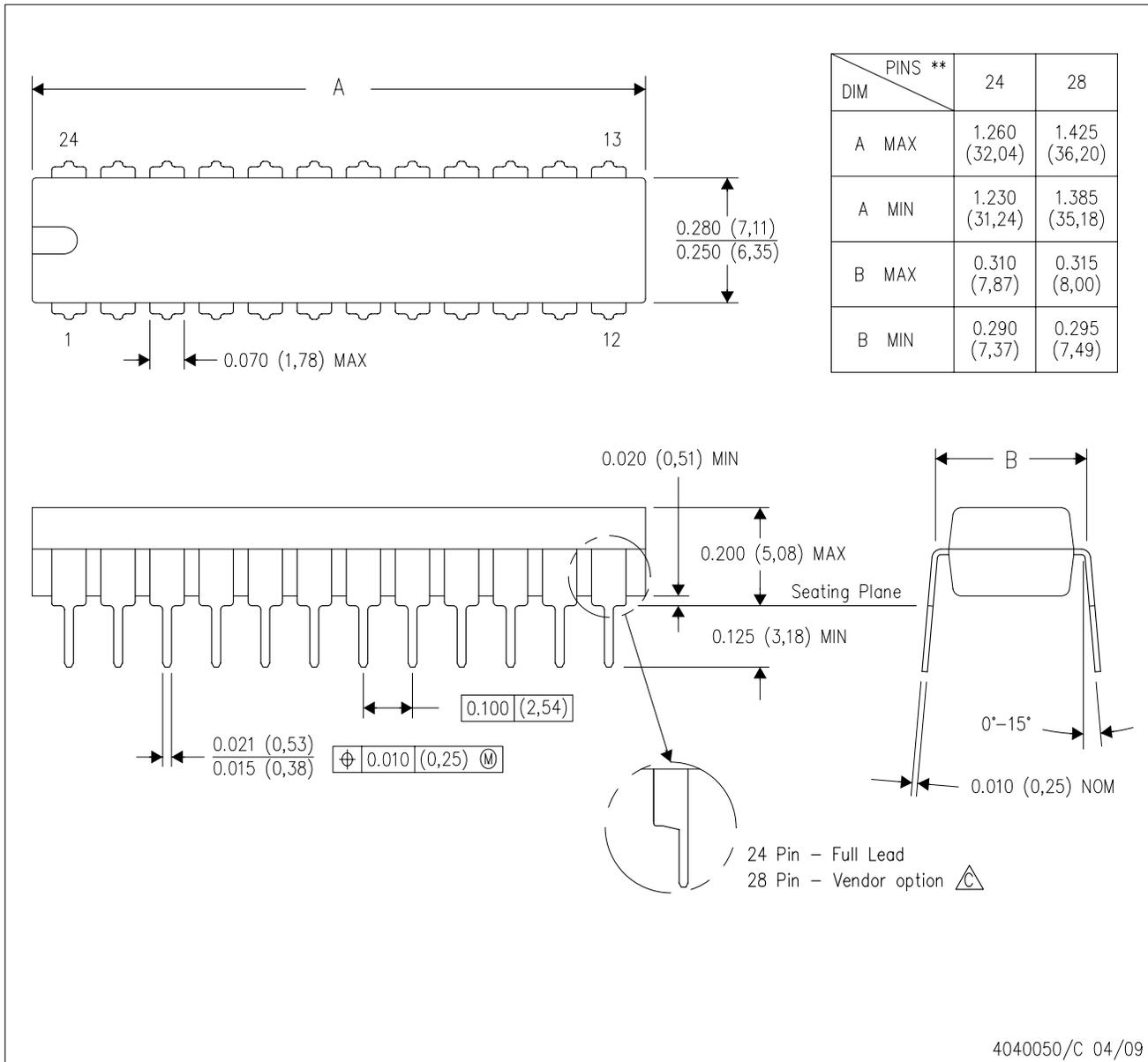
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MECHANICAL DATA

NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

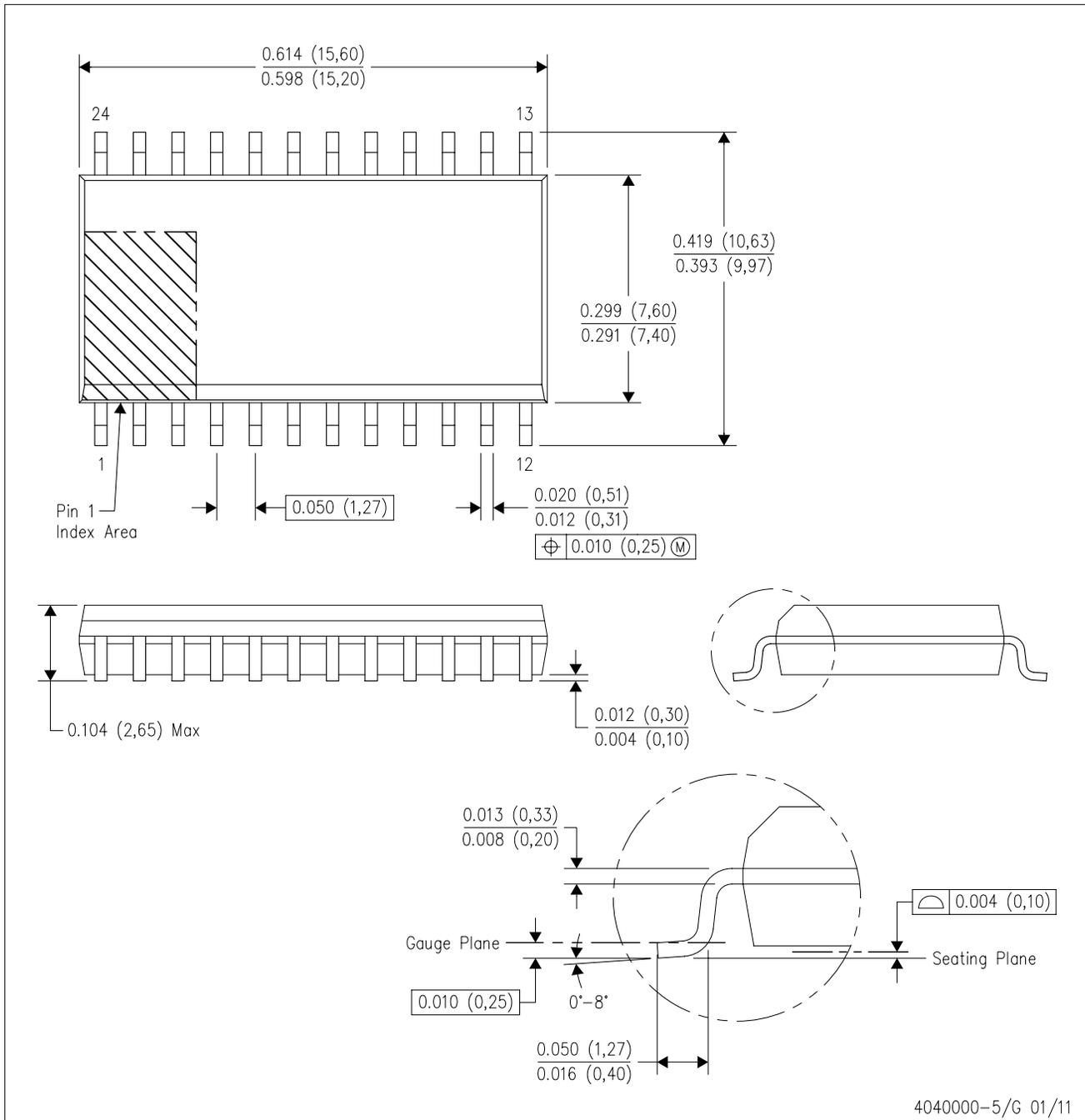
24 PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

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