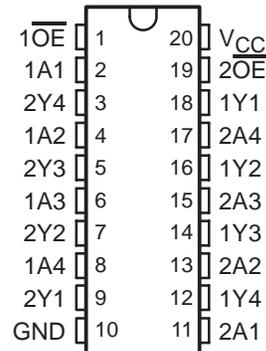


SN74HC244-Q1 OCTAL BUFFER AND LINE DRIVER WITH 3-STATE OUTPUTS

SCLS543A – SEPTEMBER 2002 – REVISED APRIL 2008

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Wide Operating Voltage Range of 2 V to 6 V
- High-Current Outputs Drive Up To 15 LSTTL Loads
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 11$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max

DW OR PW PACKAGE
(TOP VIEW)



description/ordering information

This octal buffer and line driver is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The SN74HC244 is organized as two 4-bit buffers/drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes noninverted data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

ORDERING INFORMATION†

T _A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SOIC – DW	Reel of 2000		
–40°C to 125°C	TSSOP – PW	Reel of 2000	SN74HC244QDWRQ1	HC244Q
			SN74HC244QPWRQ1	HC244Q

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

FUNCTION TABLE
(each buffer/driver)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
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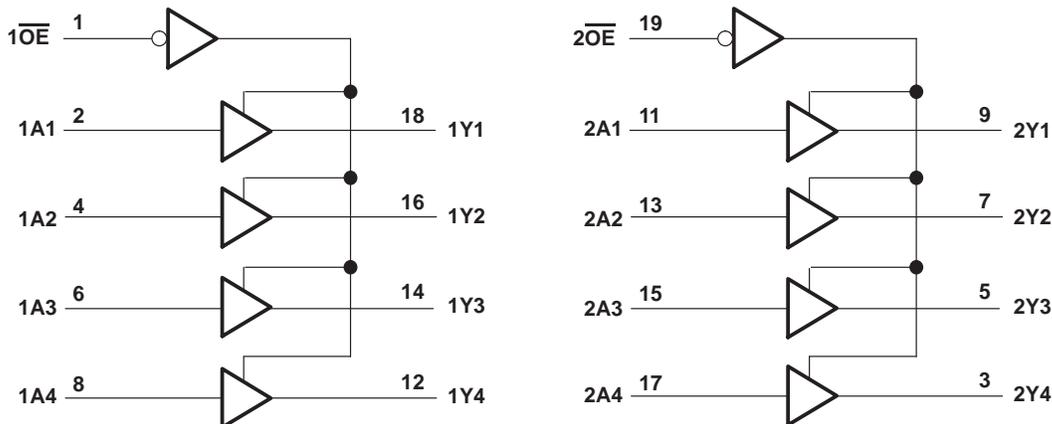
SN74HC244-Q1

OCTAL BUFFER AND LINE DRIVER

WITH 3-STATE OUTPUTS

SCLS543A – SEPTEMBER 2002 – REVISED APRIL 2008

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND	± 70 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	58°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5		V
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 6$ V	4.2		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5	V
		$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 6$ V		1.8	
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
t_t	Input transition (rise and fall) time	$V_{CC} = 2$ V		1000	ns
		$V_{CC} = 4.5$ V		500	
		$V_{CC} = 6$ V		400	
T_A	Operating free-air temperature	-40		125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74HC244-Q1
OCTAL BUFFER AND LINE DRIVER
WITH 3-STATE OUTPUTS

SCLS543A – SEPTEMBER 2002 – REVISED APRIL 2008

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998	1.9	V	
			4.5 V	4.4	4.499	4.4		
			6 V	5.9	5.999	5.9		
		I _{OH} = -6 mA	4.5 V	3.98	4.3	3.7		
			6 V	5.48	5.8	5.2		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V	0.002	0.1	0.1	V	
			4.5 V	0.001	0.1	0.1		
			6 V	0.001	0.1	0.1		
		I _{OL} = 6 mA	4.5 V	0.17	0.26	0.4		
			6 V	0.15	0.26	0.4		
I _I	V _I = V _{CC} or 0	6 V	±0.1	±100	±1000	nA		
I _{OZ}	V _O = V _{CC} or 0, V _I = V _{IH} or V _{IL}	6 V	±0.01	±0.5	±10	μA		
I _{CC}	V _I = V _{CC} or 0, I _O = 0	6 V		8	160	μA		
C _i		2 V to 6 V		3	10	10	pF	

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _{pd}	A	Y	2 V	40	115	170	ns		
			4.5 V	13	23	34			
			6 V	11	20	29			
t _{en}	\overline{OE}	Y	2 V	75	150	225	ns		
			4.5 V	15	30	45			
			6 V	13	26	38			
t _{dis}	\overline{OE}	Y	2 V	75	150	225	ns		
			4.5 V	15	30	45			
			6 V	13	26	38			
t _t		Y	2 V	28	60	90	ns		
			4.5 V	8	12	18			
			6 V	6	10	15			

operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per buffer/driver	No load	35	pF



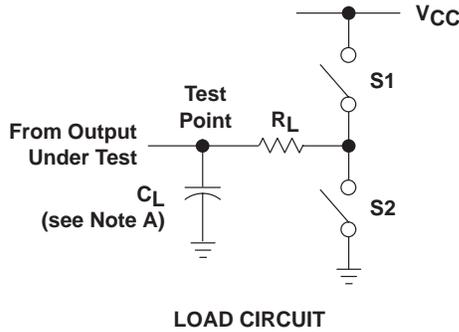
SN74HC244-Q1

OCTAL BUFFER AND LINE DRIVER

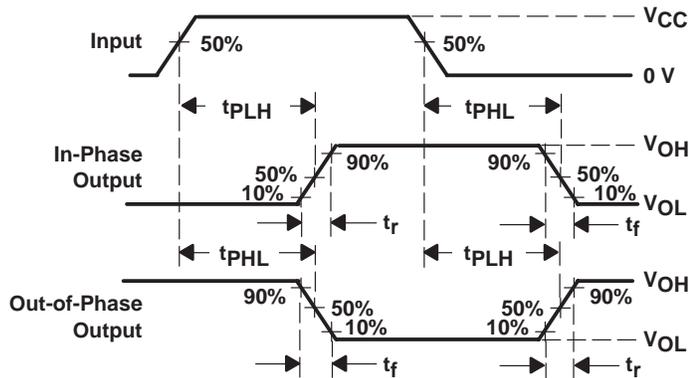
WITH 3-STATE OUTPUTS

SCLS543A – SEPTEMBER 2002 – REVISED APRIL 2008

PARAMETER MEASUREMENT INFORMATION



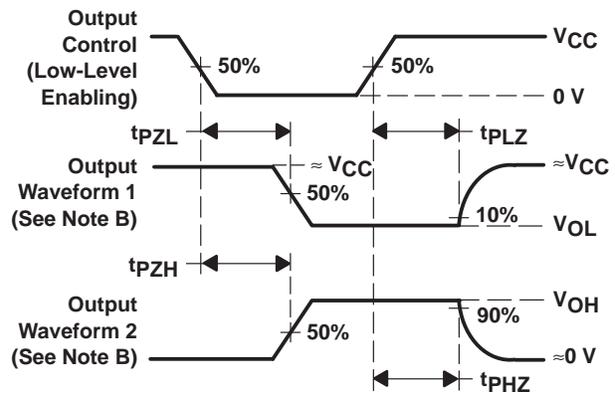
PARAMETER	R_L	C_L	S1	S2
t_{en}	1 k Ω	50 pF	Open	Closed
			Closed	Open
t_{dis}	1 k Ω	50 pF	Open	Closed
			Closed	Open
t_{pd} or t_t	--	50 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74HC244QDWRQ1	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC244QPWRG4Q1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC244QPWRQ1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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- Catalog: [SN74HC244](#)

- Enhanced Product: [SN74HC244-EP](#)

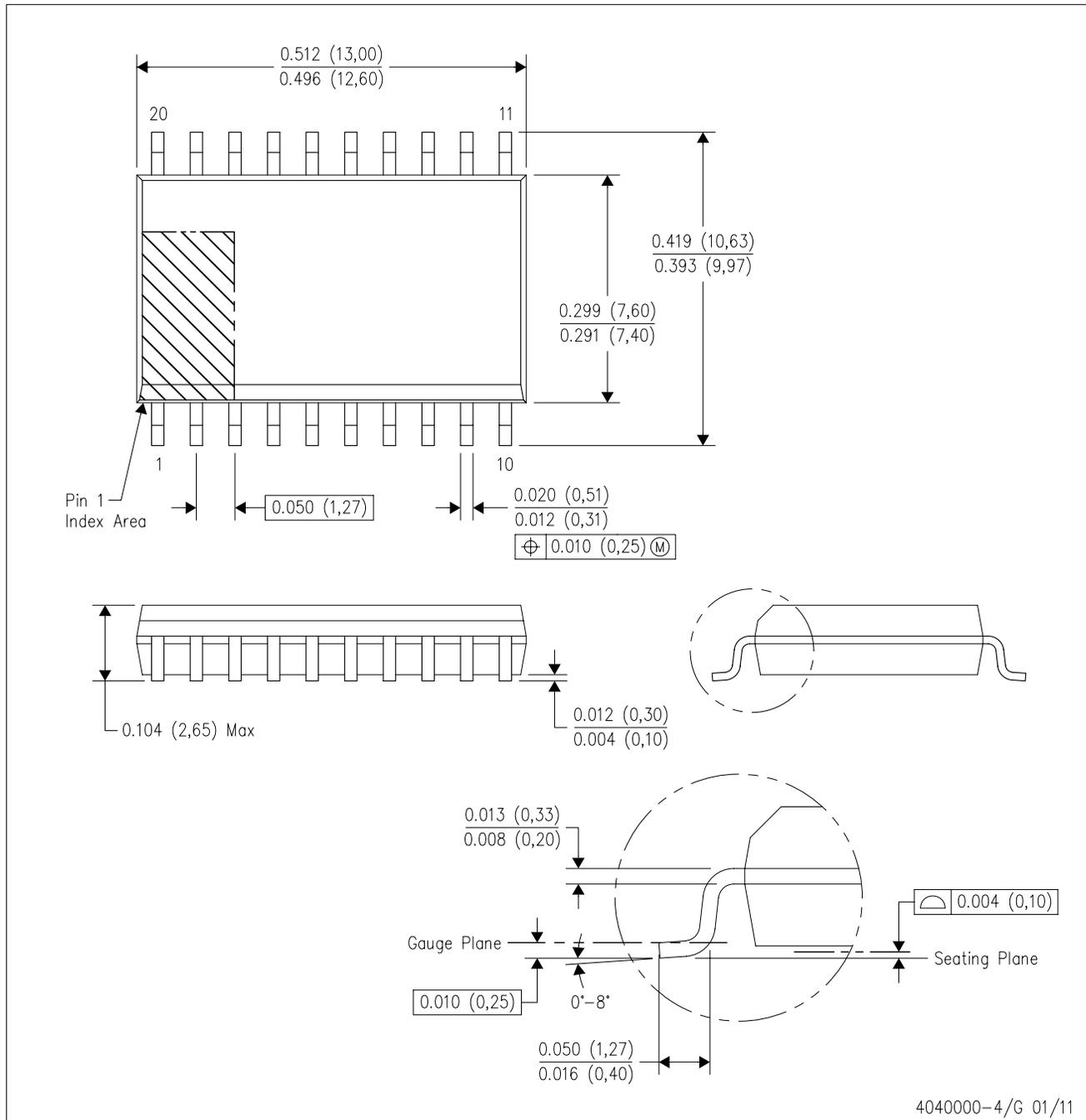
- Military: [SN54HC244](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

DW (R-PDSO-G20)

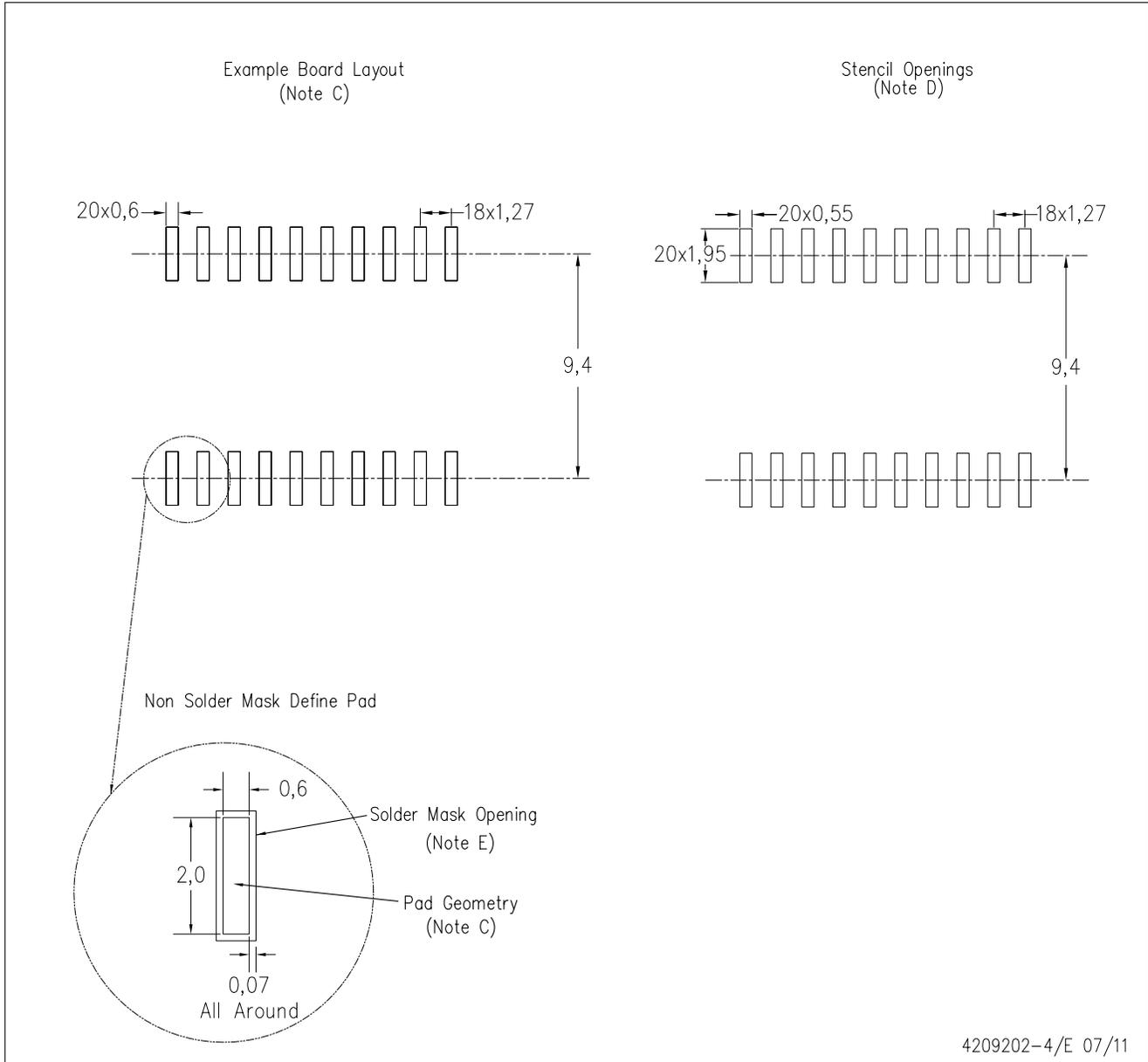
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

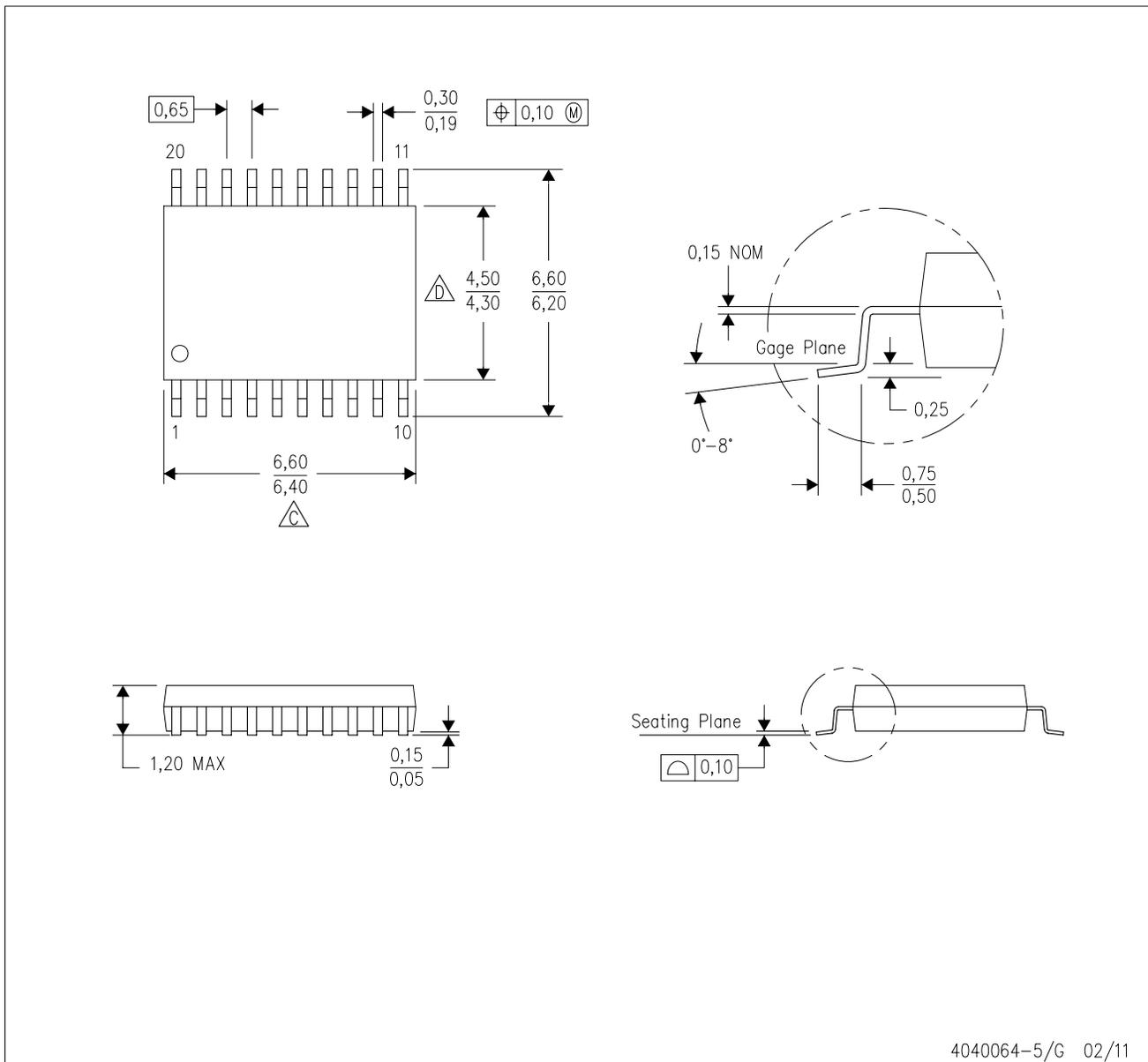


4209202-4/E 07/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

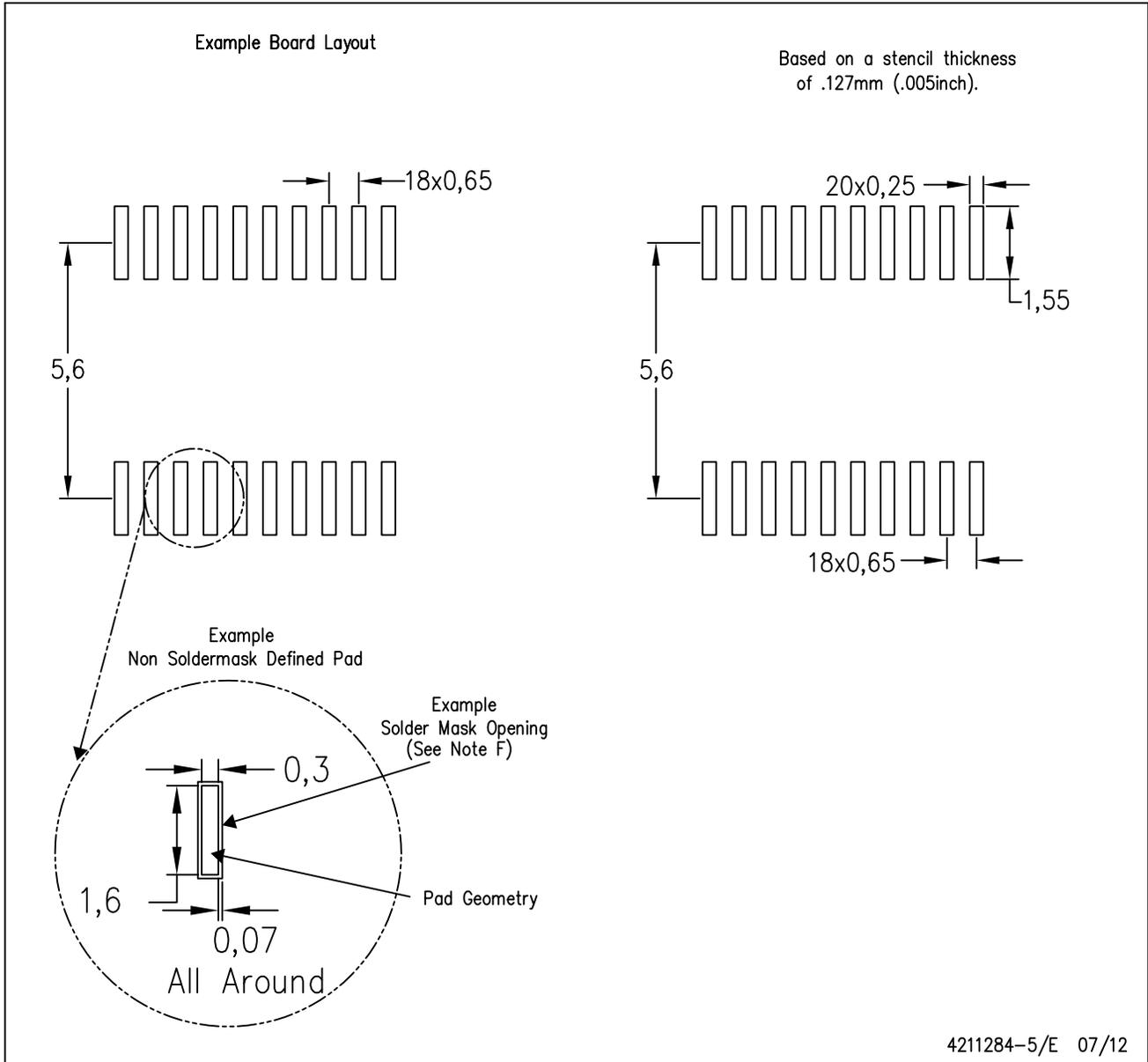


4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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