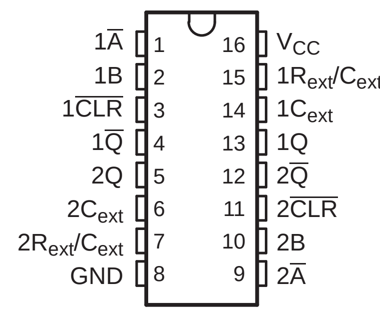
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH SCHMITT-TRIGGER INPUTS

Check for Samples: SN74LV123A-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Supports Mixed-Mode Voltage Operation on All Ports**
- **Schmitt-Trigger Circuitry on $\overline{A}$, B, and $\overline{CLR}$ Inputs for Slow Input Transition Rates**
- **Edge Triggered From Active-High or Active-Low Gated Logic Inputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Retriggerable for Very Long Output Pulses, up to 100% Duty Cycle**
- **Overriding Clear Terminates Output Pulse**
- **Glitch-Free Power-Up Reset on Outputs**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

PW PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74LV123A is a dual retriggerable monostable multivibrator designed for 2-V to 5.5-V V_{CC} operation.

This edge-triggered multivibrator features output pulse-duration control by three methods. In the first method, the $\overline{A}$ input is low, and the B input goes high. In the second method, the B input is high, and the $\overline{A}$ input goes low. In the third method, the $\overline{A}$ input is low, the B input is high, and the clear ($\overline{CLR}$) input goes high.

The output pulse duration is programmable by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC}. To obtain variable pulse durations, connect an external variable resistance between R_{ext}/C_{ext} and V_{CC}. The output pulse duration also can be reduced by taking $\overline{CLR}$ low.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The $\overline{A}$, B, and $\overline{CLR}$ inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Once triggered, the basic pulse duration can be extended by retriggering the gated low-level-active ($\overline{A}$) or high-level-active (B) input. Pulse duration can be reduced by taking $\overline{CLR}$ low. The input/output timing diagram illustrates pulse control by retriggering the inputs and early clearing.

During power up, Q outputs are in the low state, and $\overline{Q}$ outputs are in the high state. The outputs are glitch free, without applying a reset pulse.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	TSSOP – PW	Tape and reel	SN74LV123ATPWRQ1	LV123AQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Table 1. FUNCTION TABLE (EACH MULTIVIBRATOR)

INPUTS			OUTPUTS	
$\overline{CLR}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L(1)	H(1)
X	X	L	L(1)	H(1)
H	L	↑	⎍	⊔
H	↓	H	⎍	⊔
↑	L	H	⎍	⊔

(1) These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

Figure 1. LOGIC DIAGRAM, EACH MULTIVIBRATOR (POSITIVE LOGIC)

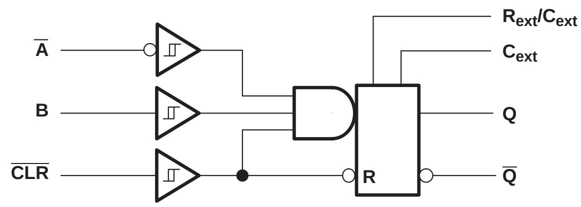
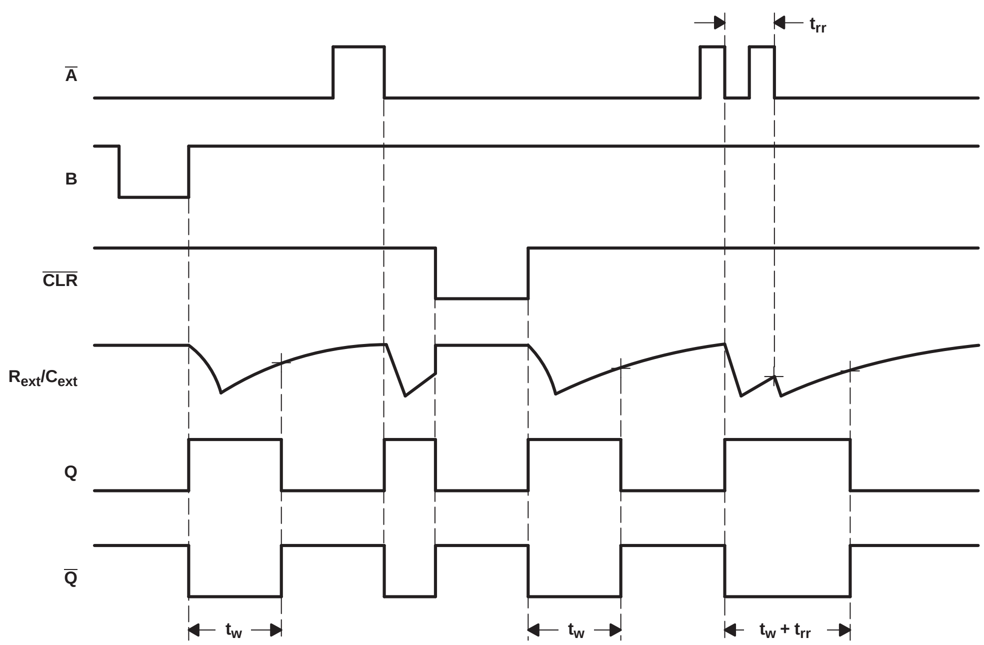


Figure 2. INPUT/OUTPUT TIMING DIAGRAM



Absolute Maximum Ratings[1]

over operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range[2]		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		–0.5	7	V
V_O	Output voltage range in the high or low state[2] [3]		–0.5	V_{CC} + 0.5	V
V_O	Output voltage range in power-off state[2]		–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance[4]			113	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value is limited to 5.5 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	µA
		V_{CC} = 2.3 V to 2.7 V		–2	mA
		V_{CC} = 3 V to 3.6 V		–6	
		V_{CC} = 4.5 V to 5.5 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		6	
		V_{CC} = 4.5 V to 5.5 V		12	
R_{ext}	External timing resistance	V_{CC} = 2 V	5		kΩ
		$V_{CC} \geq 3$ V	1		
C_{ext}	External timing capacitance		No restriction		pF
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		1		ms/V
T_A	Operating free-air temperature		–40	105	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

THERMAL INFORMATION

THERMAL METRIC(1)		SN74LV123ATPWRQ1 TSSOP – PW 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	111.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	46.1	
θ_{JB}	Junction-to-board thermal resistance(4)	56.3	
ψ_{JT}	Junction-to-top characterization parameter(5)	5.6	
ψ_{JB}	Junction-to-board characterization parameter(6)	55.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}		I_{OH} = –50 µA	2 V to 5.5 V	V_{CC} – 0.1			V
		I_{OH} = –2 mA	2.3 V	2			
		I_{OH} = –6 mA	3 V	2.48			
		I_{OH} = –12 mA	4.5 V	3.8			
V_{OL}		I_{OL} = 50 µA	2 V to 5.5 V			0.1	V
		I_{OL} = 2 mA	2.3 V			0.4	
		I_{OL} = 6 mA	3 V			0.44	
		I_{OL} = 12 mA	4.5 V			0.55	
I_I	R_{ext}/C_{ext} (1)	V_I = 5.5 V or GND	5.5 V			±2.5	µA
	$\overline{A}$, B, and $\overline{CLR}$	V_I = 5.5 V or GND	0 V			±1	
			0 to 5.5 V			±1	
I_{CC}	Quiescent	V_I = V_{CC} or GND, I_O = 0	5.5 V			20	µA
I_{CC}	Active state (per circuit)	V_I = V_{CC} or GND, R_{ext}/C_{ext} = 0.5 V_{CC}	3 V			280	µA
			4.5 V			650	
			5.5 V			975	
I_{off}		V_I or V_O = 0 to 5.5 V	0 V			5	µA
C_i		V_I = V_{CC} or GND	3.3 V		1.9		pF
			5 V		1.9		

(1) This test is performed with the terminal in the off-state condition.

Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 3)

PARAMETER			TEST CONDITIONS		T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	MIN	MAX	UNIT
t_w	Pulse duration	$\overline{CLR}$			5			5		ns
t_w	Pulse duration	$\overline{A}$ or B trigger			5			5		ns
t_{rr}	Pulse retrigger time		R_{ext} = 1 kΩ	C_{ext} = 100 pF	(1)	76		(1)		ns
t_{rr}	Pulse retrigger time		R_{ext} = 1 kΩ	C_{ext} = 0.01 μF	(1)	1.8		(1)		μs

(1) See retriggering data in the *application information* section

Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 3)

PARAMETER			TEST CONDITIONS		T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	MIN	MAX	UNIT
t_w	Pulse duration	$\overline{CLR}$			5			5		ns
t_w	Pulse duration	$\overline{A}$ or B trigger			5			5		ns
t_{rr}	Pulse retrigger time		R_{ext} = 1 kΩ	C_{ext} = 100 pF	(1)	59		(1)		ns
t_{rr}	Pulse retrigger time		R_{ext} = 1 kΩ	C_{ext} = 0.01 μF	(1)	1.5		(1)		μs

(1) See retriggering data in the *application information* section

Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	MIN	MAX	UNIT
t_{pd}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 50 pF		11.8	24.1	1	27.5	ns
t_{pd}	$\overline{CLR}$	Q or $\overline{Q}$	C_L = 50 pF		10.5	19.3	1	22	ns
t_{pd}	$\overline{CLR}$ trigger	Q or $\overline{Q}$	C_L = 50 pF		12.3	25.9	1	29.5	ns
t_w (1)		Q or $\overline{Q}$	C_L = 50 pF C_{ext} = 28 pF R_{ext} = 2 kΩ		182	240		300	ns
t_w (1)		Q or $\overline{Q}$	C_L = 50 pF C_{ext} = 0.01 μF R_{ext} = 10 kΩ	90	100	110	90	110	μs
t_w (1)		Q or $\overline{Q}$	C_L = 50 pF C_{ext} = 0.1 μF R_{ext} = 10 kΩ	0.9	1	1.1	0.9	1.1	ms
Δt_w (2)			C_L = 50 pF		±1				%

(1) t_w = Duration of pulse at Q and $\overline{Q}$ outputs
(2) Δt_w = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	MIN	MAX	UNIT
t_{pd}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 50 pF		8.3	14	1	16	ns
t_{pd}	$\overline{CLR}$	Q or $\overline{Q}$	C_L = 50 pF		7.4	11.4	1	13	ns
t_{pd}	$\overline{CLR}$ trigger	Q or $\overline{Q}$	C_L = 50 pF		8.7	14.9	1	17	ns

Switching Characteristics (continued)

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_w (1)		Q or $\overline{Q}$	C_L = 50 pF C_{ext} = 28 pF R_{ext} = 2 kΩ		167	200		240	ns
			C_L = 50 pF C_{ext} = 0.01 µF R_{ext} = 10 kΩ	90	100	110	90	110	µs
			C_L = 50 pF C_{ext} = 0.1 µF R_{ext} = 10 kΩ	0.9	1	1.1	0.9	1.1	ms
Δt_w (2)			C_L = 50 pF		±1				%

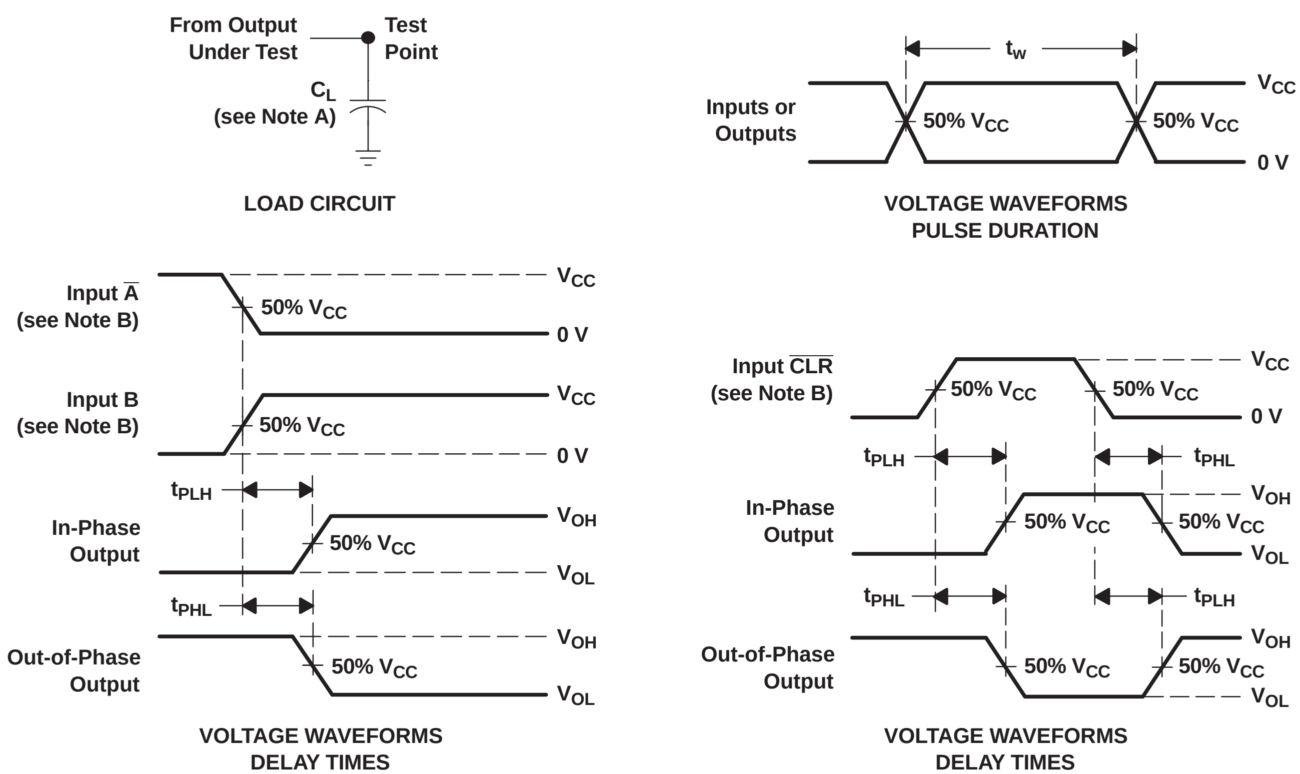
(1) t_w = Duration of pulse at Q and $\overline{Q}$ outputs
(2) Δt_w = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 10 MHz	3.3 V	44	pF
				5 V	49	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time, with one input transition per measurement.

Figure 3. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

Operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied.

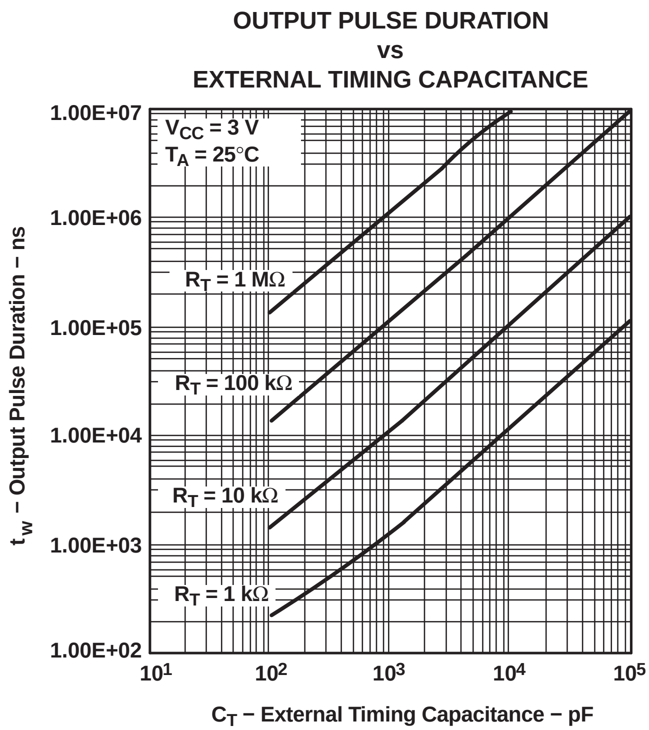


Figure 4.

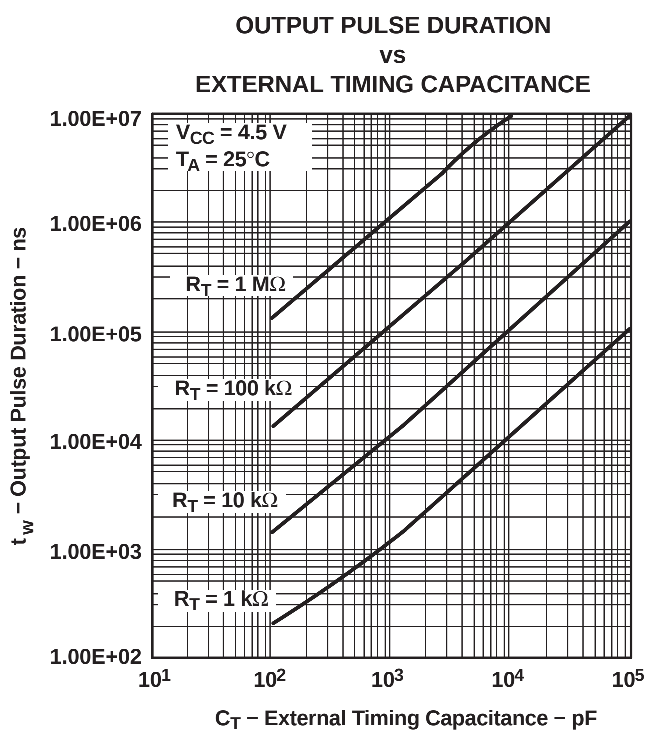


Figure 5.

APPLICATION INFORMATION

Operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied.

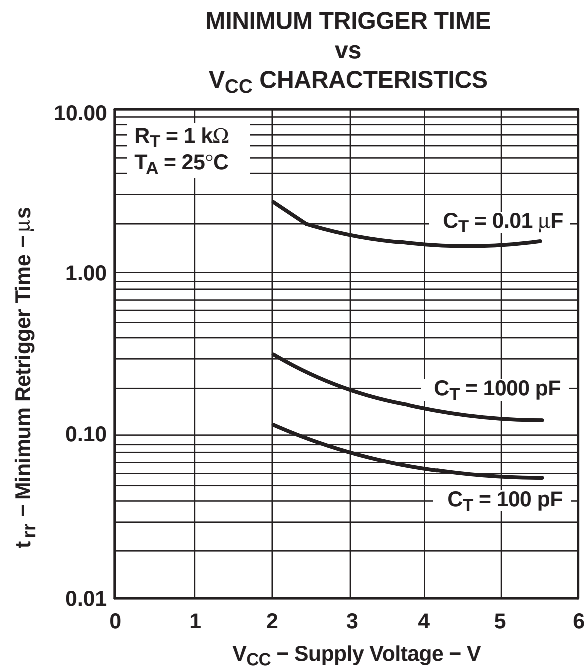


Figure 6.

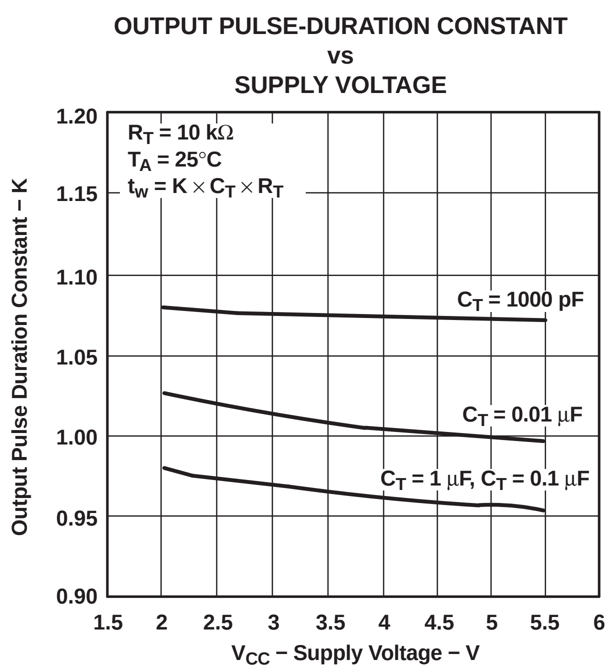


Figure 7.

Caution In Use

To prevent malfunctions due to noise, connect a high-frequency capacitor between V_{CC} and GND, and keep the wiring between the external components and C_{ext} and R_{ext} / C_{ext} terminals as short as possible.

Power-Down Considerations

Large values of C_{ext} can cause problems when powering down the 'LV123A devices because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor can discharge from V_{CC} through the protection diodes at pin 2 or pin 14. Current through the input protection diodes must be limited to 30 mA; therefore, the turn-off time of the V_{CC} power supply must not be faster than t = V_{CC} × C_{ext} / 30 mA. For example, if V_{CC} = 5 V and Cext = 15 pF, the V_{CC} supply must turn off no faster than t = (5 V) × (15 pF) / 30 mA = 2.5 ns. Usually, this is not a problem because power supplies are heavily filtered and cannot discharge at this rate. When a more rapid decrease of V_{CC} to zero occurs, the 'LV123A devices can sustain damage. To avoid this possibility, use external clamping diodes.

REVISION HISTORY

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN74LV123ATPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV123ATPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LV123A-Q1 :

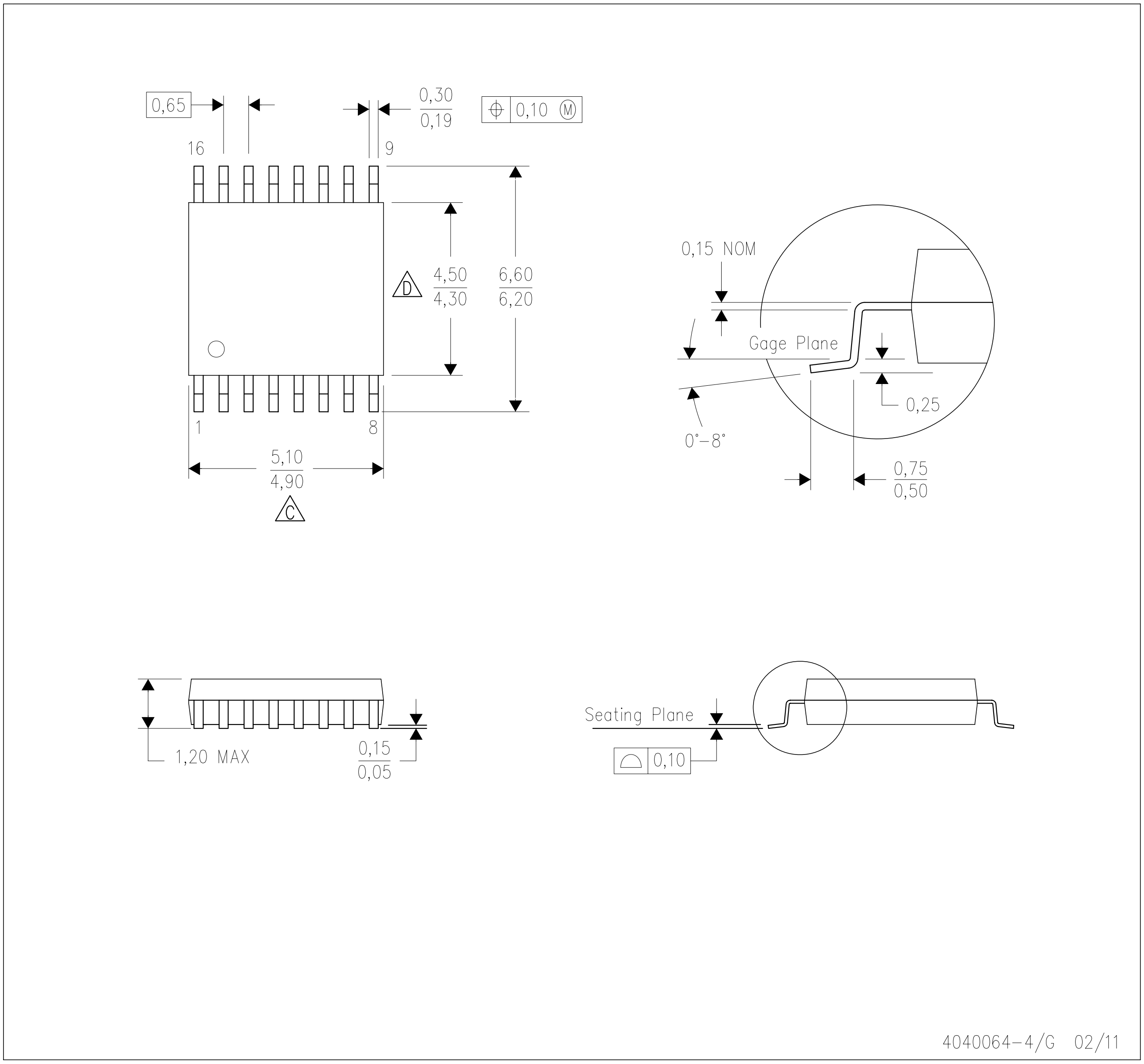
- Catalog: SN74LV123A

- Enhanced Product: SN74LV123A-EP

NOTE: Qualified Version Definitions:

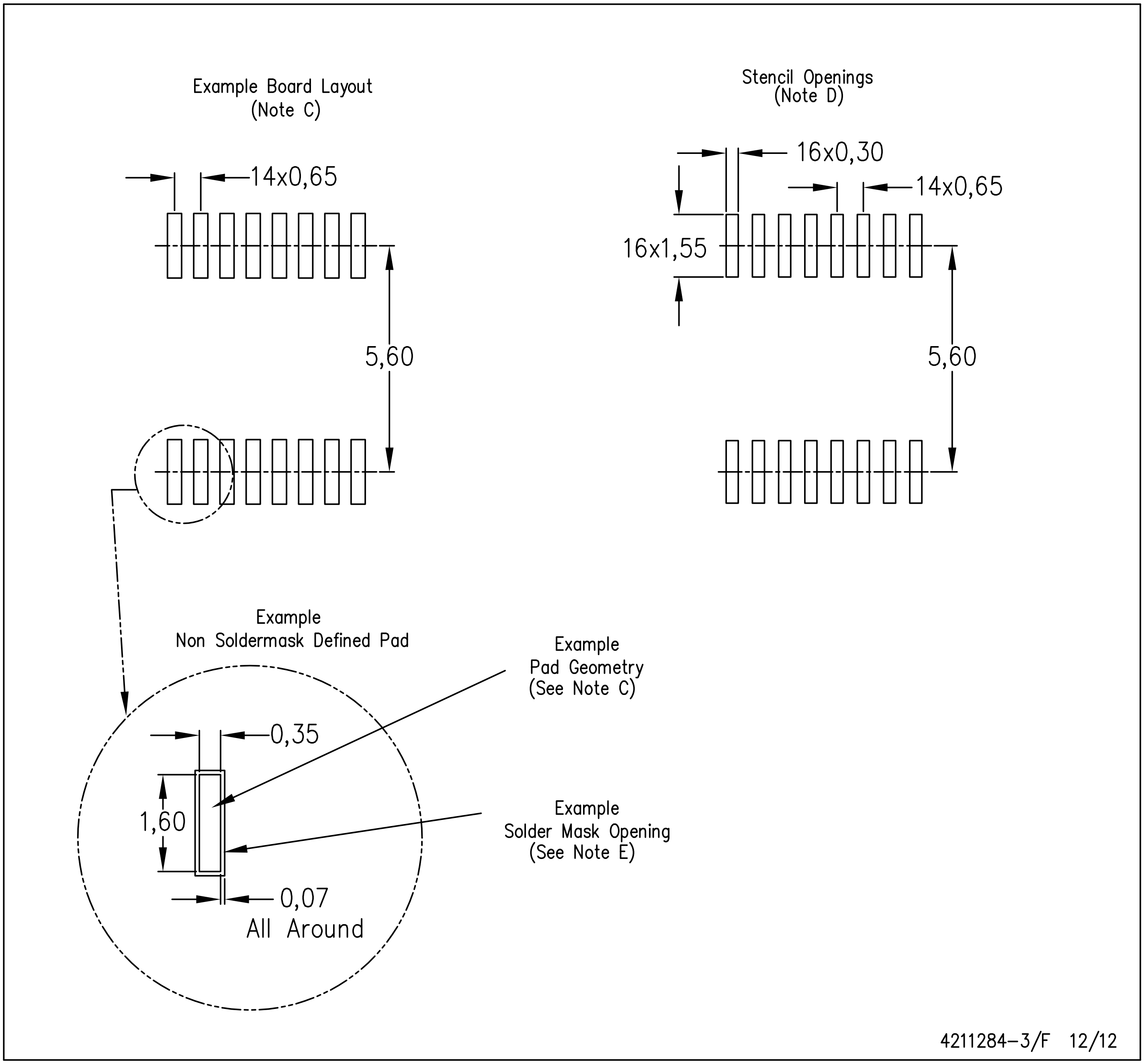
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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