

# SN54LV374, SN74LV374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS197B – FEBRUARY 1993 – REVISED APRIL 1996

- **EPIC™ (Enhanced-Performance Implanted CMOS) 2- $\mu$  Process**
- **Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$**
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2$  V at  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs**

## description

These octal edge-triggered D-type flip-flops are designed for 2.7-V to 5.5-V  $V_{CC}$  operation.

The 'LV374 feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

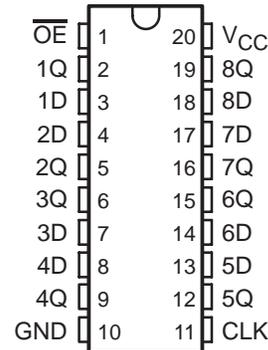
A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either as normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

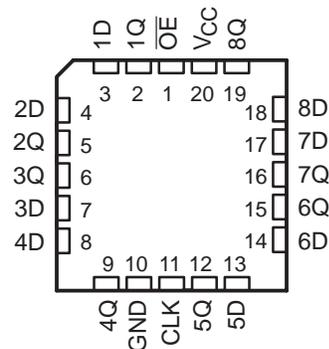
The SN74LV374 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LV374 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74LV374 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54LV374 . . . J OR W PACKAGE  
SN74LV374 . . . DB, DW, OR PW PACKAGE  
(TOP VIEW)



SN54LV374 . . . FK PACKAGE  
(TOP VIEW)



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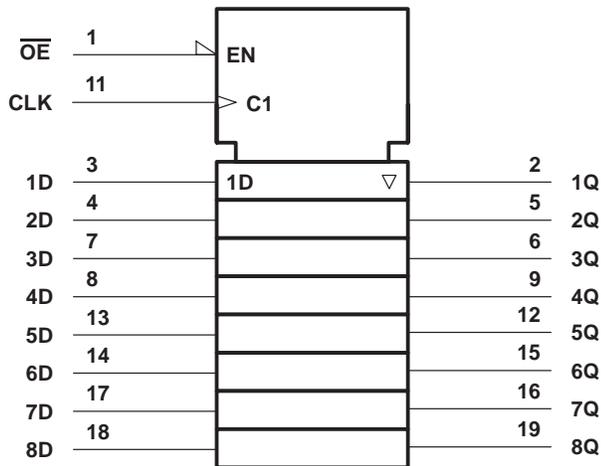
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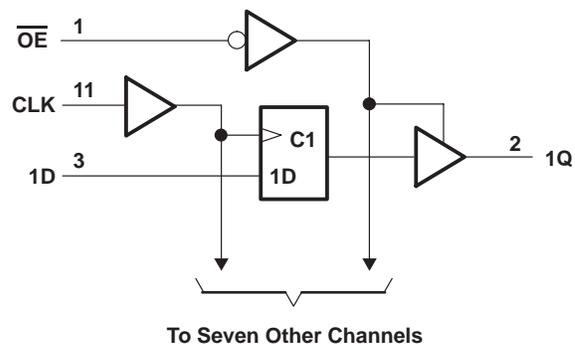
FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	$Q_0$
H	X	X	Z

## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DB, DW, J, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 35$ mA
Continuous current through $V_{CC}$ or GND	$\pm 70$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3):	
DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	$-65^\circ\text{C}$ to $150^\circ\text{C}$

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. This value is limited to 7 V maximum.

3. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils.



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## recommended operating conditions (see Note 4)

		SN54LV374		SN74LV374		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	5.5	2.7	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		2		V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		3.15		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8		V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		1.65		
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		-8		mA
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		-16		
$I_{OL}$	Low-level output current	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		8		mA
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		16		
$\Delta t/\Delta v$	Input transition rise or fall rate	0	100	0	100	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}^\dagger$	SN54LV374			SN74LV374			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OH}$	$I_{OH} = -100\ \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			$V_{CC} - 0.2$			V
	$I_{OH} = -8\ \text{mA}$	3 V	2.4			2.4			
	$I_{OH} = -16\ \text{mA}$	4.5 V	3.6			3.6			
$V_{OL}$	$I_{OL} = 100\ \mu\text{A}$	MIN to MAX	0.2			0.2			V
	$I_{OL} = 8\ \text{mA}$	3 V	0.4			0.4			
	$I_{OL} = 16\ \text{mA}$	4.5 V	0.55			0.55			
$I_I$	$V_I = V_{CC}$ or GND	3.6 V	$\pm 1$			$\pm 1$			$\mu\text{A}$
		5.5 V	$\pm 1$			$\pm 1$			
$I_{OZ}$	$V_O = V_{CC}$ or GND	3.6 V	$\pm 5$			$\pm 5$			$\mu\text{A}$
		5.5 V	$\pm 5$			$\pm 5$			
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	20			20			$\mu\text{A}$
		5.5 V	20			20			
$\Delta I_{CC}$	One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND	3 V to 3.6 V	500			500			$\mu\text{A}$
$C_i$	$V_I = V_{CC}$ or GND	3.3 V	2.5			2.5			pF
		5 V	3			3			
$C_o$	$V_O = V_{CC}$ or GND	3.3 V	7			7			pF
		5 V	8			8			

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

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# SN54LV374, SN74LV374

## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		SN54LV374						UNIT
		V <sub>CC</sub> = 5 V ± 0.5 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	45	0	40	0	35	MHz
t <sub>w</sub>	Pulse duration, CLK high or low	9		10		13		ns
t <sub>su</sub>	Setup time before CLK↑	7		10		11		ns
	High or low							
t <sub>h</sub>	Hold time, data after CLK↑	3		2		2		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		SN74LV374						UNIT
		V <sub>CC</sub> = 5 V ± 0.5 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	45	0	40	0	35	MHz
t <sub>w</sub>	Pulse duration, CLK high or low	9		10		13		ns
t <sub>su</sub>	Setup time before CLK↑	7		10		11		ns
	High or low							
t <sub>h</sub>	Hold time, data after CLK↑	3		2		2		ns

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV374						UNIT		
			V <sub>CC</sub> = 5 V ± 0.5 V			V <sub>CC</sub> = 3.3 V ± 0.3 V				V <sub>CC</sub> = 2.7 V	
			MIN	TYP	MAX	MIN	TYP	MAX		MIN	MAX
f <sub>max</sub>			45	80		40	70		35	MHz	
t <sub>pd</sub>	CLK	Q		11	19		15	24		29	ns
t <sub>en</sub>	$\overline{OE}$	Q		10	20		13	24		28	ns
t <sub>dis</sub>	$\overline{OE}$	Q		8	21		12	24		29	ns

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV374						UNIT		
			V <sub>CC</sub> = 5 V ± 0.5 V			V <sub>CC</sub> = 3.3 V ± 0.3 V				V <sub>CC</sub> = 2.7 V	
			MIN	TYP	MAX	MIN	TYP	MAX		MIN	MAX
f <sub>max</sub>			45	80		40	70		35	MHz	
t <sub>pd</sub>	CLK	Q		11	19		15	24		29	ns
t <sub>en</sub>	$\overline{OE}$	Q		10	20		13	24		28	ns
t <sub>dis</sub>	$\overline{OE}$	Q		8	21		12	24		29	ns

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**WITH 3-STATE OUTPUTS**

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operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per flip-flop	C <sub>L</sub> = 50 pF, f = 10 MHz	3.3 V	52	pF
	Outputs enabled			34	
	Outputs disabled		5 V	60	
	Outputs enabled			35	



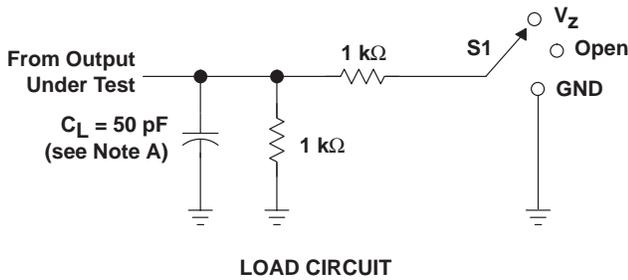
# SN54LV374, SN74LV374

## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

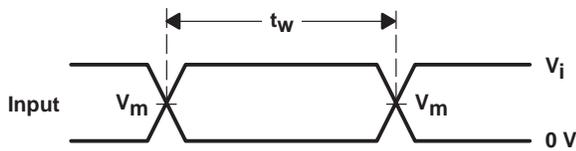
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#### PARAMETER MEASUREMENT INFORMATION

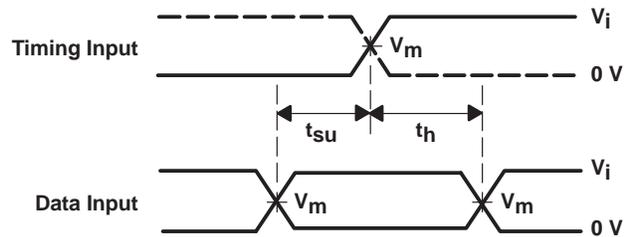


TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>Z</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

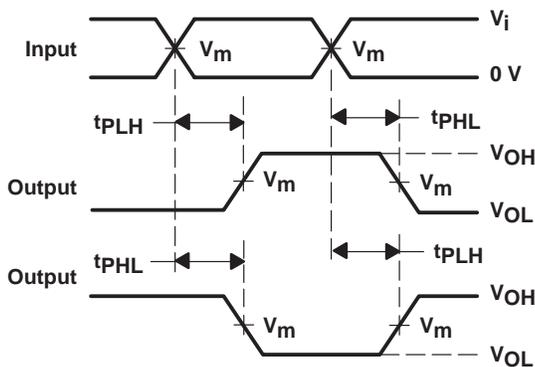
WAVEFORM CONDITION	V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> = 2.7 V to 3.6 V
V <sub>m</sub>	0.5 × V <sub>CC</sub>	1.5 V
V <sub>i</sub>	V <sub>CC</sub>	2.7 V
V <sub>Z</sub>	2 × V <sub>CC</sub>	6 V



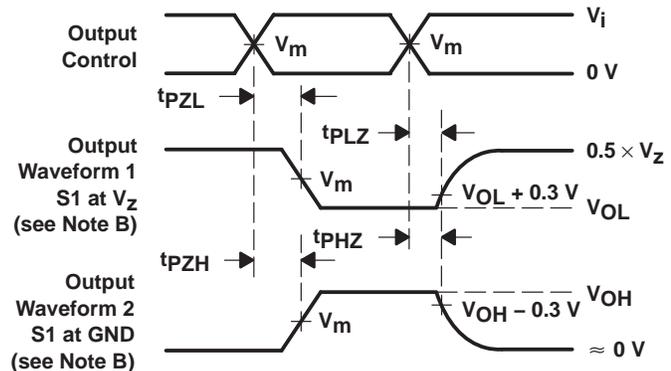
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C<sub>L</sub> includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - The outputs are measured one at a time with one transition per measurement.
  - t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.

Figure 1. Load Circuit and Voltage Waveforms



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LV374DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74LV374DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74LV374DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74LV374PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

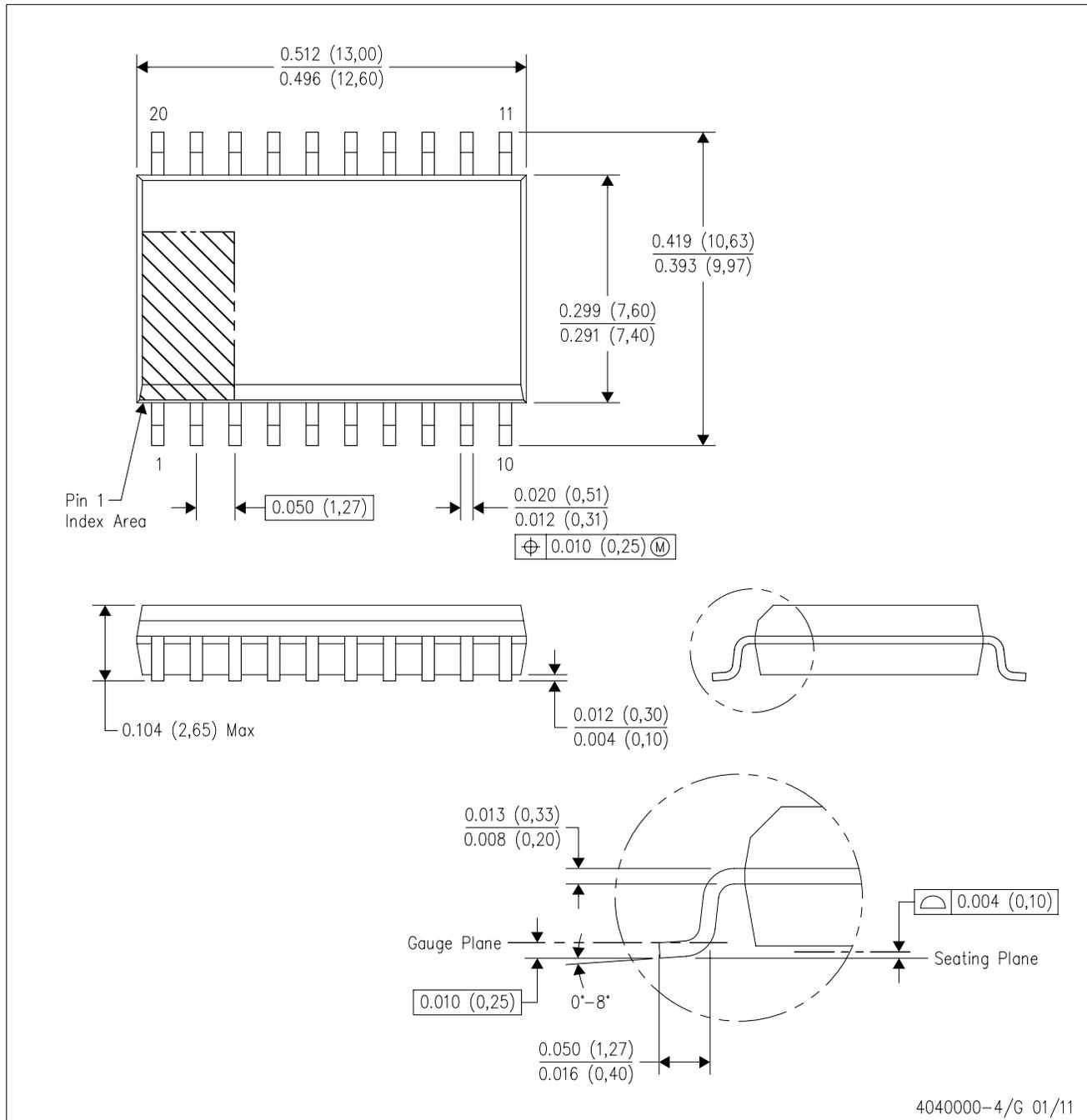
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G20)

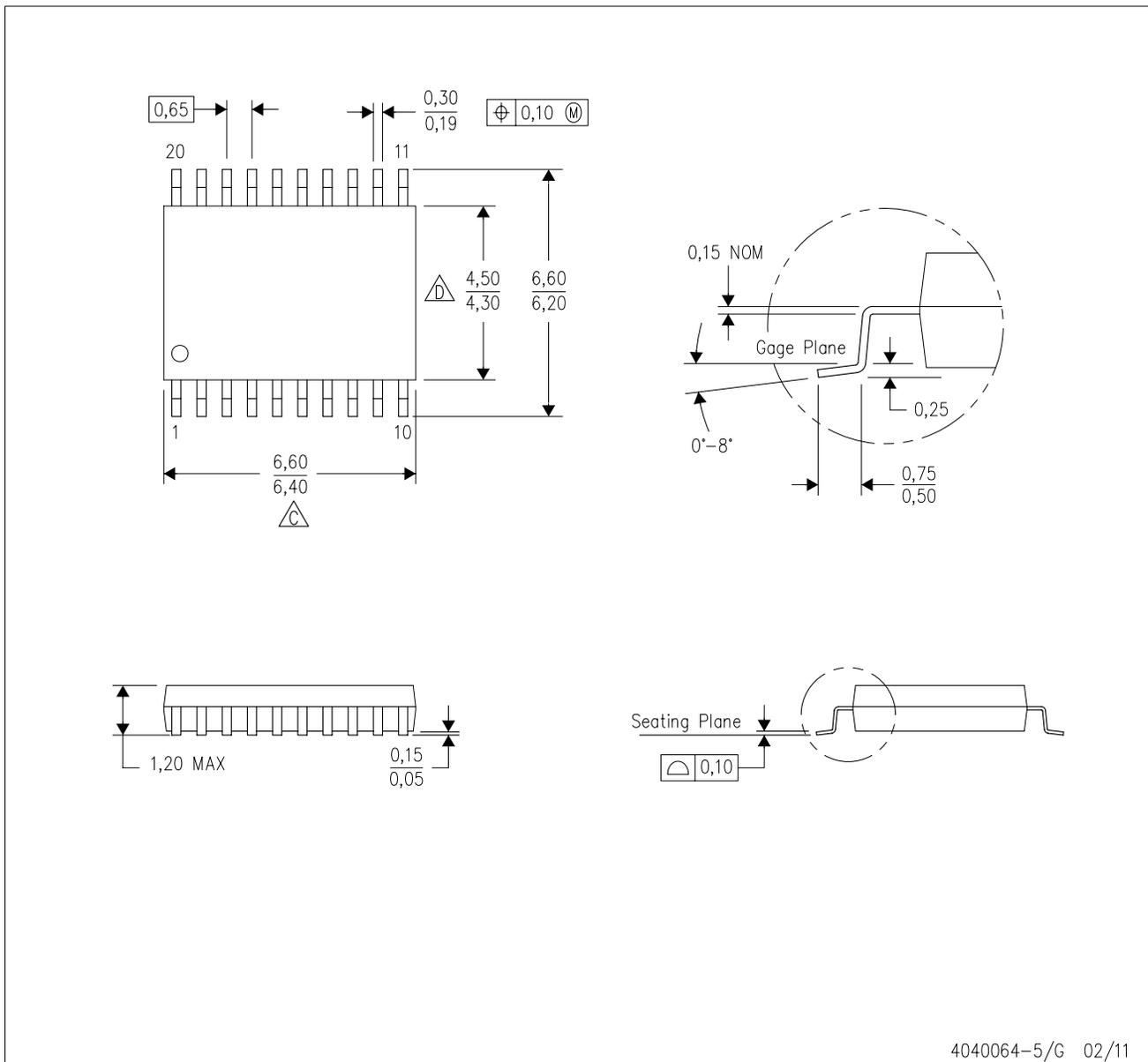
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



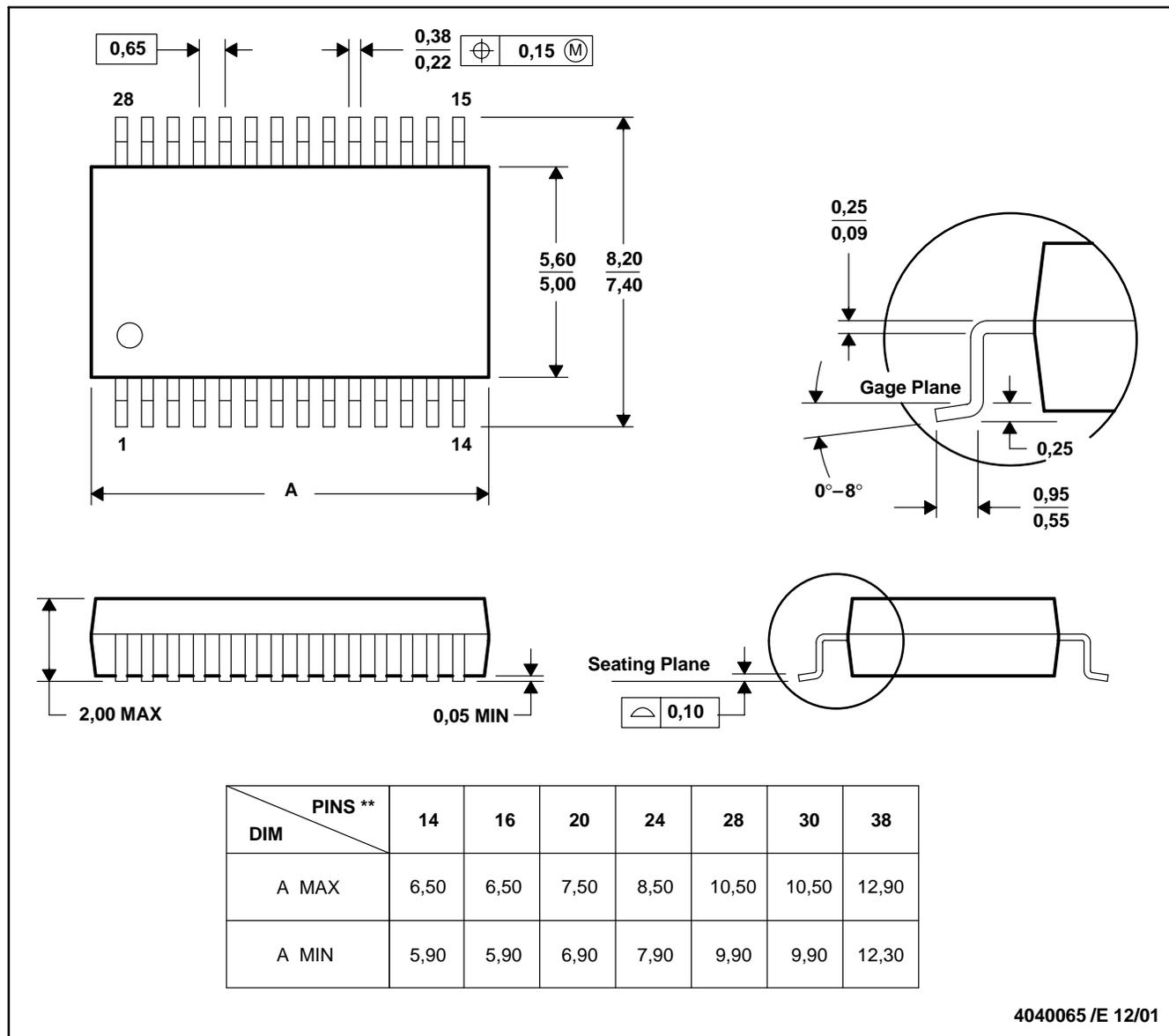
4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
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Logic	<a href="http://logic.ti.com">logic.ti.com</a>
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