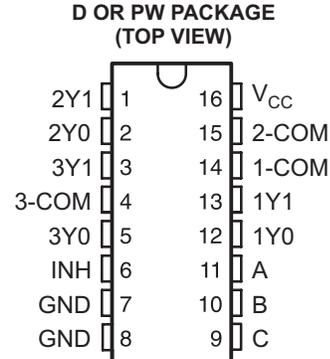


TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

Check for Samples: [SN74LV4053A-Q1](#)

FEATURES

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- 2-V to 5.5-V V_{CC} Operation
- Supports Mixed-Mode Voltage Operation on All Ports
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Individual Switch Controls
- Extremely Low Input Current



DESCRIPTION

This triple 2-channel CMOS analog multiplexer/demultiplexer is designed for 2-V to 5.5-V V_{CC} operation.

The SN74LV4053A handles both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 105°C	SOIC – D	Tape and reel	SN74LV4053ATDRQ1	L4053AQ
	TSSOP – PW	Tape and reel	SN74LV4053ATPWRQ1	L4053AQ
-40°C to 125°C	TSSOP – PW	Tape and reel	SN74LV4053AQPWRQ1	4053AQ1

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

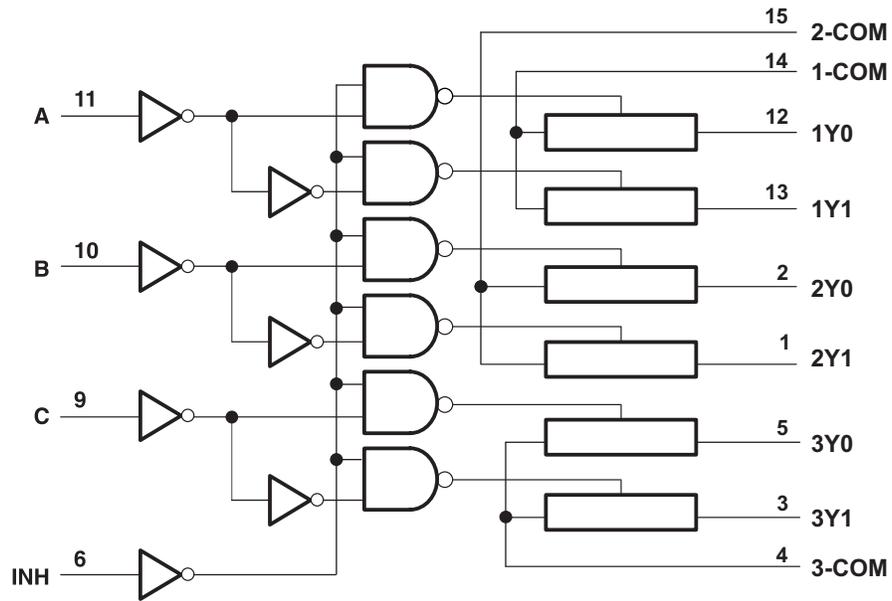
FUNCTION TABLE

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	1Y0, 2Y0, 3Y0
L	L	L	H	1Y1, 2Y0, 3Y0
L	L	H	L	1Y0, 2Y1, 3Y0
L	L	H	H	1Y1, 2Y1, 3Y0
L	H	L	L	1Y0, 2Y0, 3Y1
L	H	L	H	1Y1, 2Y0, 3Y1
L	H	H	L	1Y0, 2Y1, 3Y1
L	H	H	H	1Y1, 2Y1, 3Y1
H	X	X	X	None



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage range		–0.5 V to 7 V
V_I	Input voltage range ⁽²⁾		–0.5 V to 7 V
V_{IO}	Switch I/O voltage range ^{(2) (3)}		–0.5 V to $V_{CC} + 0.5$ V
I_{IK}	Input clamp current	$V_I < 0$	–20 mA
I_{IOK}	I/O diode current	$V_{IO} < 0$	–50 mA
I_T	Switch through current	$V_{IO} = 0$ to V_{CC}	±25 mA
	Continuous current through V_{CC} or GND		±50 mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	D package	73°C/W
		PW package	108°C/W
T_{stg}	Storage temperature range		–65°C to 150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2 ⁽²⁾	5.5	V
V_{IH}	High-level input voltage, control inputs	$V_{CC} = 2$ V	1.5		V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$		
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$		
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage, control inputs	$V_{CC} = 2$ V		0.5	V
		$V_{CC} = 2.3$ V to 2.7 V		$V_{CC} \times 0.3$	
		$V_{CC} = 3$ V to 3.6 V		$V_{CC} \times 0.3$	
		$V_{CC} = 4.5$ V to 5.5 V		$V_{CC} \times 0.3$	
V_I	Control input voltage		0	5.5	V
V_{IO}	Input/output voltage		0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V		200	ns/V
		$V_{CC} = 3$ V to 3.6 V		100	
		$V_{CC} = 4.5$ V to 5.5 V		20	
T_A	Operating free-air temperature	SN74LV4053ATDRQ1, SN74LV4053ATPWRQ1	–40	105	°C
T_A	Operating free-air temperature	SN74LV4053AQPWRQ1	–40	125	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).
- (2) With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = -40 to 105°C		T _A = -40 to 125°C		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
r _{on} On-state switch resistance	I _T = 2 mA, V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure 1)	2.3 V		41	180		225		225	Ω	
		3 V		30	150		190		190		
		4.5 V		23	75		100		100		
r _{on(p)} Peak on-state resistance	I _T = 2 mA, V _I = V _{CC} or GND, V _{INH} = V _{IL}	2.3 V		139	500		600		600	Ω	
		3 V		63	180		225		225		
		4.5 V		35	100		125		125		
Δr _{on} Difference in on-state resistance between switch	I _T = 2 mA, V _I = V _{CC} or GND, V _{INH} = V _{IL}	2.3 V		2	30		40		40	Ω	
		3 V		1.6	20		30		30		
		4.5 V		1.3	15		20		20		
I _I Control input current	V _I = 5.5 V or GND	0 V to 5.5 V				±0.1		±1		±2	μA
I _{S(off)} Off-state switch leakage current	V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _{INH} = V _{IH} (see Figure 2)	5.5 V				±0.1		±1		±2	μA
I _{S(on)} On-state switch leakage current	V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure 3)	5.5 V				±0.1		±1		±2	μA
I _{CC} Supply current	V _I = V _{CC} or GND	5.5 V						20		40	μA
C _{IC} Control input capacitance	f = 10 MHz	3.3 V				2					pF
C _{IS} Common terminal capacitance		3.3 V				8.2					pF
C _{OS} Switch terminal capacitance		3.3 V				5.6					pF
C _F Feedthrough capacitance						0.5					pF

SWITCHING CHARACTERISTICS

V_{CC} = 3.3 V ± 0.3 V, over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			T _A = -40 to 105°C		T _A = -40 to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} Propagation delay time t _{PHL}	COM or Y _n	Y _n or COM	C _L = 50 pF (see Figure 4)		2.9	9		12		14	ns
t _{PZH} Enable delay time t _{PZL}	INH	COM or Y _n	C _L = 50 pF (see Figure 5)		6.1	20		25		25	ns
t _{PHZ} Disable delay time t _{PLZ}	INH	COM or Y _n	C _L = 50 pF (see Figure 5)		8.9	20		25		25	ns

SWITCHING CHARACTERISTICS

 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			$T_A = -40\text{ to }105^\circ\text{C}$		$T_A = -40\text{ to }125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} Propagation delay time t_{PHL}	COM or Yn	Yn or COM	$C_L = 50\text{ pF}$ (see Figure 4)		1.8	6		8		10	ns
t_{PZH} Enable delay time t_{PZL}	INH	COM or Yn	$C_L = 50\text{ pF}$ (see Figure 5)		4.3	14		18		18	ns
t_{PHZ} Disable delay time t_{PLZ}	INH	COM or Yn	$C_L = 50\text{ pF}$ (see Figure 5)		6.3	14		18		18	ns

ANALOG SWITCH CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			UNIT
					MIN	TYP	MAX	
Frequency response (switch on)	COM or Yn	Yn or COM	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) ⁽¹⁾ (see Figure 6)	2.3 V		30	MHz	
				3 V		35		
				4.5 V		50		
Crosstalk (between any switches)	COM or Yn	Yn or COM	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 7)	2.3 V		-45	dB	
				3 V		-45		
				4.5 V		-45		
Crosstalk (control input to signal output)	INH	COM or Yn	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (square wave) (see Figure 8)	2.3 V		20	mV	
				3 V		35		
				4.5 V		65		
Feedthrough attenuation (switch off)	COM or Yn	Yn or COM	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ ⁽²⁾ (see Figure 9)	2.3 V		-45	dB	
				3 V		-45		
				4.5 V		-45		
Sine-wave distortion	COM or Yn	Yn or COM	$C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$, $f_{in} = 1\text{ kHz}$ (sine wave) (see Figure 10)	$V_I = 2\text{ Vp-p}$	2.3 V	0.1	%	
				$V_I = 2.5\text{ Vp-p}$	3 V	0.1		
				$V_I = 4\text{ Vp-p}$	4.5 V	0.1		

 (1) Adjust f_{in} voltage to obtain 0-dBm output. Increase f_{in} frequency until dB meter reads -3 dB.

 (2) Adjust f_{in} voltage to obtain 0-dBm input.

OPERATING CHARACTERISTICS

 $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	5.3	pF

PARAMETER MEASUREMENT INFORMATION

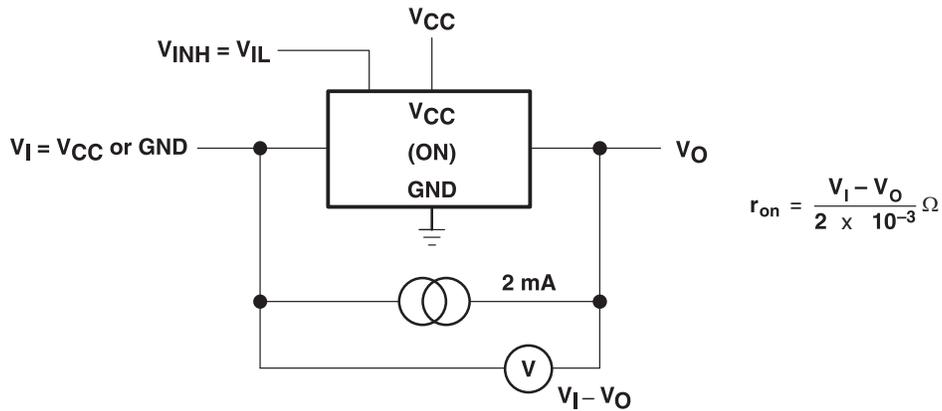


Figure 1. On-State Resistance Test Circuit

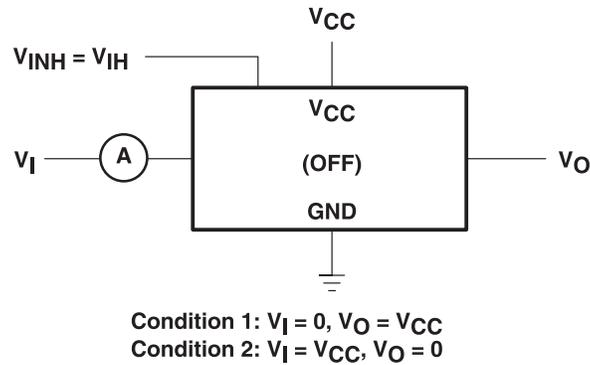


Figure 2. Off-State Switch Leakage-Current Test Circuit

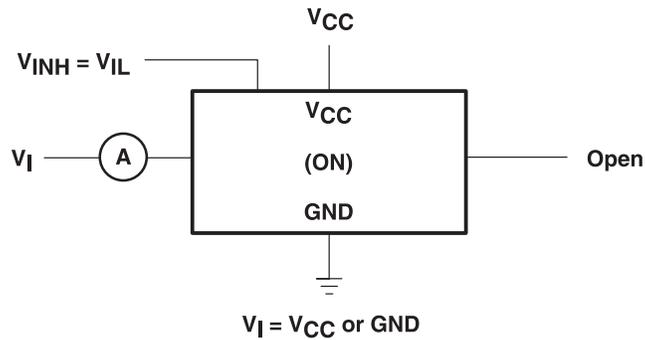


Figure 3. On-State Switch Leakage-Current Test Circuit

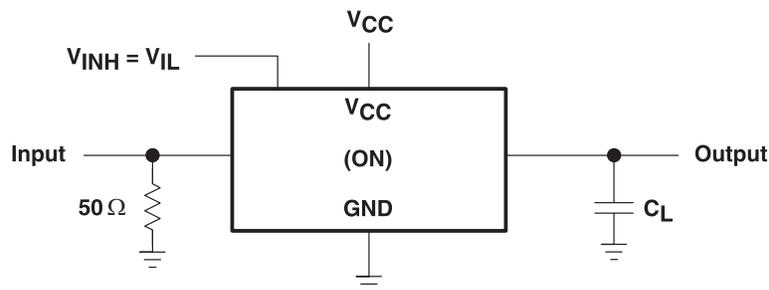
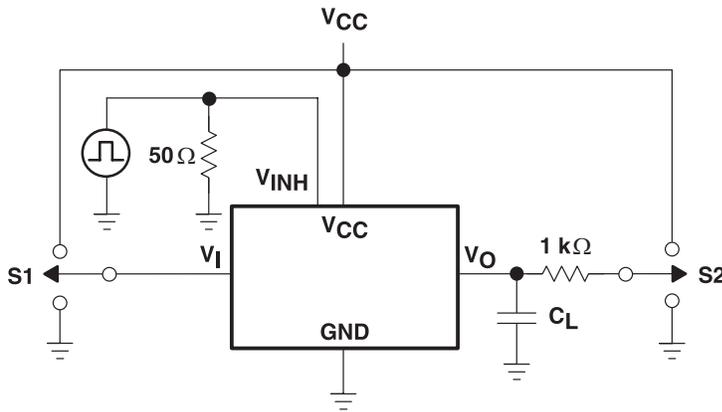


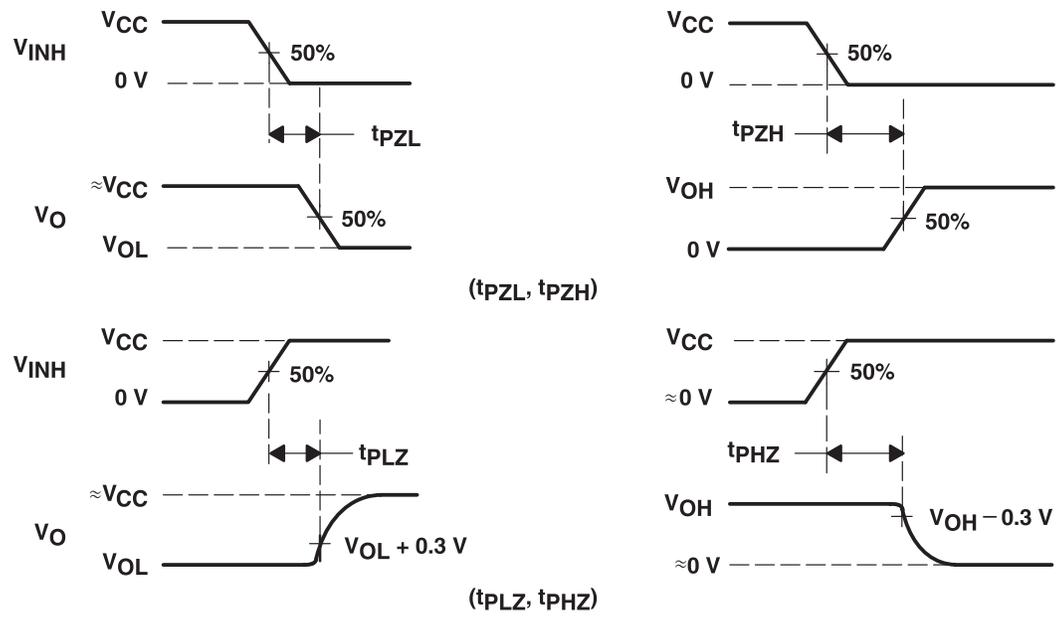
Figure 4. Propagation Delay Time, Signal Input to Signal Output

PARAMETER MEASUREMENT INFORMATION (continued)



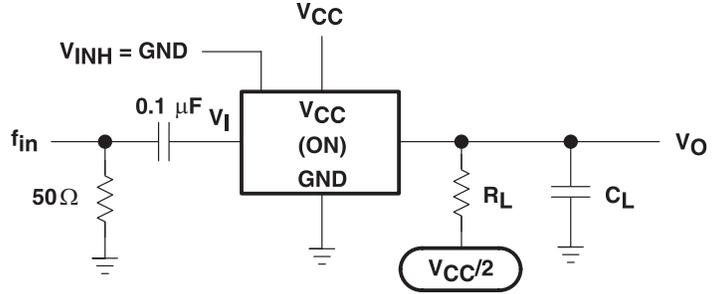
TEST	S1	S2
t_{PLZ}/t_{PZL}	GND	V_{CC}
t_{PHZ}/t_{PZH}	V_{CC}	GND

TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 5. Switching Time (t_{PZL} , t_{PLZ} , t_{PZH} , t_{PHZ}), Control to Signal Output



NOTE A: f_{in} is a sine wave.

Figure 6. Frequency Response (Switch On)

PARAMETER MEASUREMENT INFORMATION (continued)

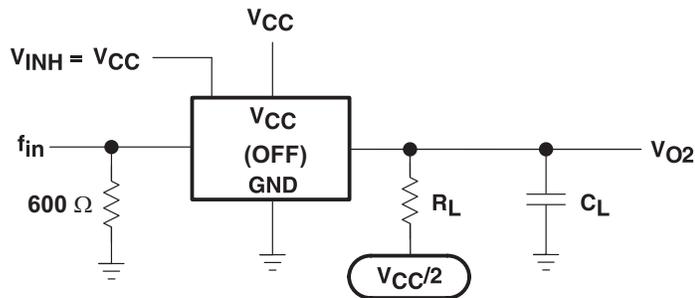
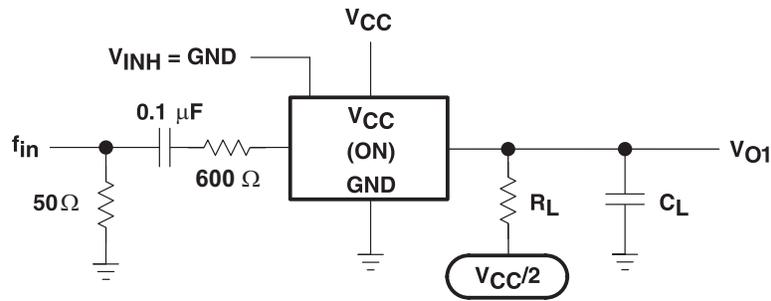


Figure 7. Crosstalk Between Any Two Switches

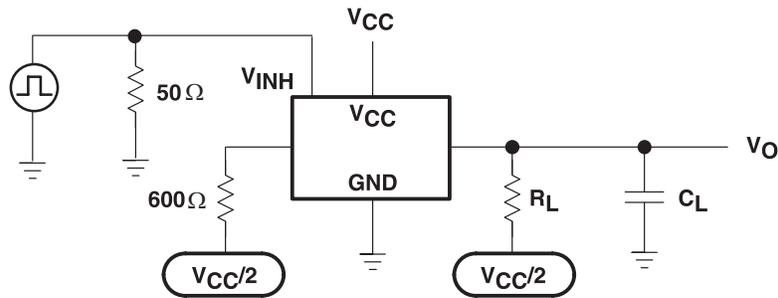


Figure 8. Crosstalk Between Control Input and Switch Output

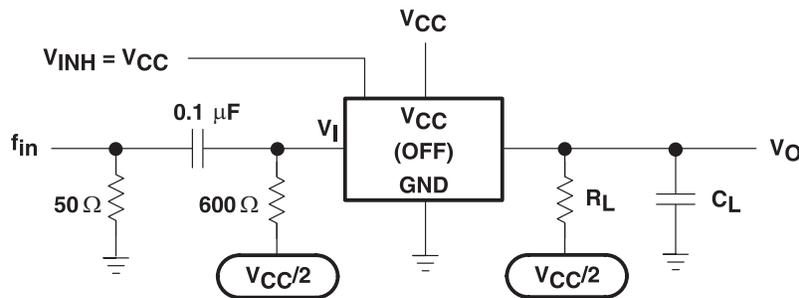


Figure 9. Feedthrough Attenuation (Switch Off)

PARAMETER MEASUREMENT INFORMATION (continued)

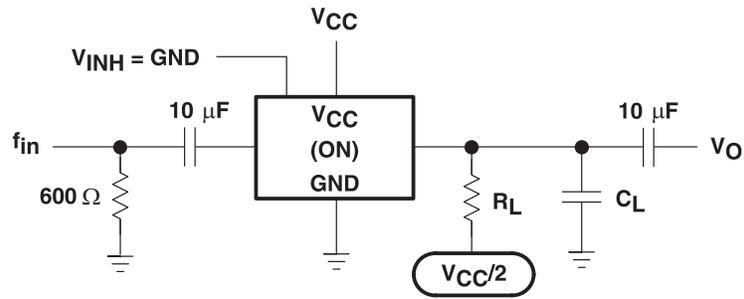


Figure 10. Sine-Wave Distortion

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CLV4053ATPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV4053AQPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV4053ATDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV4053ATPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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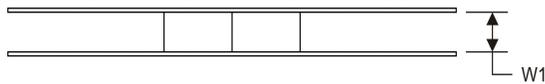
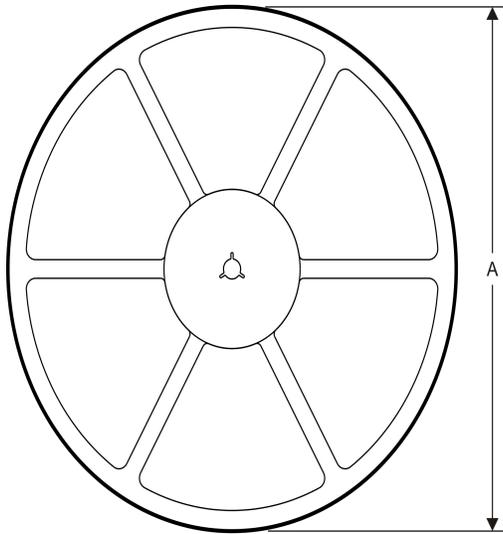
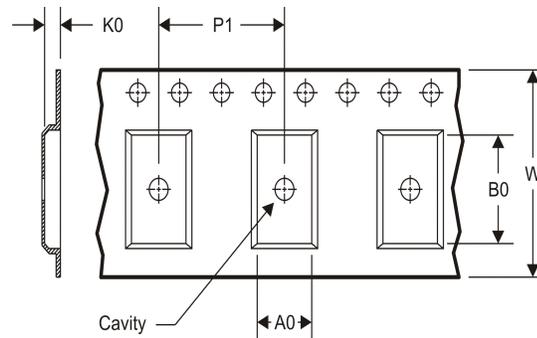
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV4053A-Q1 :

- Catalog: [SN74LV4053A](#)
- Enhanced Product: [SN74LV4053A-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


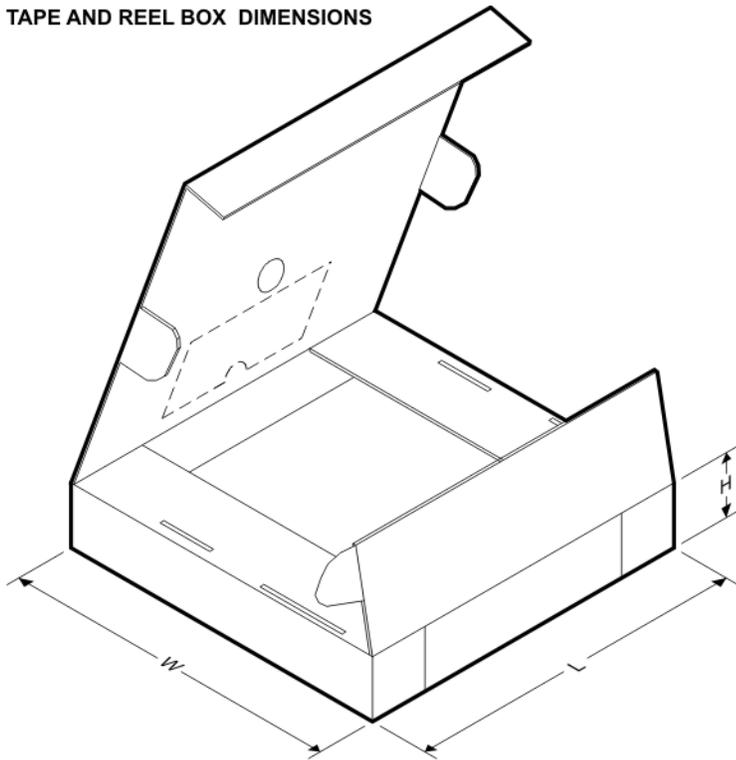
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4053AQPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

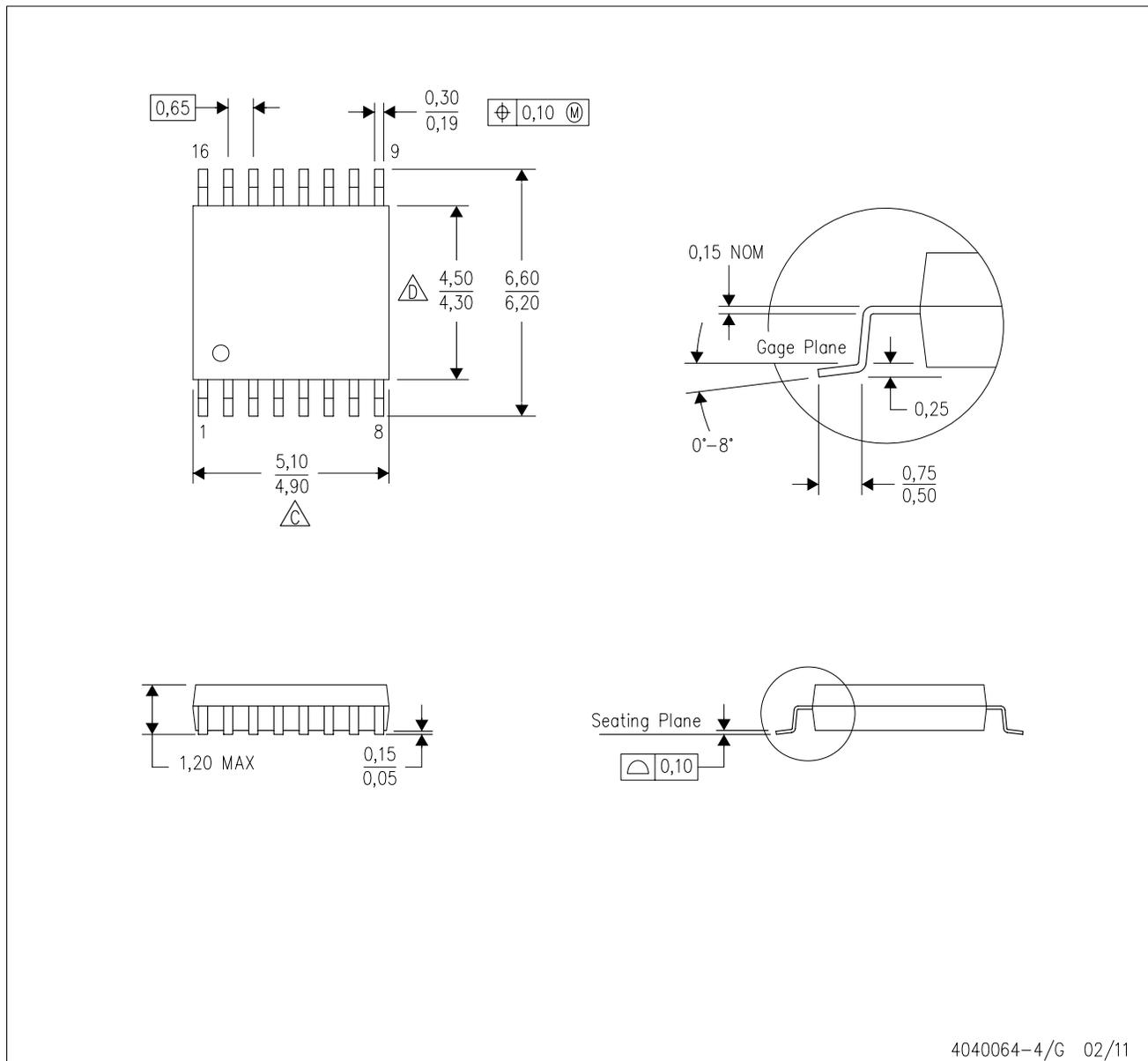


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4053AQPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

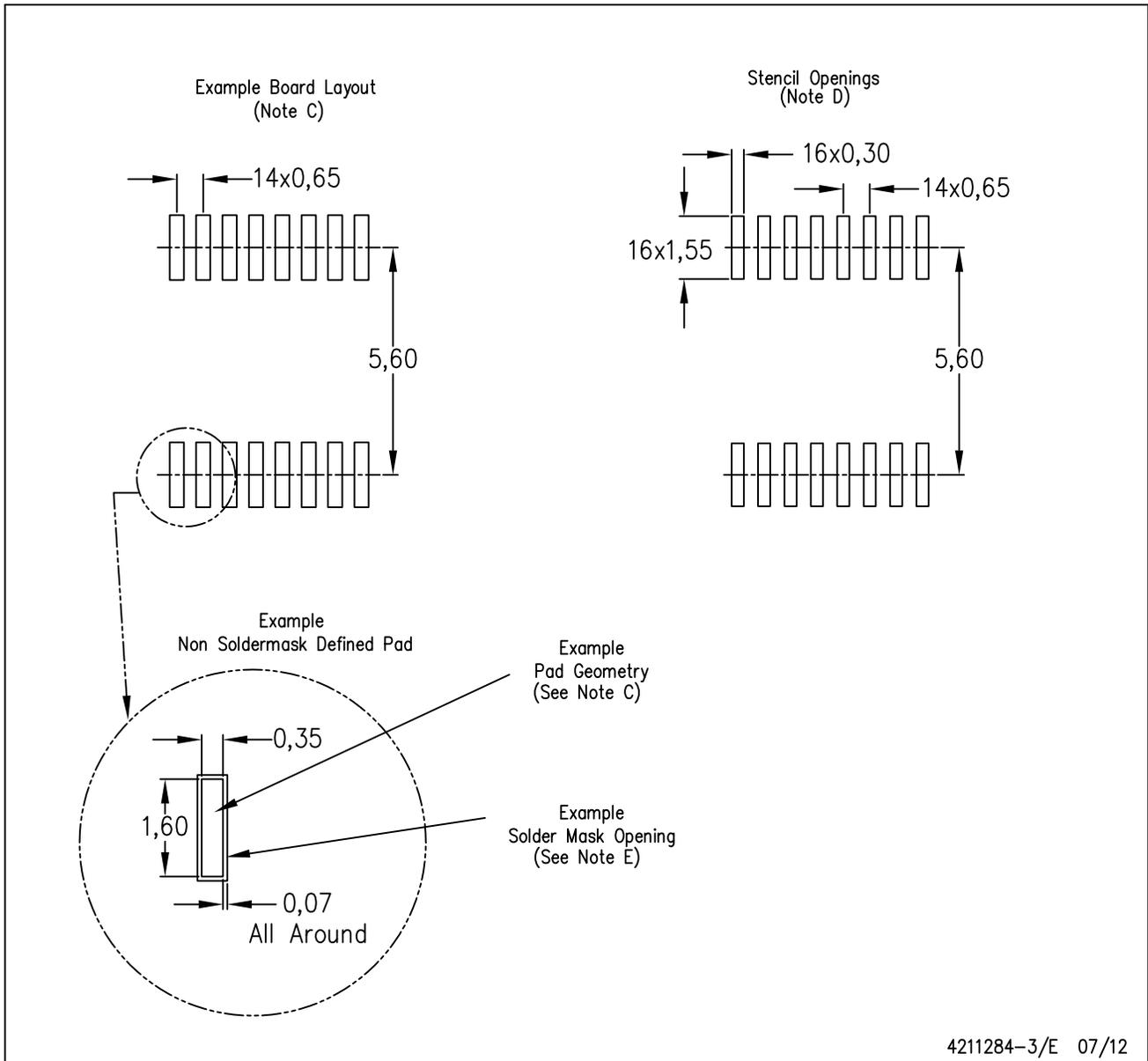


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

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