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SN74LVC32245
32-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS
SCES343D−OCTOBER 2000−REVISED APRIL 2005

FEATURES

- **Member of the Texas Instruments Widebus+™ Family**
- **Operates From 1.65 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 4 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**

- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**

DESCRIPTION/ORDERING INFORMATION

This 32-bit noninverting bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC32245 is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as four 8-bit transceivers, two 16-bit transceivers, or one 32-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	LFBGA – GKE	Tape and reel	SN74LVC32245GKER	NC245
	LFBGA – ZKE (Pb-free)		SN74LVC32245ZKER	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
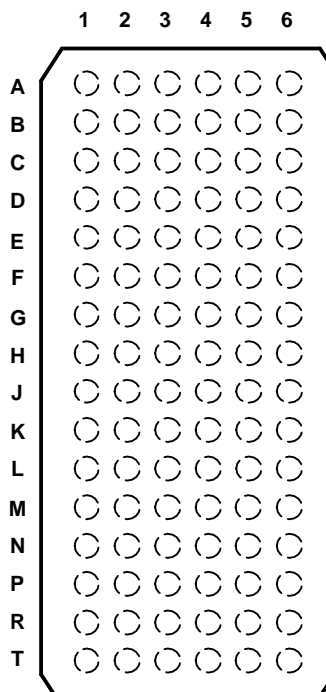
![warning triangle symbol] Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
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GKE OR ZKE PACKAGE
(TOP VIEW)

TERMINAL ASSIGNMENTS

	1	2	3	4	5	6
A	1B2	1B1	1DIR	1$\overline{\text{OE}}$	1A1	1A2
B	1B4	1B3	GND	GND	1A3	1A4
C	1B6	1B5	V_{CC}	V_{CC}	1A5	1A6
D	1B8	1B7	GND	GND	1A7	1A8
E	2B2	2B1	GND	GND	2A1	2A2
F	2B4	2B3	V_{CC}	V_{CC}	2A3	2A4
G	2B6	2B5	GND	GND	2A5	2A6
H	2B7	2B8	2DIR	2$\overline{\text{OE}}$	2A8	2A7
J	3B2	3B1	3DIR	3$\overline{\text{OE}}$	3A1	3A2
K	3B4	3B3	GND	GND	3A3	3A4
L	3B6	3B5	V_{CC}	V_{CC}	3A5	3A6
M	3B8	3B7	GND	GND	3A7	3A8
N	4B2	4B1	GND	GND	4A1	4A2
P	4B4	4B3	V_{CC}	V_{CC}	4A3	4A4
R	4B6	4B5	GND	GND	4A5	4A6
T	4B7	4B8	4DIR	4$\overline{\text{OE}}$	4A8	4A7

FUNCTION TABLE
(EACH 8-BIT SECTION)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

LOGIC DIAGRAM (POSITIVE LOGIC)

To Seven Other Channels

To Seven Other Channels

To Seven Other Channels

To Seven Other Channels

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Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6.5	V
V_I	Input voltage range[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2][3]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[4]	GKE/ZKE package		40	°C/W
T_{stg}	Storage temperature range		−65	150	°C

(1)   Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2)   The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3)   The value of V_{CC} is provided in the recommended operating conditions table.
(4)   The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V		−4	mA
		V_{CC} = 2.3 V		−8	
		V_{CC} = 2.7 V		−12	
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			5	ns/V
T_A	Operating free-air temperature		−40	85	°C

(1)   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{OH}		$I_{OH} = -100$ μA		1.65 V to 3.6 V	$V_{CC} - 0.2$			V
		$I_{OH} = -4$ mA		1.65 V	1.2			
		$I_{OH} = -8$ mA		2.3 V	1.7			
		$I_{OH} = -12$ mA		2.7 V	2.2			
				3 V	2.4			
		$I_{OH} = -24$ mA		3 V	2.2			
V_{OL}		$I_{OL} = 100$ μA		1.65 V to 3.6 V			0.2	V
		$I_{OL} = 4$ mA		1.65 V			0.45	
		$I_{OL} = 8$ mA		2.3 V			0.7	
		$I_{OL} = 12$ mA		2.7 V			0.4	
		$I_{OL} = 24$ mA		3 V			0.55	
I_I	Control inputs	$V_I = 0$ to 5.5 V		3.6 V			±5	μA
I_{off}		V_I or $V_O = 5.5$ V		0			±10	μA
I_{OZ}[2]		$V_O = 0$ to 5.5 V		2.3 V to 3.6 V			±5	μA
I_{CC}		$V_I = V_{CC}$ or GND	$I_O = 0$	3.6 V			20	μA
		3.6 V $\leq V_I \leq 5.5$ V[3]					20	
ΔI_{CC}		One input at $V_{CC} - 0.6$ V,	Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND		3.3 V		5		pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		7.5		pF

(1) All typical values are at $V_{CC} = 3.3$ V, $T_A = 25°C$.
(2) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(3) This applies in the disabled state only.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8$ V ± 0.15 V		$V_{CC} = 2.5$ V ± 0.2 V		$V_{CC} = 2.7$ V		$V_{CC} = 3.3$ V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	1.5	7.1	1	4.5	1	4.7	1	4	ns
t_{en}	$\overline{OE}$	A or B	1.5	8.9	1	5.6	1.5	6.7	1.5	5.5	ns
t_{dis}	$\overline{OE}$	A or B	1.5	11.9	1	6.8	1.5	7.1	1.5	6.6	ns
$t_{sk(o)}$										1	ns

Operating Characteristics

$T_A = 25°C$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8$ V	$V_{CC} = 2.5$ V	$V_{CC} = 3.3$ V	UNIT
			TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	34	37	38	pF
		Outputs disabled	3	3	4	

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PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V

**VOLTAGE WAVEFORMS
PULSE DURATION**
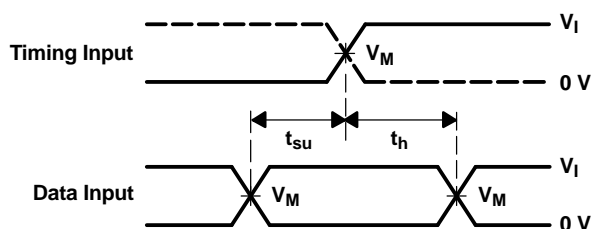
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**
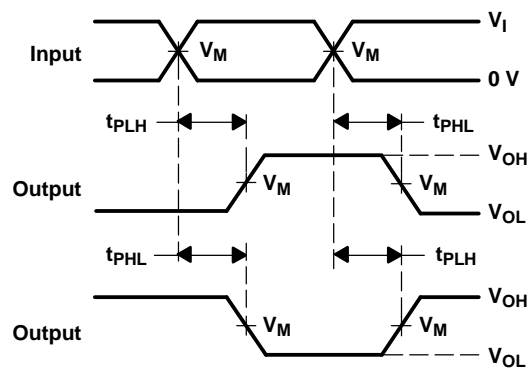
**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**
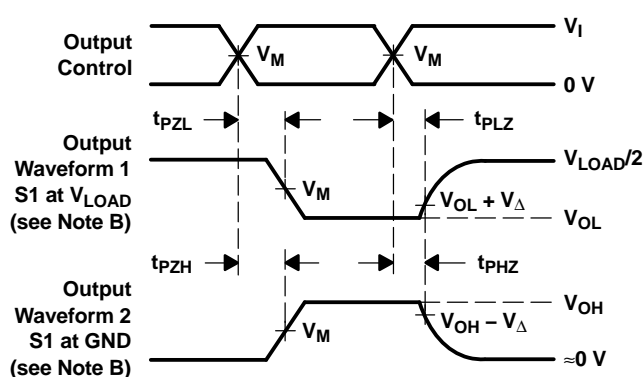
**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

![Texas Instruments logo]

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74LVC32245GKER	NRND	LFBGA	GKE	96	1000	TBD	SNPB	Level-2-235C-1 YEAR	-40 to 85	NC245	
SN74LVC32245ZKER	ACTIVE	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	NC245	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC32245GKER	LFBGA	GKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1
SN74LVC32245ZKER	LFBGA	ZKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC32245GKER	LFBGA	GKE	96	1000	333.2	345.9	31.8
SN74LVC32245ZKER	LFBGA	ZKE	96	1000	333.2	345.9	31.8
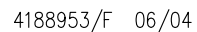
GKE (R−PBGA−N96)   PLASTIC BALL GRID ARRAY

5,60
5,40

4,00

0,80

0,40

13,60
13,40

T
R
P
N
M
L
K
J
H
G
F
E
D
C
B
A

0,80

12,00

0,40

1   2   3   4   5   6

Bottom View

A1 Corner

0,95
0,85

0,12

1,40 Max

Seating Plane

96X Ø $\frac{0,55}{0,45}$

0,45
0,35

⊕ Ø 0,08 Ⓜ

4188953/F 06/04

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MO−205 variation CC.
         D.   This package is tin−lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead−free.

ZKE (R−PBGA−N96)   PLASTIC BALL GRID ARRAY
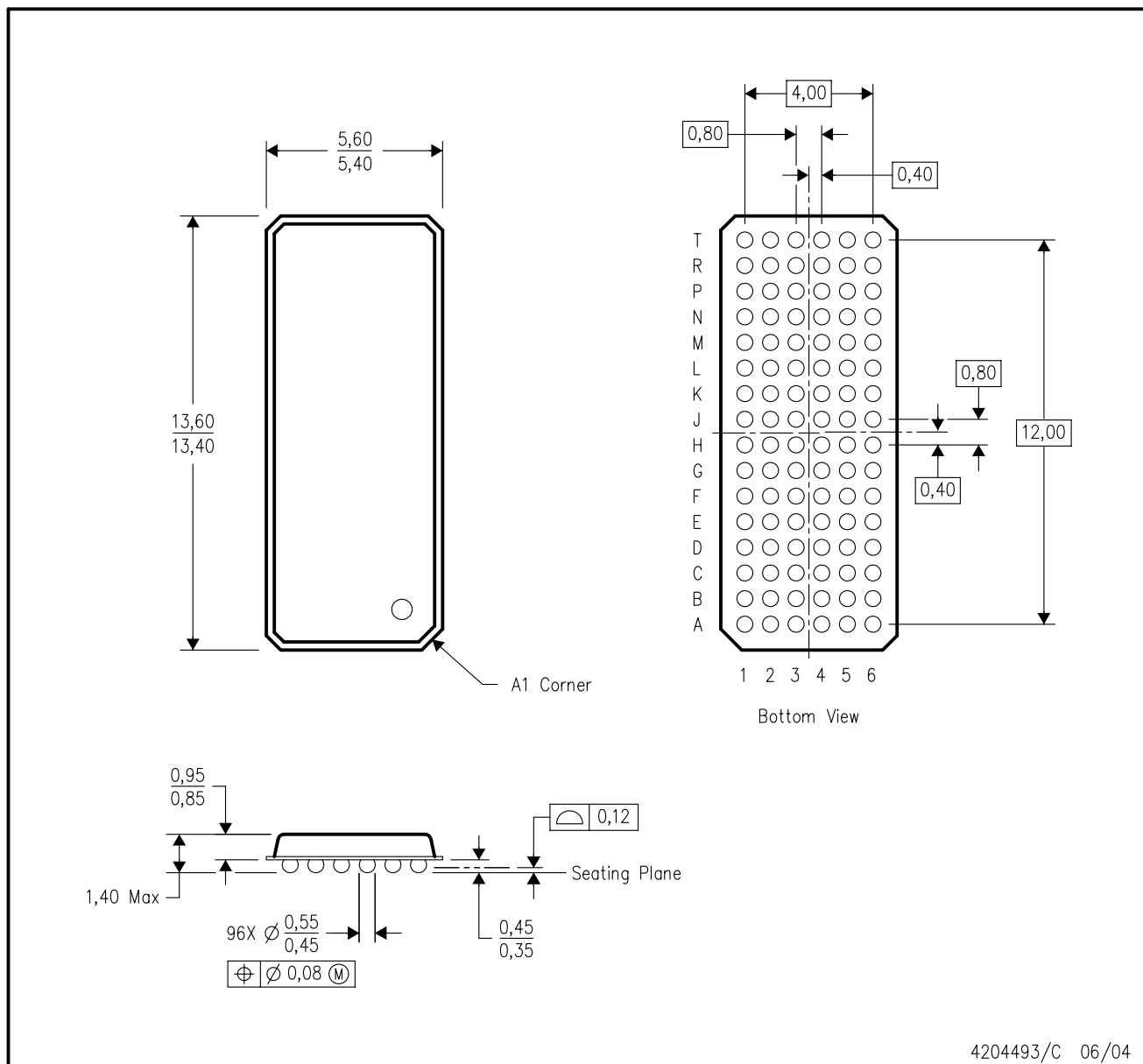
A1 Corner

Bottom View

Seating Plane

4204493/C 06/04

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MO−205 variation CC.
         D.   This package is lead−free. Refer to the 96 GKE package (drawing 4188953) for tin−lead (SnPb).

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