SN74LVCH16543A
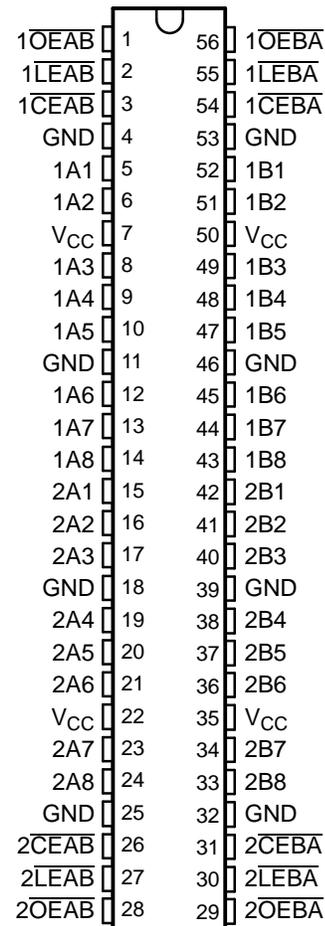# 16-BIT REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS

FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **Operates From 1.65 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 5.4 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **– 2000-V Human-Body Model (A114-A)**
  - **– 200-V Machine Model (A115-A)**
  - **– 1000-V Charged-Device Model (C101)**

DESCRIPTION/ORDERING INFORMATION

This 16-bit registered transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCH16543A can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register, to permit independent control in either direction of data flow.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)

Pin	Left		Right	Pin
1	1$\overline{OEAB}$		1$\overline{OEBA}$	56
2	1$\overline{LEAB}$		1$\overline{LEBA}$	55
3	1$\overline{CEAB}$		1$\overline{CEBA}$	54
4	GND		GND	53
5	1A1		1B1	52
6	1A2		1B2	51
7	V_{CC}		V_{CC}	50
8	1A3		1B3	49
9	1A4		1B4	48
10	1A5		1B5	47
11	GND		GND	46
12	1A6		1B6	45
13	1A7		1B7	44
14	1A8		1B8	43
15	2A1		2B1	42
16	2A2		2B2	41
17	2A3		2B3	40
18	GND		GND	39
19	2A4		2B4	38
20	2A5		2B5	37
21	2A6		2B6	36
22	V_{CC}		V_{CC}	35
23	2A7		2B7	34
24	2A8		2B8	33
25	GND		GND	32
26	2$\overline{CEAB}$		2$\overline{CEBA}$	31
27	2$\overline{LEAB}$		2$\overline{LEBA}$	30
28	2$\overline{OEAB}$		2$\overline{OEBA}$	29

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP – DL	Tube	SN74LVCH16543ADL	LVCH16543A
		Tape and reel	SN74LVCH16543ADLR	
	TSSOP – DGG	Tape and reel	SN74LVCH16543ADGGR	LVCH16543A
	TVSOP – DGV	Tape and reel	SN74LVCH16543ADGVR	LDH543A
	VFBGA – GQL	Tape and reel	SN74LVCH16543AGQLR	LDH543A
	VFBGA – ZQL (Pb-free)		SN74LVCH16543AZQLR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The A-to-B enable ($\overline{\text{CEAB}}$) input must be low to enter data from A or to output data from B. If $\overline{\text{CEAB}}$ is low and $\overline{\text{LEAB}}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{\text{LEAB}}$ puts the A latches in the storage mode. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended. The bus-hold circuitry is part of the input circuit and is not disabled by $\overline{\text{OE}}$ or DIR.

GQL OR ZQL PACKAGE
(TOP VIEW)
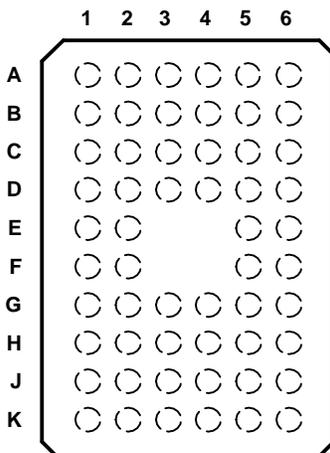
TERMINAL ASSIGNMENTS

	1	2	3	4	5	6
A	1$\overline{\text{CEAB}}$	1$\overline{\text{LEAB}}$	1$\overline{\text{OEAB}}$	1$\overline{\text{OEBA}}$	1$\overline{\text{LEBA}}$	1$\overline{\text{CEBA}}$
B	1A2	1A1	GND	GND	1B1	1B2
C	1A4	1A3	V_{CC}	V_{CC}	1B3	1B4
D	1A6	1A5	GND	GND	1B5	1B6
E	1A8	1A7			1B7	1B8
F	2A1	2A2			2B2	2B1
G	2A3	2A4	GND	GND	2B4	2B3
H	2A5	2A6	V_{CC}	V_{CC}	2B6	2B5
J	2A7	2A8	GND	GND	2B8	2B7
K	2$\overline{\text{CEAB}}$	2$\overline{\text{LEAB}}$	2$\overline{\text{OEAB}}$	2$\overline{\text{OEBA}}$	2$\overline{\text{LEBA}}$	2$\overline{\text{CEBA}}$

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FUNCTION TABLE[1]
(EACH 8-BIT SECTION)

INPUTS				OUTPUT B
$\overline{\text{CEAB}}$	$\overline{\text{LEAB}}$	$\overline{\text{OEAB}}$	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0[2]
L	L	L	L	L
L	L	L	H	H

(1) A-to-B data flow is shown; B-to-A flow control is the same, except that it uses $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$.
(2) Output level before the indicated steady-state input conditions were established

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LOGIC DIAGRAM (POSITIVE LOGIC)

To Seven Other Channels

To Seven Other Channels
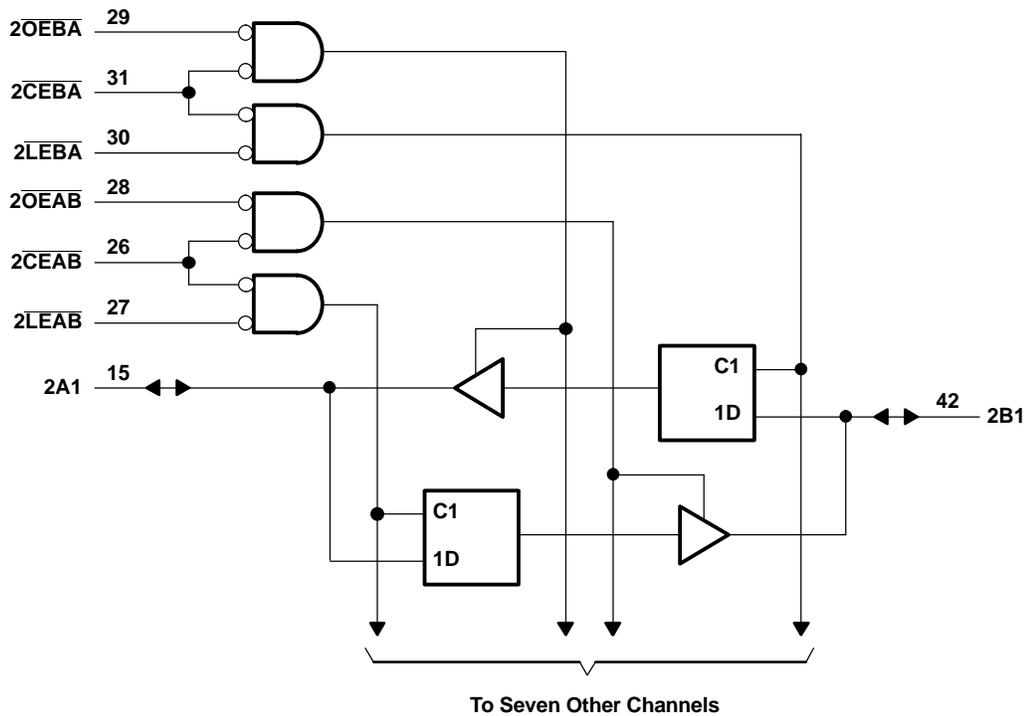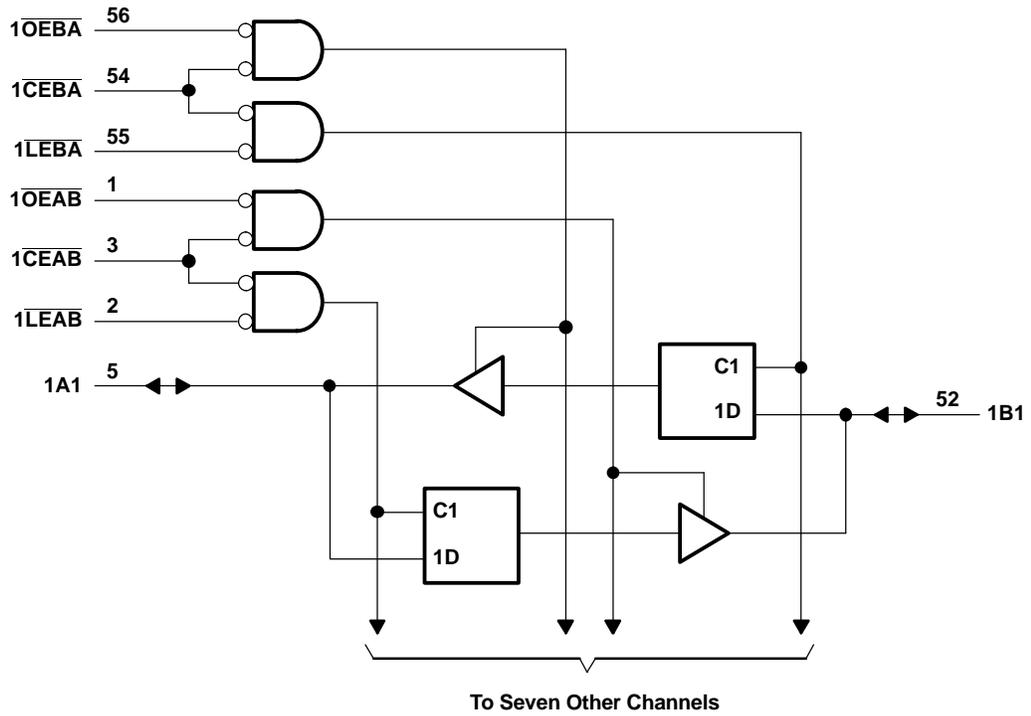
Pin numbers shown are for the DGG, DGV, and DL packages.

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Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6.5	V
V_I	Input voltage range[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2][3]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		−50	mA
I_{OK}	Output clamp current	V_O < 0		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[4]	DGG package		64	°C/W
		DGV package		48	
		DL package		56	
		GQL/ZQL package		42	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V		−4	mA
		V_{CC} = 2.3 V		−8	
		V_{CC} = 2.7 V		−12	
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		−40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{OH}		$I_{OH} = -100\ \mu A$	1.65 V to 3.6 V	$V_{CC} - 0.2$			V
		$I_{OH} = -4$ mA	1.65 V	1.2			
		$I_{OH} = -8$ mA	2.3 V	1.7			
		$I_{OH} = -12$ mA	2.7 V	2.2			
			3 V	2.4			
		$I_{OH} = -24$ mA	3 V	2.2			
V_{OL}		$I_{OL} = 100\ \mu A$	1.65 V to 3.6 V			0.2	V
		$I_{OL} = 4$ mA	1.65 V			0.45	
		$I_{OL} = 8$ mA	2.3 V			0.7	
		$I_{OL} = 12$ mA	2.7 V			0.4	
		$I_{OL} = 24$ mA	3 V			0.55	
I_I	Control inputs	$V_I = 0$ to 5.5 V	3.6 V			±5	µA
I_{off}		V_I or $V_O = 5.5$ V	0			±10	µA
$I_{I(hold)}$	A or B ports	$V_I = 0.58$ V	1.65 V		(2)		µA
		$V_I = 1.07$ V			(2)		
		$V_I = 0.7$ V	2.3 V		45		
		$V_I = 1.7$ V			−45		
		$V_I = 0.8$ V	3 V		75		
		$V_I = 2$ V			−75		
		$V_I = 0$ to 3.6 V [3]	3.6 V			±500	
I_{OZ} [4]		$V_O = 0$ V or (V_{CC} to 5.5 V)	2.3 V to 3.6 V			±5	µA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	µA
		$3.6\ V \le V_I \le 5.5\ V$ [5], $I_O = 0$				20	
ΔI_{CC}		One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500	µA
C_i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V		5		pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V		8		pF

(1)   All typical values are at $V_{CC} = 3.3$ V, $T_A = 25°C$.
(2)   This information was not available at the time of publication.
(3)   This is the bus-hold maximum dynamic current required to switch the input from one state to another.
(4)   For the total leakage current in an I/O port, consult the $I_{I(hold)}$ specification for the input voltage condition, 0 V < V_I < V_{CC}, and the I_{OZ} specification for the input voltage conditions, $V_I = 0$ V or $V_I = V_{CC}$ to 5.5 V. The bus-hold current, at input voltage greater than V_{CC}, is negligible.
(5)   This applies in the disabled state only.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		$V_{CC} = 1.8$ V ± 0.15 V		$V_{CC} = 2.5$ V ± 0.2 V		$V_{CC} = 2.7$ V		$V_{CC} = 3.3$ V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LE}$ or $\overline{CE}$ low	(1)		(1)		3.3		3.3		ns
t_{su}	Setup time, data before $\overline{LE}$ or $\overline{CE}\downarrow$	(1)		(1)		1.1		1.1		ns
t_h	Hold time, data after $\overline{LE}$ or $\overline{CE}\downarrow$	(1)		(1)		1.9		1.9		ns

(1)   This information was not available at the time of publication.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	(1)	(1)	(1)	(1)		6.1	1.2	5.4	ns
	$\overline{LE}$	A or B	(1)	(1)	(1)	(1)		7.4	1.5	6.1	
t_{en}	$\overline{CE}$	A or B	(1)	(1)	(1)	(1)		7.9	1.2	6.6	ns
t_{dis}			(1)	(1)	(1)	(1)		7.1	1.5	6.6	
t_{en}	$\overline{OE}$	A or B	(1)	(1)	(1)	(1)		7.6	1	6.3	ns
t_{dis}			(1)	(1)	(1)	(1)		6.9	1.5	6.3	

(1)   This information was not available at the time of publication.

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	(1)	(1)	44	pF
		Outputs disabled	(1)	(1)	4	

with test conditions f = 10 MHz spanning both rows.

(1)   This information was not available at the time of publication.

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PARAMETER MEASUREMENT INFORMATION
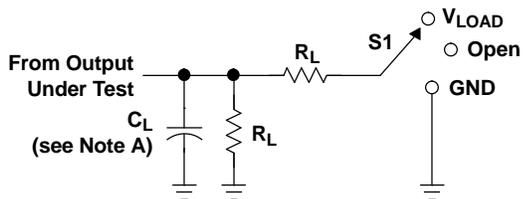
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V $\pm$ 0.15 V	V_{CC}	$\leq$2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V $\pm$ 0.2 V	V_{CC}	$\leq$2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq$2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V $\pm$ 0.3 V	2.7 V	$\leq$2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
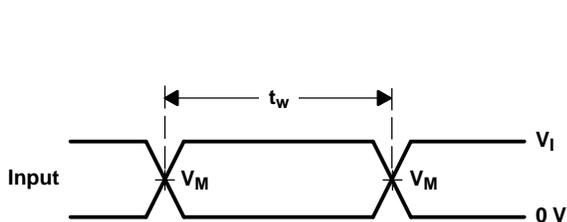
VOLTAGE WAVEFORMS
PULSE DURATION
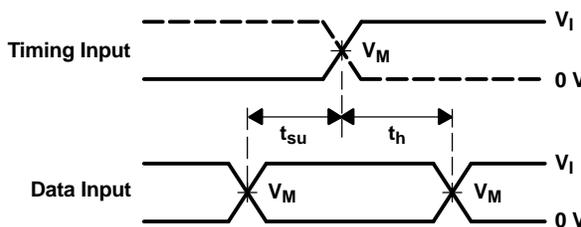
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
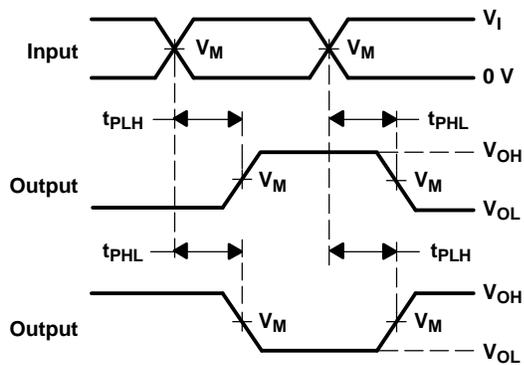
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS
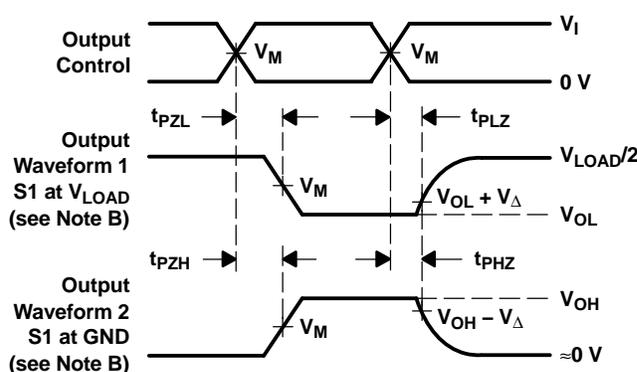
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
74LVCH16543ADGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVCH16543ADGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVCH16543ADGVRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVCH16543ADGVRG4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVCH16543ADLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVCH16543ADGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVCH16543ADGVR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVCH16543ADL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVCH16543ADLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVCH16543ADLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVCH16543AGQLR	OBSOLETE	BGA MICROSTAR JUNIOR	GQL	56		TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCH16543ADGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74LVCH16543ADGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74LVCH16543ADLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS
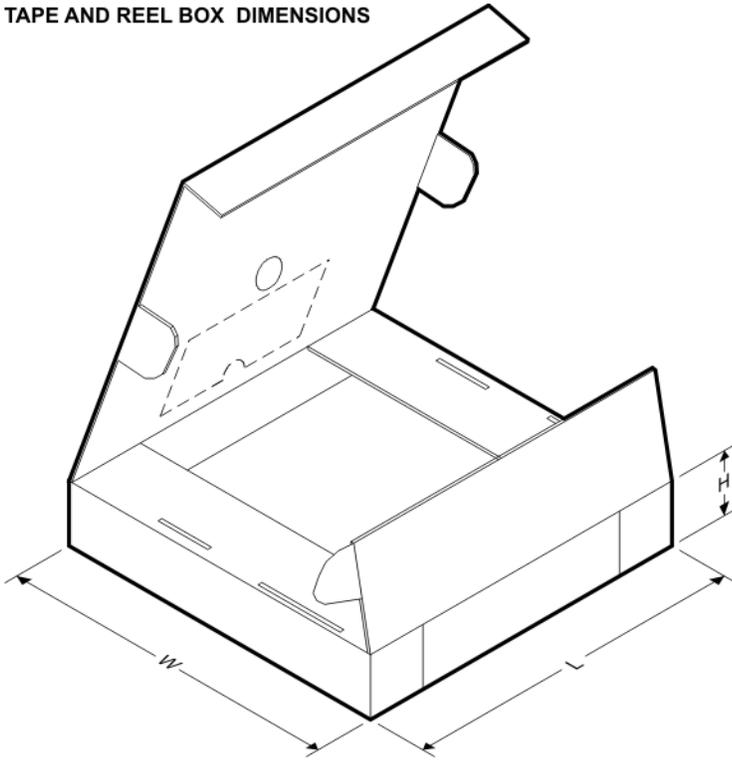
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCH16543ADGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74LVCH16543ADGVR	TVSOP	DGV	56	2000	367.0	367.0	45.0
SN74LVCH16543ADLR	SSOP	DL	56	1000	367.0	367.0	55.0

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN
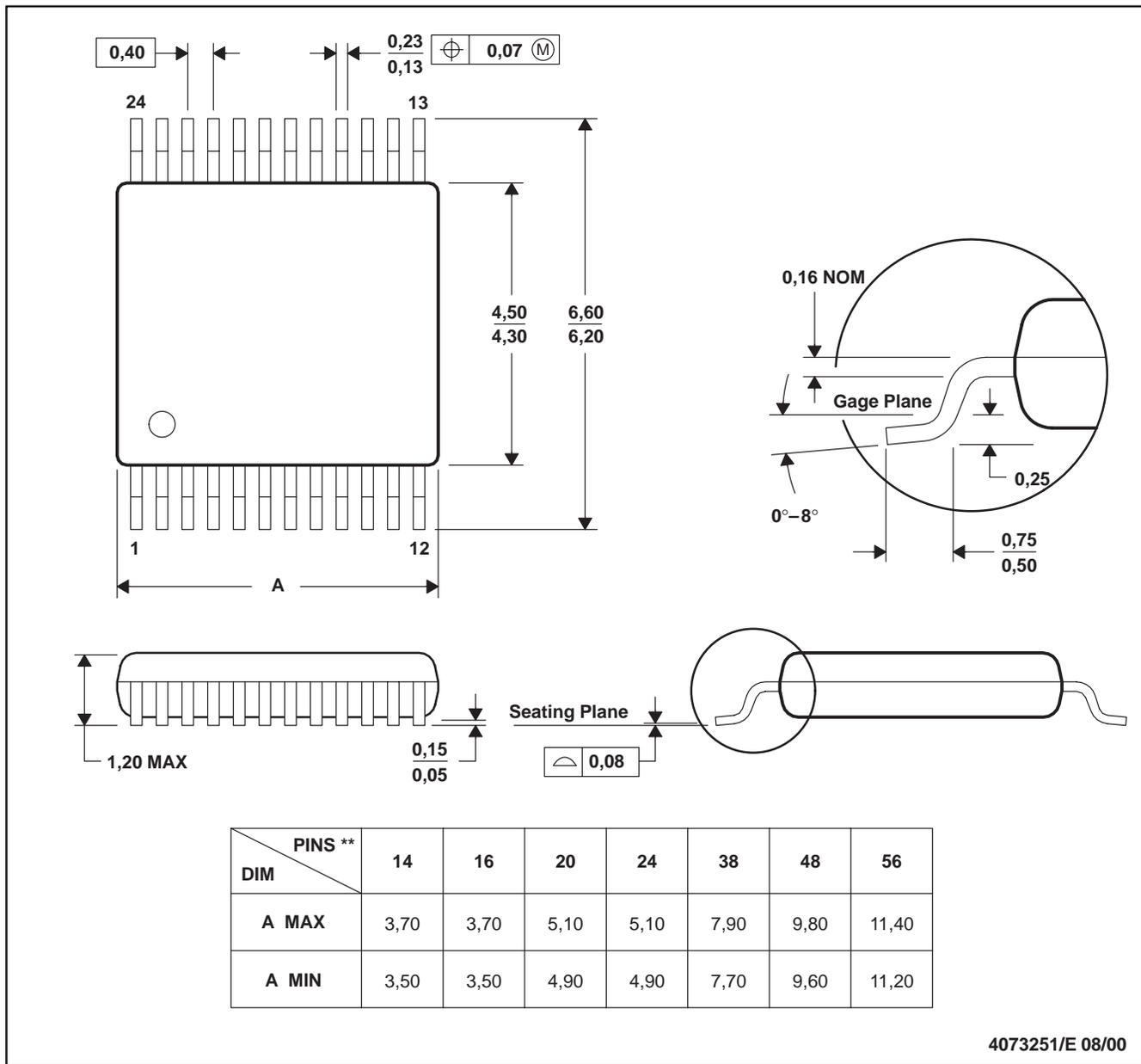
PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
        D. Falls within JEDEC: 24/48 Pins – MO-153
                                 14/16/20/56 Pins – MO-194

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

GQL (R−PBGA−N56)   PLASTIC BALL GRID ARRAY

4,60 / 4,40

7,10 / 6,90

A1 Corner

1,00 Max

0,35 / 0,15

0,10 C

Seating Plane

3,25

0,65

0,325

3X Via Hole Without Ball

Missing Via Hole Indicates Pin A1 Quadrant

0,65

5,85

0,325

K J H G F E D C B A

1 2 3 4 5 6

Bottom View

56X Ø 0,45 / 0,35

Ø 0,15 (M) C A B
Ø 0,08 (M) C

4200583−3/K   06/2007
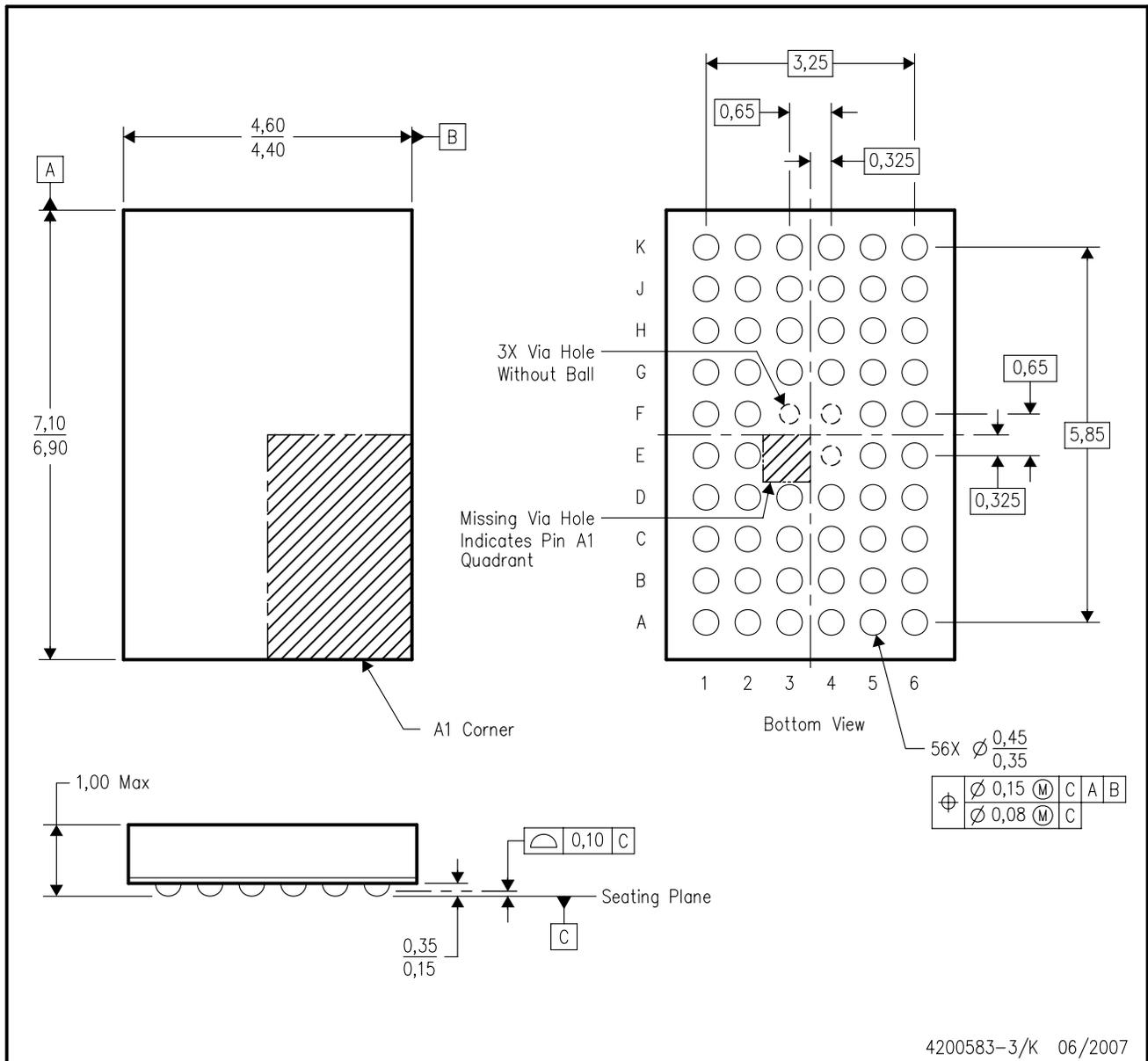
NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
B.   This drawing is subject to change without notice.
C.   Falls within JEDEC MO−285 variation BA−2.
D.   This package is tin−lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead−free.

DL (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

0.025 (0,635)

$\dfrac{0.0135\ (0,343)}{0.008\ (0,203)}$

⊕ 0.005 (0,13) Ⓜ

48   25

$\dfrac{0.299\ (7,59)}{0.291\ (7,39)}$

$\dfrac{0.420\ (10,67)}{0.395\ (10,03)}$

$\dfrac{0.010\ (0,25)}{0.005\ (0,13)}$

Gage Plane

0.010 (0,25)

0°–8°

$\dfrac{0.040\ (1,02)}{0.020\ (0,51)}$

1   24

A

0.110 (2,79) MAX   0.008 (0,20) MIN

Seating Plane

△ 0.004 (0,10)

PINS ** / DIM	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048 / E 12/01
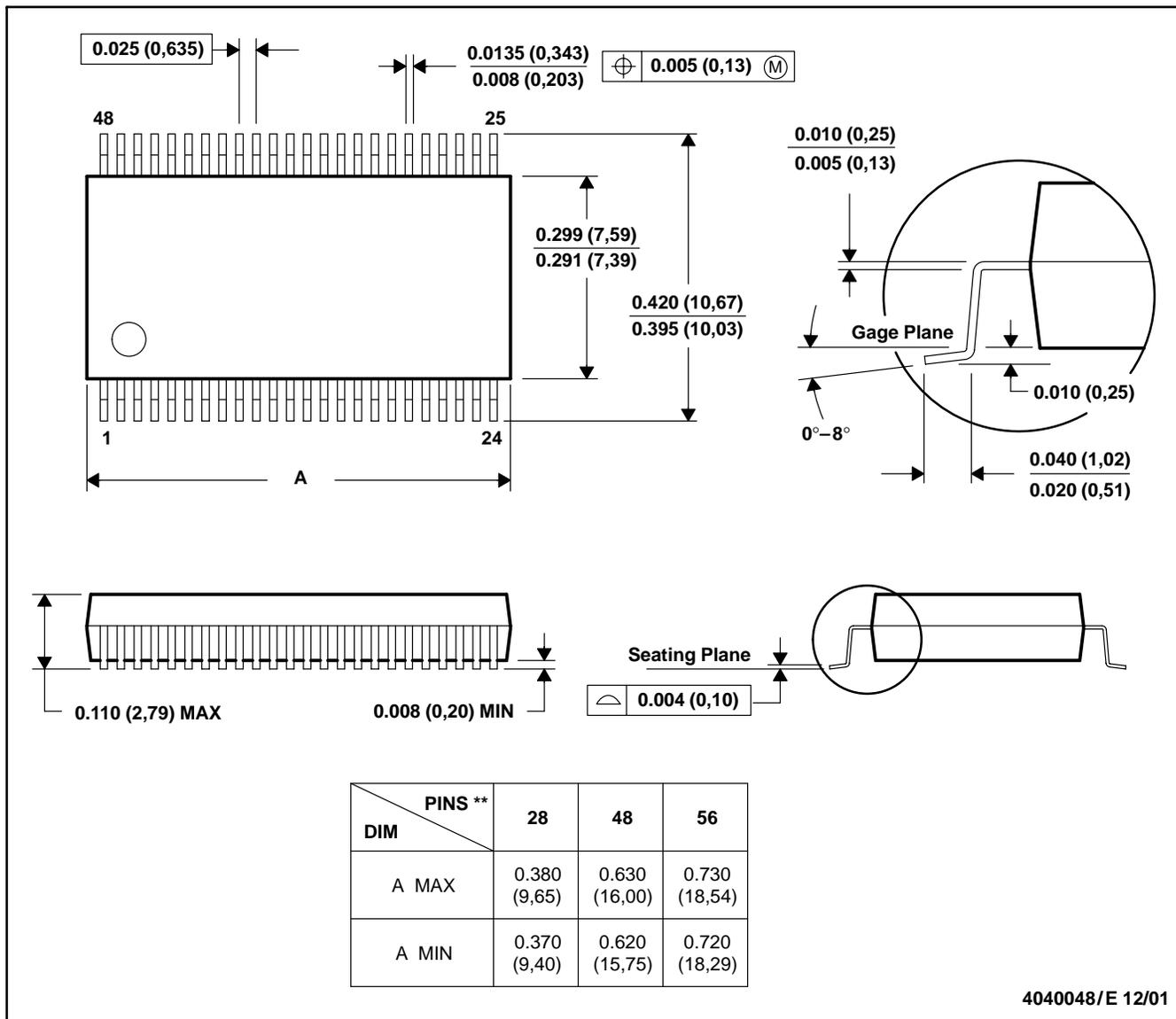
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

DGG (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE PACKAGE**
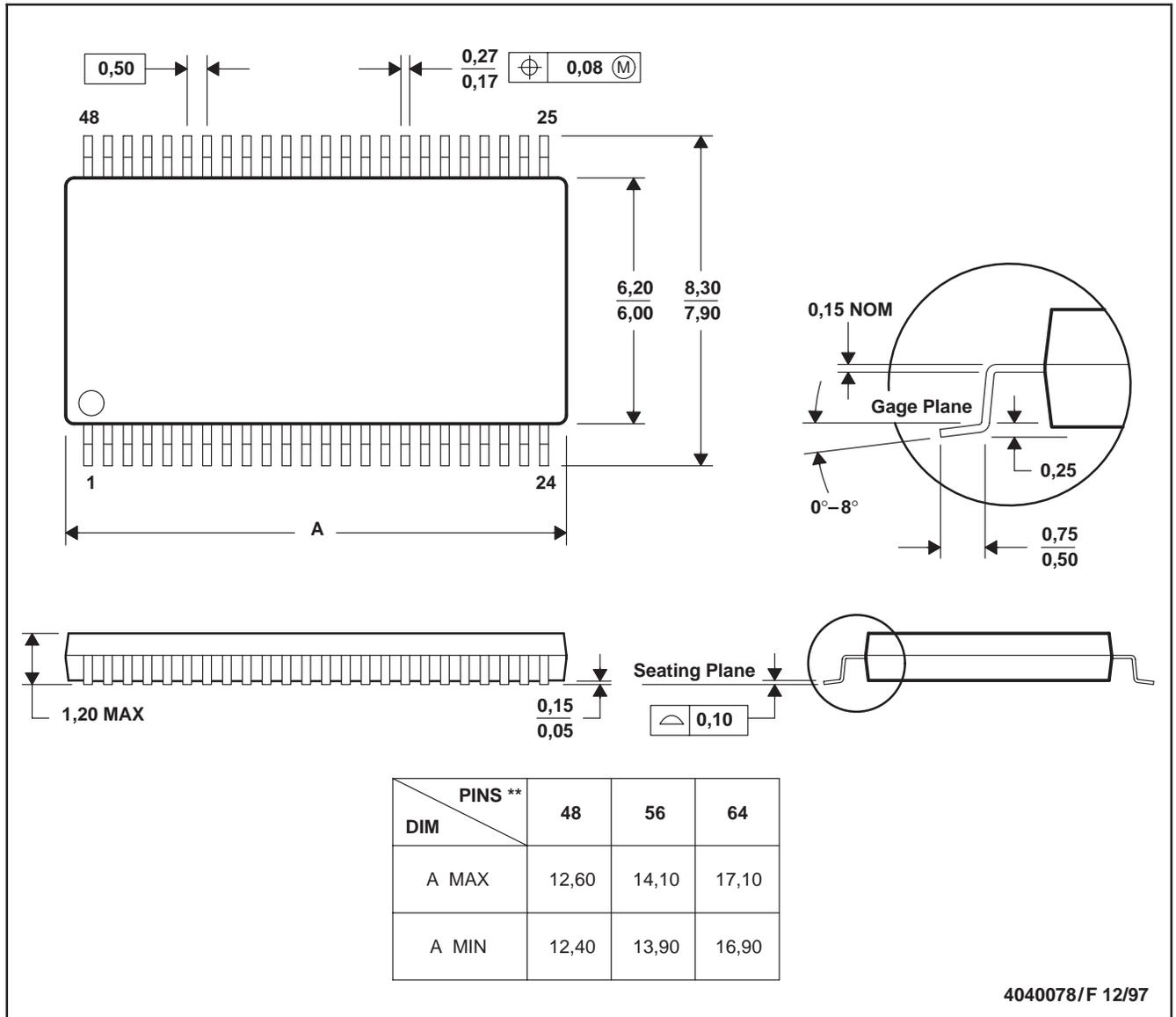
48 PINS SHOWN

	PINS **	48	56	64
DIM				
A MAX		12,60	14,10	17,10
A MIN		12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold protrusion not to exceed 0,15.
   D. Falls within JEDEC MO-153

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265