

SN74LVTH32373-EP

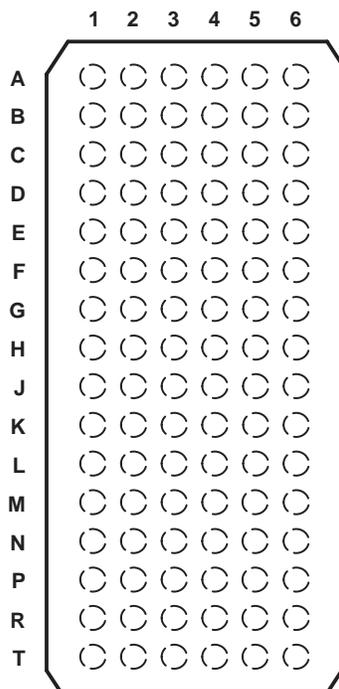
3.3-V ABT 32-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

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- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Member of the Texas Instruments Widebus+™ Family**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Supports Unregulated Battery Operation Down To 2.7 V**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

**GKE PACKAGE
(TOP VIEW)**



terminal assignments

	1	2	3	4	5	6
A	1Q2	1Q1	$\overline{1OE}$	1LE	1D1	1D2
B	1Q4	1Q3	GND	GND	1D3	1D4
C	1Q6	1Q5	1V _{CC}	1V _{CC}	1D5	1D6
D	1Q8	1Q7	GND	GND	1D7	1D8
E	2Q2	2Q1	GND	GND	2D1	2D2
F	2Q4	2Q3	1V _{CC}	1V _{CC}	2D3	2D4
G	2Q6	2Q5	GND	GND	2D5	2D6
H	2Q7	2Q8	$\overline{2OE}$	2LE	2D8	2D7
J	3Q2	3Q1	$\overline{3OE}$	3LE	3D1	3D2
K	3Q4	3Q3	GND	GND	3D3	3D4
L	3Q6	3Q5	2V _{CC}	2V _{CC}	3D5	3D6
M	3Q8	3Q7	GND	GND	3D7	3D8
N	4Q2	4Q1	GND	GND	4D1	4D2
P	4Q4	4Q3	2V _{CC}	2V _{CC}	4D3	4D4
R	4Q6	4Q5	GND	GND	4D5	4D6
T	4Q7	4Q8	$\overline{4OE}$	4LE	4D8	4D7



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description/ordering information

The SN74LVTH32373 is a 32-bit transparent D-type latch designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

This device can be used as four 8-bit latches, two 16-bit latches, or one 32-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	LFBGA – GKE	Tape and reel	CLVTH32373IGKEREPEP	L373EP

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

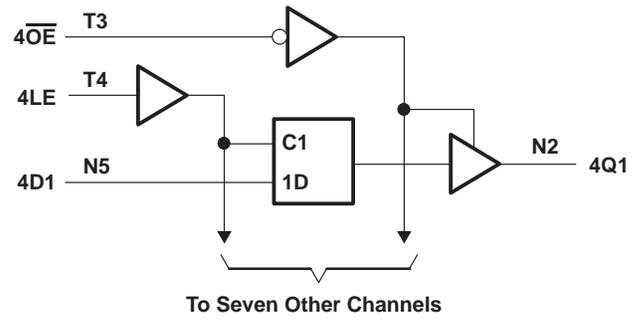
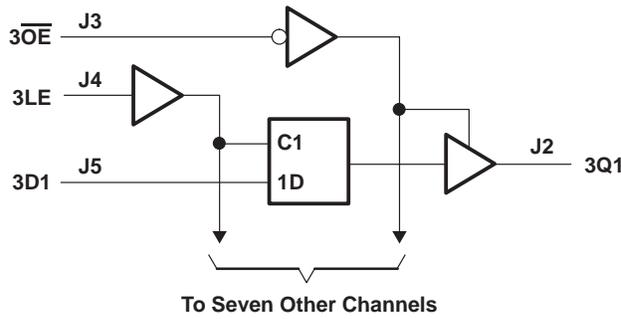
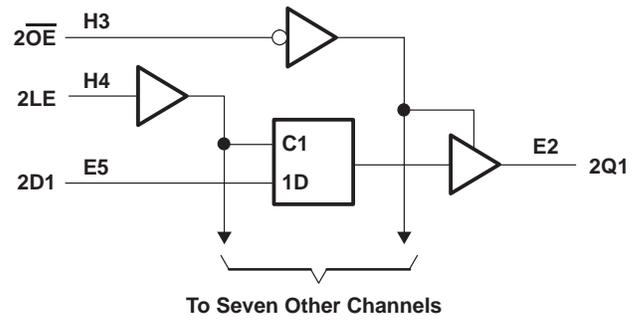
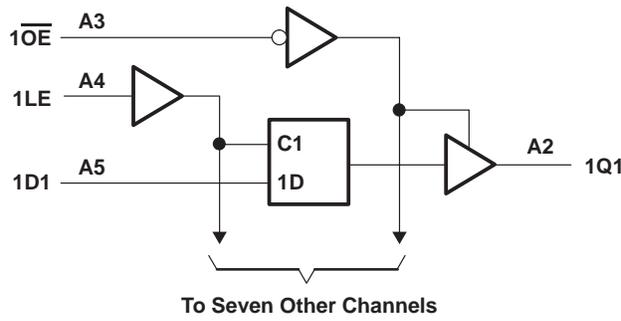
FUNCTION TABLE
(each 8-bit latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

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logic diagram (positive logic)



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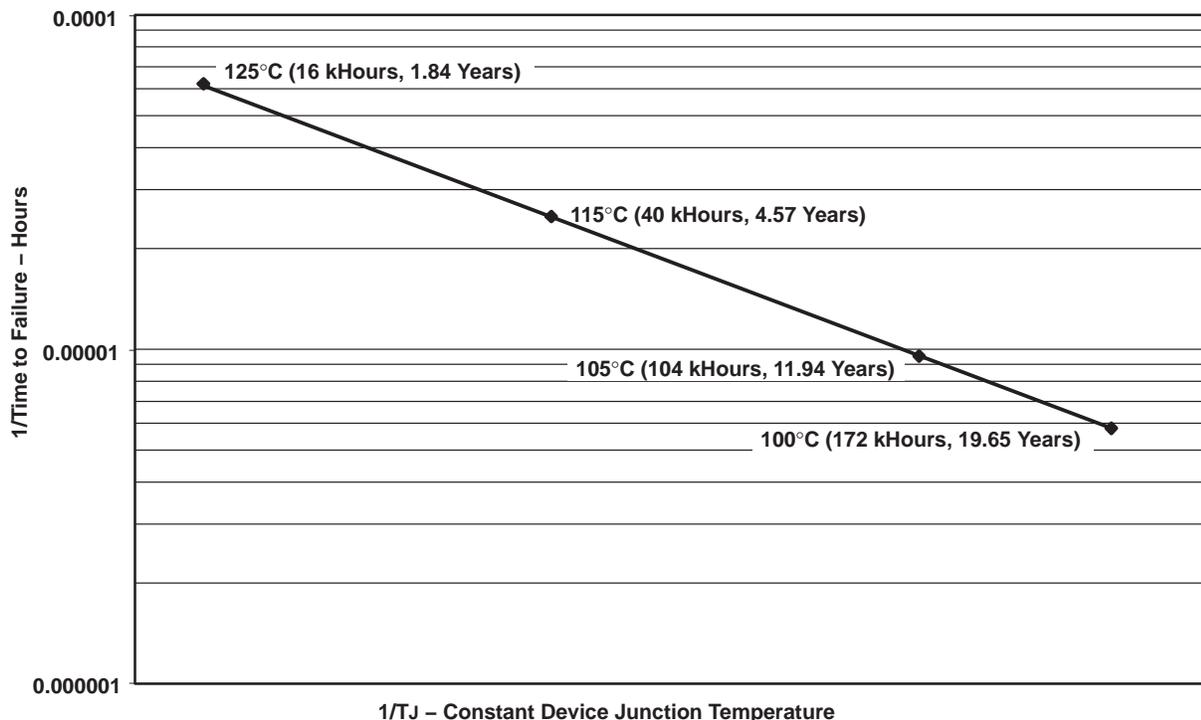
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O	128 mA
Current into any output in the high state, I_O (see Note 2)	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 3)	40°C/W
Storage temperature range, T_{stg} (see Note 4)	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See Figure 1 for additional information on thermal derating.



**Figure 1. Estimated Wirebond Life
 Based on Elevated-Temperature Kirkendall-Voiding Failure Mode**



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recommended operating conditions (see Note 5)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	2.7	3.6	V	
V _{IH}	High-level input voltage	2		V	
V _{IL}	Low-level input voltage		0.8	V	
V _I	Input voltage		5.5	V	
I _{OH}	High-level output current		-32	mA	
I _{OL}	Low-level output current		64	mA	
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200			μs/V
T _A	Operating free-air temperature	-40	85		°C

NOTE 5: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}		V _{CC} = 2.7 V, I _I = -18 mA				-1.2	V
V _{OH}		V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA		V _{CC} -0.2			V
		V _{CC} = 2.7 V, I _{OH} = -8 mA		2.4			
		V _{CC} = 3 V, I _{OH} = -32 mA		2			
V _{OL}		V _{CC} = 2.7 V		I _{OL} = 100 μA		0.2	V
				I _{OL} = 24 mA		0.5	
		V _{CC} = 3 V		I _{OL} = 16 mA		0.4	
				I _{OL} = 32 mA		0.5	
				I _{OL} = 64 mA		0.55	
I _I		V _{CC} = 0 or 3.6 V, V _I = 5.5 V			10	μA	
		Control inputs V _{CC} = 3.6 V, V _I = V _{CC} or GND			±1		
		Data inputs V _{CC} = 3.6 V, V _I = V _{CC}			1		
		V _I = 0			-5		
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V				±100	μA
I _{I(hold)}		V _{CC} = 3 V		V _I = 0.8 V		75	μA
				V _I = 2 V		-75	
		V _{CC} = 3.6 V, ‡		V _I = 0 to 3.6 V			
I _{OZH}		V _{CC} = 3.6 V, V _O = 3 V				5	μA
I _{OZL}		V _{CC} = 3.6 V, V _O = 0.5 V				-5	μA
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, \overline{OE} = don't care				±100	μA
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, \overline{OE} = don't care				±100	μA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		0.38	mA
				Outputs low		10	
				Outputs disabled		0.38	
ΔI _{CC} §		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				0.2	mA
C _i		V _I = 3 V or 0				3	pF
C _o		V _O = 3 V or 0				9	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
		MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high	3		3		ns
t _{su}	Setup time, data before LE↓	1		0.6		ns
t _h	Hold time, data after LE↓	1		1.1		ns



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

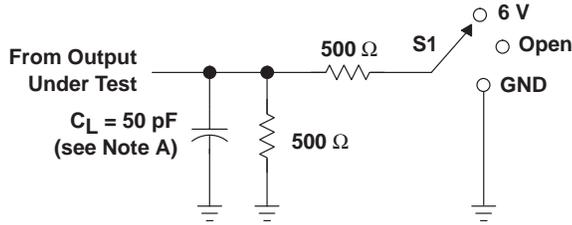
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		UNIT
			MIN	TYP†	MAX	MIN	MAX	
t _{PLH}	D	Q	1.5	2.7	3.8	4.2		ns
t _{PHL}			1.5	2.5	3.6	4		
t _{PLH}	LE	Q	2.1	3	4.3	4.8		ns
t _{PHL}			2.1	2.9	4	4		
t _{PZH}	\overline{OE}	Q	1.5	2.8	4.3	5.1		ns
t _{PZL}			1.5	2.8	4.3	4.7		
t _{PHZ}	\overline{OE}	Q	2.4	3.5	5	5.4		ns
t _{PLZ}			2	3.2	4.7	4.8		
t _{sk(o)}			0.5					ns

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

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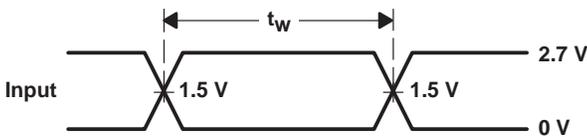
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PARAMETER MEASUREMENT INFORMATION

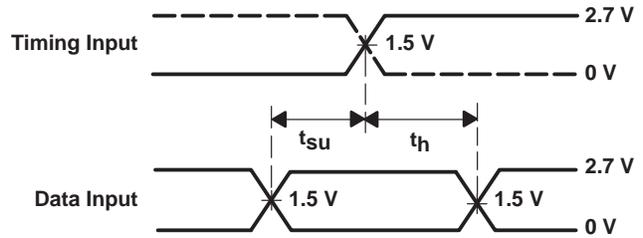


LOAD CIRCUIT

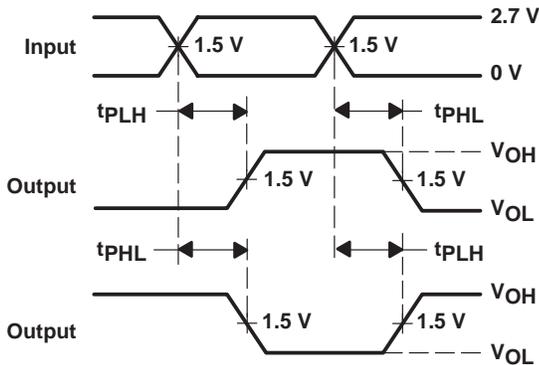
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



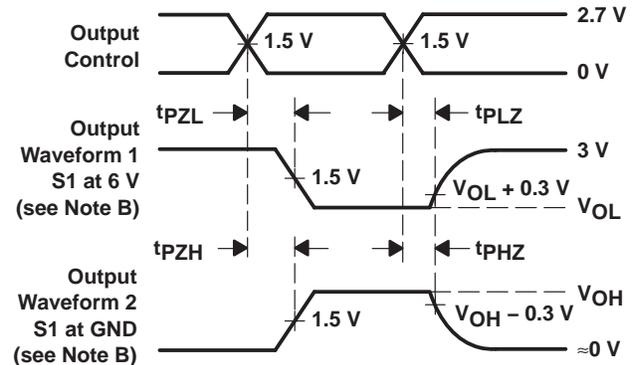
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CLVTH32373IGKEREP	ACTIVE	LFBGA	GKE	96	1000	TBD	SNPB	Level-3-220C-168 HR	-40 to 85	L373EP	Samples
V62/04721-01XA	ACTIVE	LFBGA	GKE	96	1000	TBD	SNPB	Level-3-220C-168 HR	-40 to 85	L373EP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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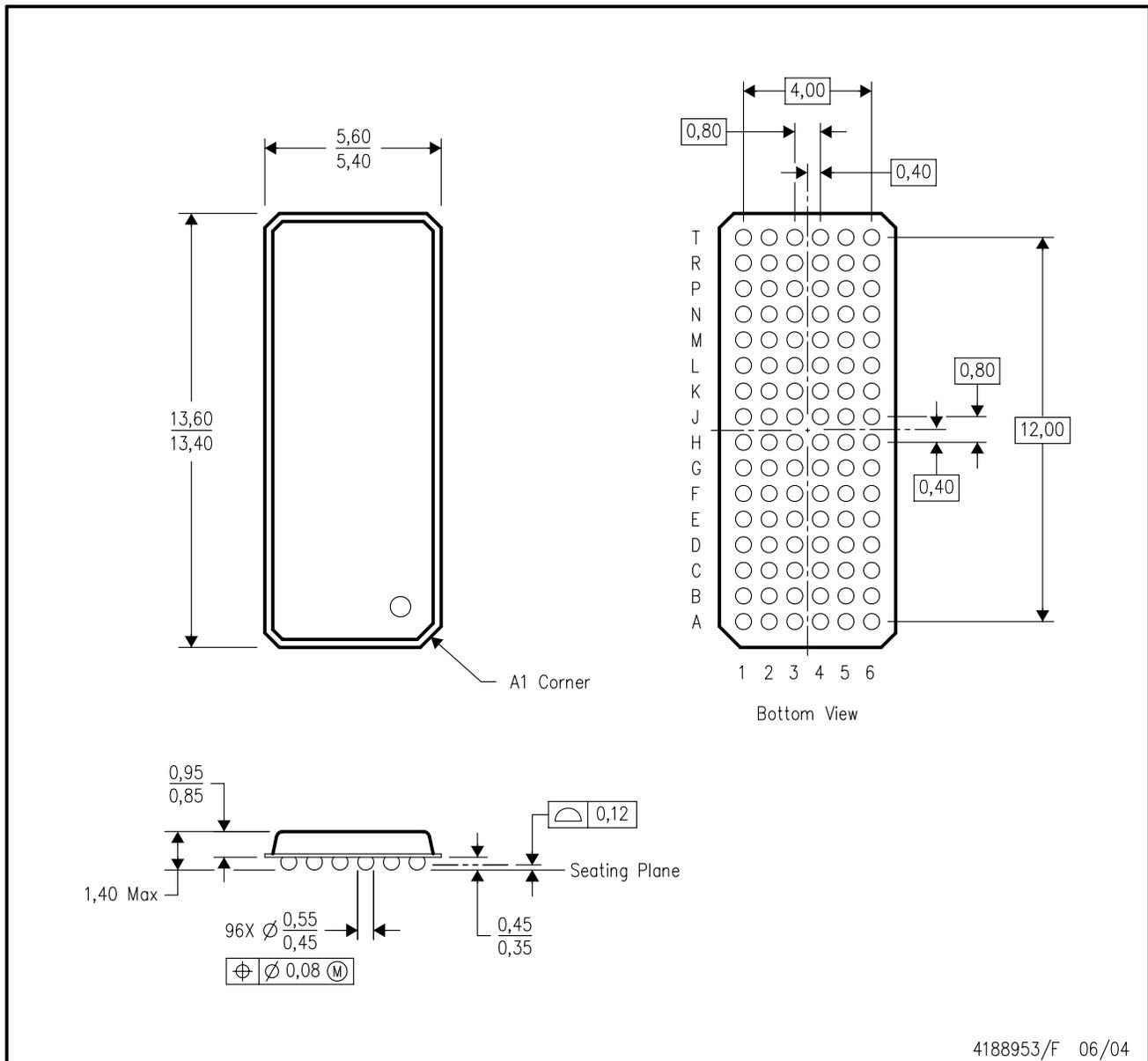
- Catalog: [SN74LVTH32373](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation CC.
 - D. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

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